Testing and characterization of IEEE 802.15.4 ZigBee Radio Transceiver

A Project Report

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THESIS CERTIFICATE

This is to certify that the thesis titled **Testing and characterization of IEEE 802.15.4 ZigBee Radio Transceiver**, submitted by **Debasish Behera**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology**, is a bona fide record of the project work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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I thank Vallabhaneni.M and Divya Kesharwani for helping me continuously during the course of my work.Without their help it would have been difficult to take this project to this extent.

Finally I dedicate this thesis to my parents for their support and encouragement through all these years. This work would not have been possible without their love and understanding.

ABSTRACT

This project is part of a project dealing with the design of a zigbee radio transceiver.The project involves the testing and validating a IEEE 802.15.4 zigbee radio transceiver.

A rectangular microstrip antenna for zigbee transceiver was fabricated and tested using Vector network analyzer(VNA).An impedance bandwidth of 195MHz was obtained from 2.385GHz to 2.560GHz which satisfies zigbee requirements(2.405GHz-2.480GHz).

This transceiver is controlled by a control register.A verilog code was written and implemented on spartan-3 FPGA board to pass data to the control register.A PCB test board was designed for the zigbee chip. In all 8 chips were tested,out of which only chip 4 and chip 2 are working.Chip 4 is tested under different conditions and voltage controlled oscillator(VCO) is characterized by plotting output frequency versus control voltage.

Power amplifier(PA) is characterized by changing its control pins,$txpower[3:0]$ and measuring its output power.But the output power is very low in comparison to the specification specified by zigbee(0dBm).The maximum output power delivered is -19.5dBm.In nut shell,the PLL is working properly.There are some issues with power amplifier which have to be sorted out.

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CHAPTER 1

Introduction

The need for ubiquitous mobile computing and networking has lead to the development of various wireless standards by the IEEE in consortium with the industry over the last decade. ZigBee is a new industrial standard for ad hoc networks based on IEEE 802.15.4. It is used for low data rate wireless networks and sensor networks. It was developed as a wireless standard for Wireless-Personal Area Networks working at data rates up to 250 Kbps. Typical operational range of target appliances is around 10 metres. It can be easily incorporated into devices used in home automation, PC peripherals and health care appliances.

The prime concern in the transceiver design is low cost and low power. So, it is important to minimize the use of off-chip components as much as possible. Therefore, direct conversion was used for the transceiver. The design and implementation of the Zigbee transceiver is a collaborative effort of previous year students .This thesis deals with the characterization and validation of the Phase locked loop (PLL) and transmitter chain through hardware testing.An active integrated antenna for zigbee transceiver is fabricated and tested.

1.1 Organization of Thesis

Chapter 2 explains the design of the antenna.It deals with the comparison of results obtained from simulation with that from VNA.

Chapter 3 explains the architecture of the zigbee chip.

Chapter 4 explains the programming of the control register

Chapter 5 It deals with the measurements related to PLL and power amplifier.

Chapter 6 Layout of antenna and board.

Chapter 7 Conclusions.

CHAPTER 2

Antenna Measurements

2.1 Introduction

The transceiver block requires a receiver antenna and a transmitter antenna. The rectangular microstrip antenna(RMSA) is one of simplest and most widely used MSA antenna. Microstrip antennas have recently received much attention due to the increasing demand of small antennas for personal communications equipment. It consists of a LxW radiating patch placed on a dielectric substrate, the other end being an infinite ground plane. The patch is excited by the connector in the coaxial cable

2.2 Antenna Properties

2.2.1 Voltage Standing Wave Ratio(VSWR)

When we fail to match the impedance of an antenna to its input transmission line leading from the transmitter or to the receiver, the system degrades due to reflected power. The input impedance is measured with respect to some transmission line or source characteristic impedance. When the two are not the same, a voltage wave is

reflected, ρV , where ρ is voltage reflection coefficient:

$$\rho = \frac{Z_A - Z_O}{Z_A + Z_O} \tag{2.1}$$

where Z_A is the antenna impedance and Z_O is the measurement characteristics impedance. On a transmission line the two traveling waves, incident and reflected, produce a standing wave.

$$V_{max} = (1 + |\rho|)V_i \tag{2.2}$$

$$V_{min} = (1 - |\rho|)V_i \tag{2.3}$$

$$VSWR = \frac{V_{max}}{V_{min}} = \frac{1 + |\rho|}{1 - |\rho|} \tag{2.4}$$

VSWR is voltage standing wave ratio.The reflected power is given by $V_i^2 \frac{|\rho|^2}{Z_o}$.The incident power is $\frac{V_i^2}{Z_o}$.The ratio of reflected power to incident power is $|\rho|^2$.It is the returned power ratio:

$$Return\ loss = -20log|\rho| \tag{2.5}$$

2.2.2 Bandwidth of Antenna

The bandwidth can be considered to be the range of frequencies on either side of a centre frequency (usually the resonance frequency) where the antenna characteristics (such as input impedance,pattern,gain) are within an acceptable value of those at centre frequency.For the antenna designed,bandwidth is defined as the range of frequencies over which return loss is less than 10dB.In other words,VSWR ρ is less

that $\frac{1}{3}$.

2.3 Dual tuning effect

If the antenna is excited at two frequencies f1 and f2, where f1 and f2 are close to each other, it is possible to get good impedance matching in a large band of frequencies. A graphical illustration is shown in Fig.2.1

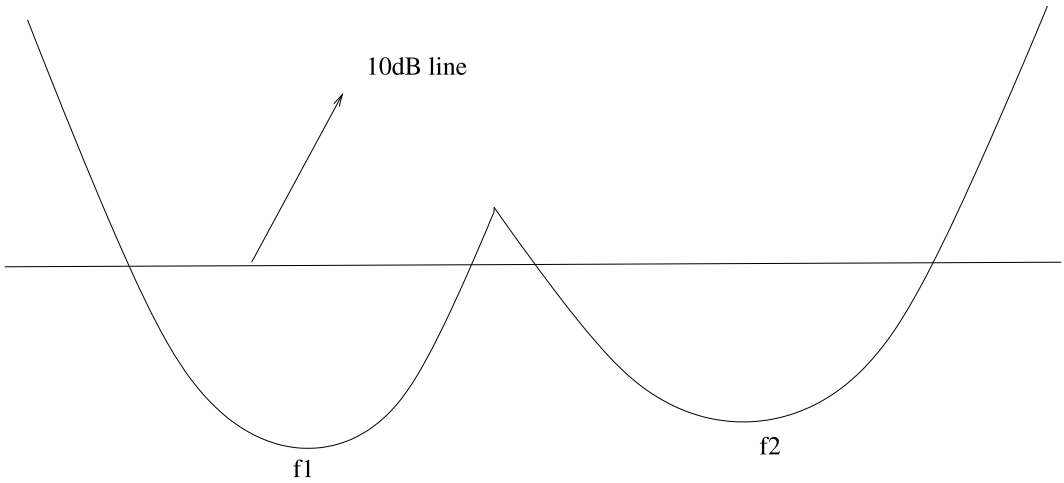

Figure 2.1: Concept of dual tuning

2.4 Gap-coupled antennas

A patch placed close to the fed patch gets excited through the coupling between the two patches. Such a patch is known as a parasitic patch. It has been observed that addition of parasitic patches increases bandwidth if the two resonating frequencies are close to each other.Parasitic patches can be placed closed to both radiating and non-radiating edges of the patch. If parasitic patch is placed close to radiating edges of the patch it is called radiating edge gap-coupled microstrip antennaand if it is

placed close to non-radiating edge it is known as non-radiating edge gap-coupled antennas.

2.5 Selection of antenna

After studying various antenna designs discussed in [2].We decided to go for NEGCOMA because it is easiest to fabricate.One can use other antennas but due to their larger size they are bulky. NEGCOMA has an impedance bandwidth of 102.2MHz from 2395.8MHz to 2498MHz.This impedance bandwidth satisfies the 80MHz band required for zigbee.

2.5.1 NEGCOMA

NEGCOMA exploits the idea of adding parasitic patches along the non-radiating edges to increase impedance bandwidth.An antenna is fabricated with the specifications shown in Table.2.1.The antenna has three resonant frequencies which combine together to give a large impedance bandwidth.But we observed only two resonant frequencies.In reality there are three resonant frequencies out of which two are close to each other so we saw only two resonant frequencies.We used VNA E8362B(10MHz-20GHz) PNA series vector network analyzer.

Dimensons of the antenna are shown in Fig.2.2

Table 2.1: Specifications of antenna

Parameter	*Name*	*Value*
ϵ_r	*Dielectric constant*	4.4
H	*Substrate thickenss*	$1.6mm$
T	*Metal thickness*	$35\mu m$
μ_r	*Relative permittivity*	1
σ	*Conductivity*	$4.37 \times 10^7 S/m$

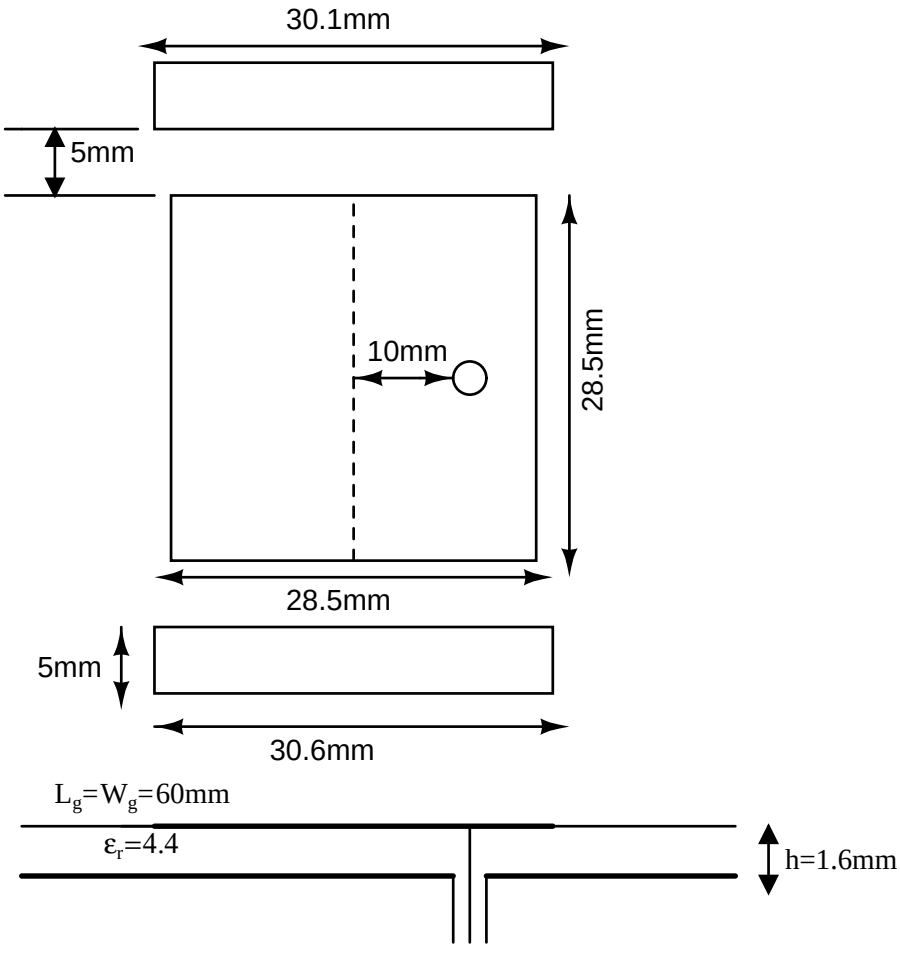

Figure 2.2: Dimensions of antenna

2.6 Results obtained from VNA

2.6.1 Feed from the non-radiating side:

The results are shown in fig.2.3

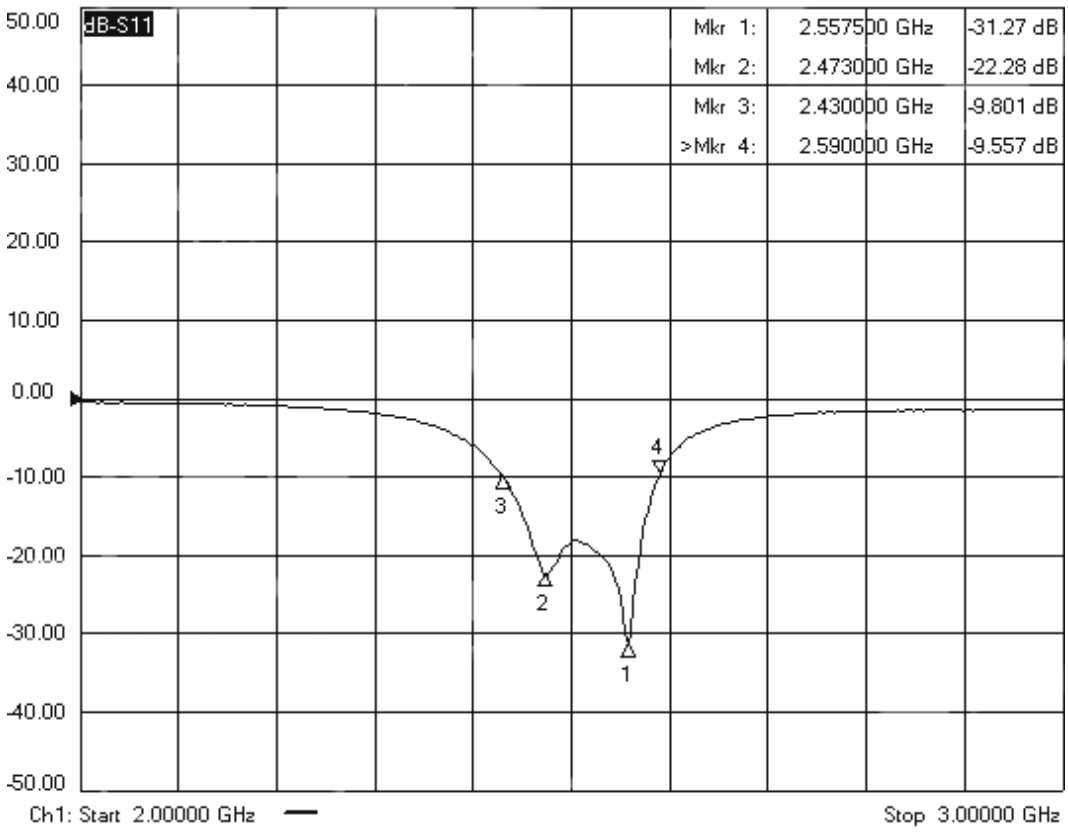

Figure 2.3: Return loss in dB for feed from non-radiating plane

From Fig.2.3,the return loss(dB) plot intersects the 10dB line at marker3 and marker4.Therefore,the bandwidth obtained is 160MHz but it ranges from 2.430GHz to 2.590GHz.From smith chart fig.2.4,the impedance offered by the antenna within the bandwidth is close to 50Ω.There are three resonant frequencies. one at 2.5575GHz and other two are very close to 2.473GHz.

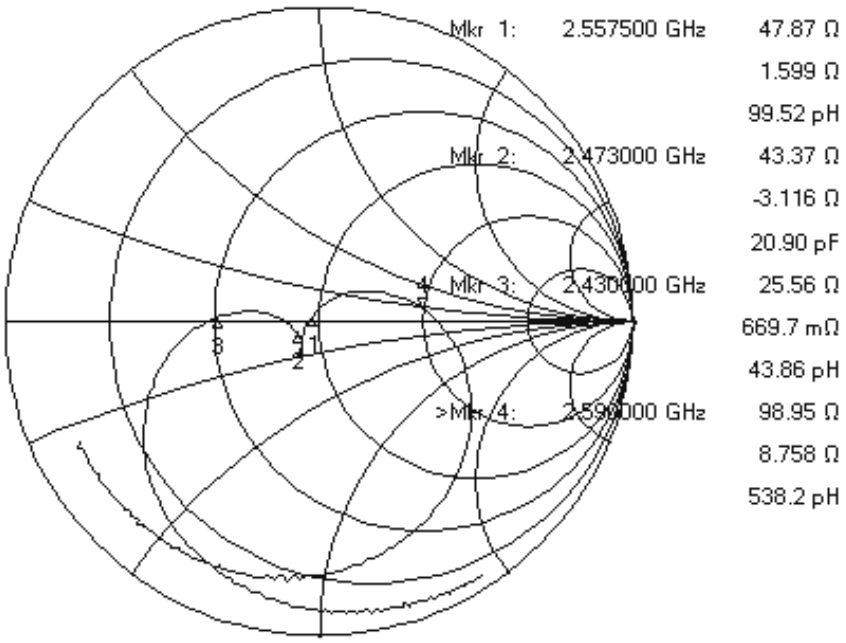

Figure 2.4: Smith chart for feed from non-radiating plane

2.6.2 Feed from the radiating side:

The results are shown in fig.2.5

In fig.2.5 the return loss(dB) plot intersects the 10dB line at 2.365GHz and at 2.560GHz.Therefore,impedance bandwidth is 175MHz which is good enough for zigbee(2.405GHz-2.480GHz).From smith chart fig.2.6,the impedance offered by the antenna within the bandwidth is close to 50Ω.There are three resonant frequencies. one at 2.426GHz and other two are very close to 2.55GHz.

A comparison between simulation results and the results obtained from vector

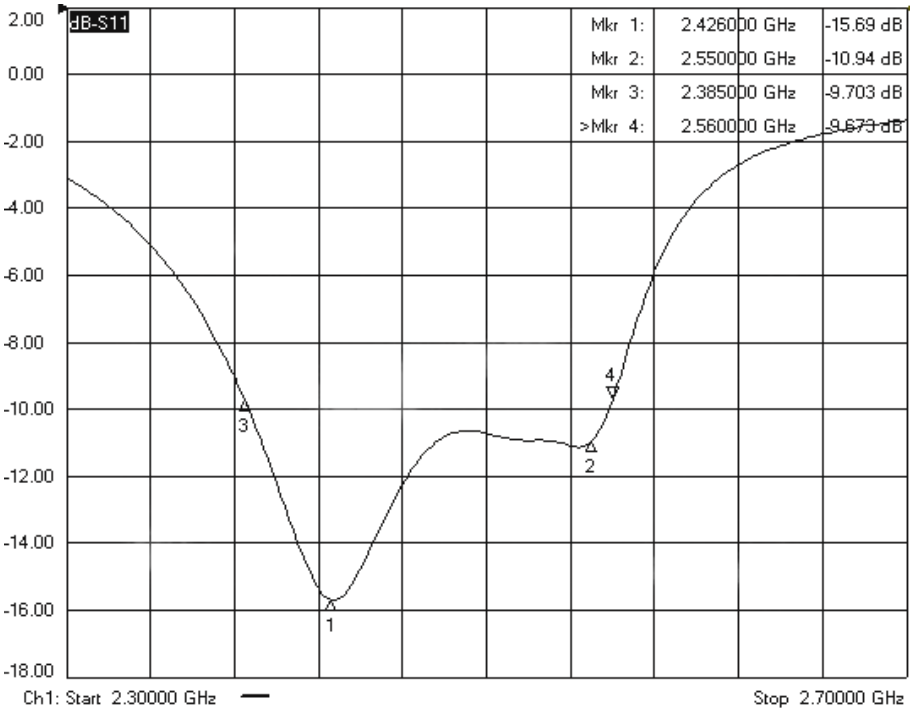

Figure 2.5: Return loss in dB for feed from radiating plane

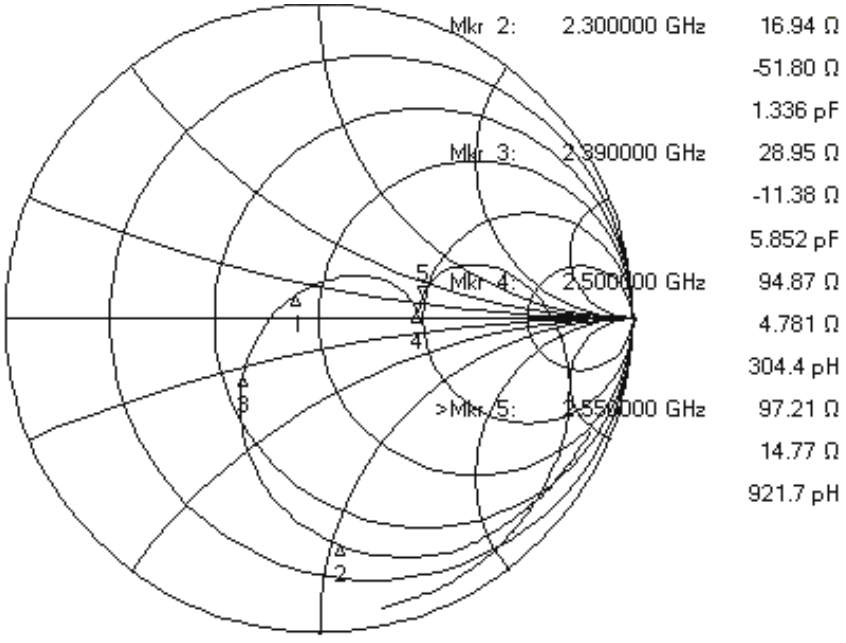

Figure 2.6: Smith chart for feed from radiating plane

network analyzer (VNA) is presented in table.2.2

Table 2.2: Comparison between simulated and measured values

Antenna	Frequency range(MHz)	Impedance bandwidth(MHz)
Simulation results	2395.8-2498	102.2
Coaxial feed from non-radiating side	2430-2590	160
Coaxial feed from radiating side	2365-2560	175

CHAPTER 3

The ZigBee Architecture

3.1 Zero-IF architecture

There are many transceiver architectures available.Common architectures which are suitable for high level of integration are zero-IF(intermediate frequency) and low-IF.In zero-IF architecture(also called direct conversion or homo dyne architecture as shown in Fig.3.2 and fig.3.1,the RF spectrum is directly down converted to the base-band,thus eliminating IR(image rejection) filters.The subsequent filtering and gain amplification is all done in base-band at low frequencies.

However,there exists many design challenges with zero-IF like DC offset and $1/f$ noise of the signal path.Since the LO is at the same frequency as carrier,it may transmit to the antenna and get reflected,resulting in self-mixing.The resulting time-varying DC offset reduces the dynamic range and may saturate the subsequent base-band circuits.Since the main aim of designing this transceiver is low cost and minimize power consumption.Therefore,zero-IF architecture was selected for zigbee transceiver.

3.2 Description of the zigbee transceiver

Block diagram of zigbee transceiver is shown below:

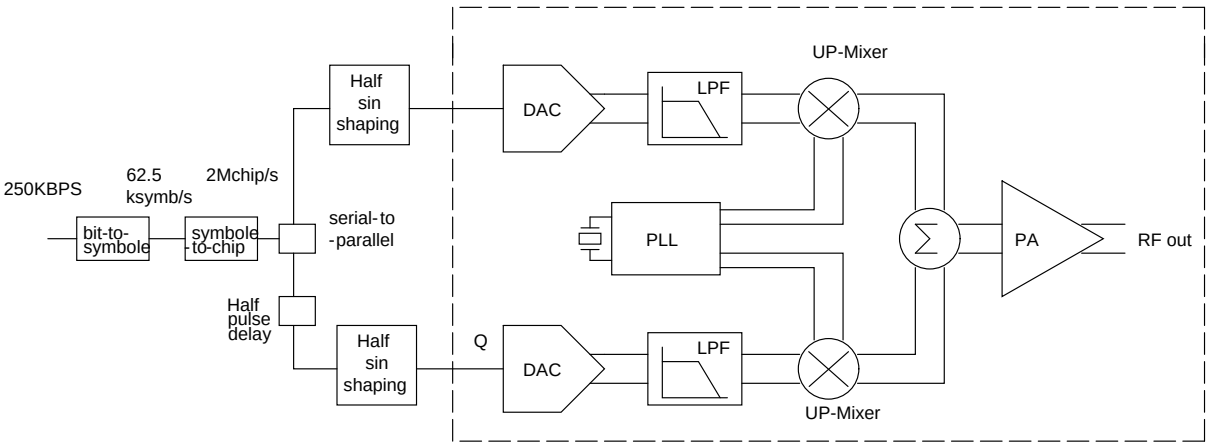

Figure 3.1: Block diagram of the transmitter[4]

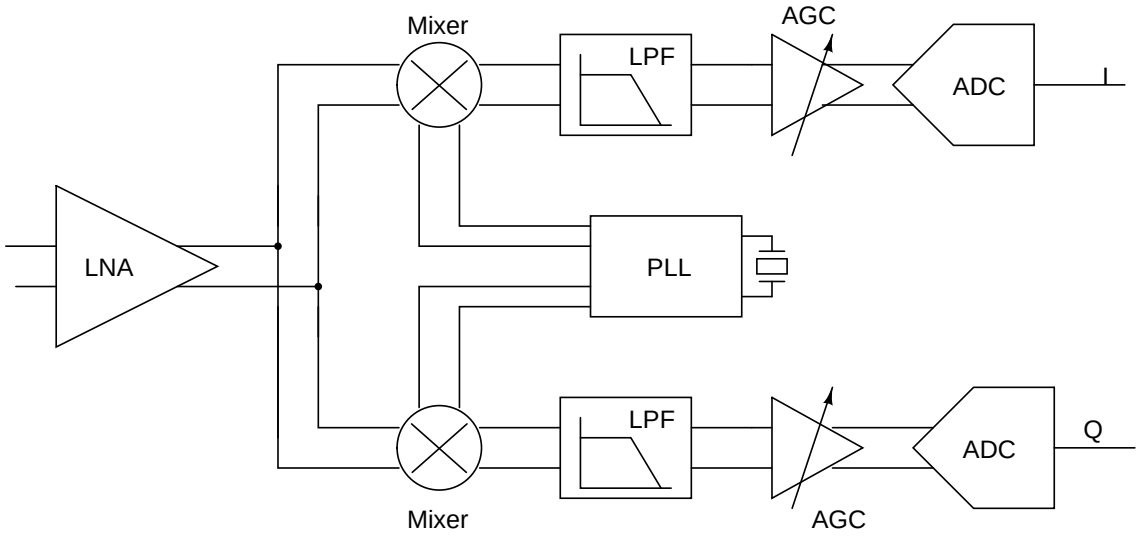

Figure 3.2: Block diagram of the receiver[4]

3.2.1 Brief description of blocks used in design

PLL LOOP

PLL is used to generate quadrature I and Q signals in the range from 2.405GHz-2.480GHz.LC based oscillator is used to design VCO.VCO is made to run at twice the required frequency and is subsequently divided by two to generate quadrature I and Q components.

Divider chain is the most power hungry block because it functions at the highest frequency.Therefore,CML dividers are used because they consume less power compared to CMOS at these frequencies.There is a fixed divider count of 480.Divider can be programmed from 480 to 496.However,divider modulus can go up to 511.The unity gain frequency of loop gain is $f_u \approx 35$KHz.

Zigbee Tx

It consists of DAC,LPF,mixer and power amplifier(PA) required in transmitter chain.4-bit DAC and LPF are used to convert the binary $txdataI[3:0]$ and $txdataQ[3:0]$ components into analog signals.Mixer has been implemented with sufficient linearity and special care has been taken to minimize the mismatch between I and Q paths.Mixer gain is set to -3.5dB.

Class AB configuration is chosen for the power amplifier.Output power can be varied with the $txpower<3:0>$ pins available on the IC.

LNA and MIXER

LNA amplifies the weak received signal using either 1dB or 15dB gain.High gain(15dB) mode is used when incoming signal power is from -85dBm to -60dBm and low gain mode is used when it is from -60dBm to -20dBm.To maintain linearity gilbert mixer was chosen.The output of the mixer is passed through a low pass filter.For testing purposes,output of the filter is brought out as $FB\_I+, FB\_I-, FB\_Q+, FB\_Q-$.

VGA and ADC

VGA is used to amplify the weak incoming signal with required gain such that the input to ADC covers its full range of 3V peak-to-peak.4-bit ADC is used to switch from the analog processing to digital base-band processing.

MEM_DIFF

This is the control block for the zigbee transceiver.Its a control register with 4 address lines and 8 data lines.It is explained in detail in chapter 4.

AM_CLOCKS_TOP

The input to this block is a 80MHz clock.It generates 16MHz DAC clock($dacclk$),16MHz ADC clock and 80MHz reference clock for PLL($fref_{pll}$).

BIAS_SOURCES_SINK

The functionality of this block is to provide bias currents.All the currents are generated from a 5μA reference.

The pin arrangement for the chip is shown in fig. 3.3

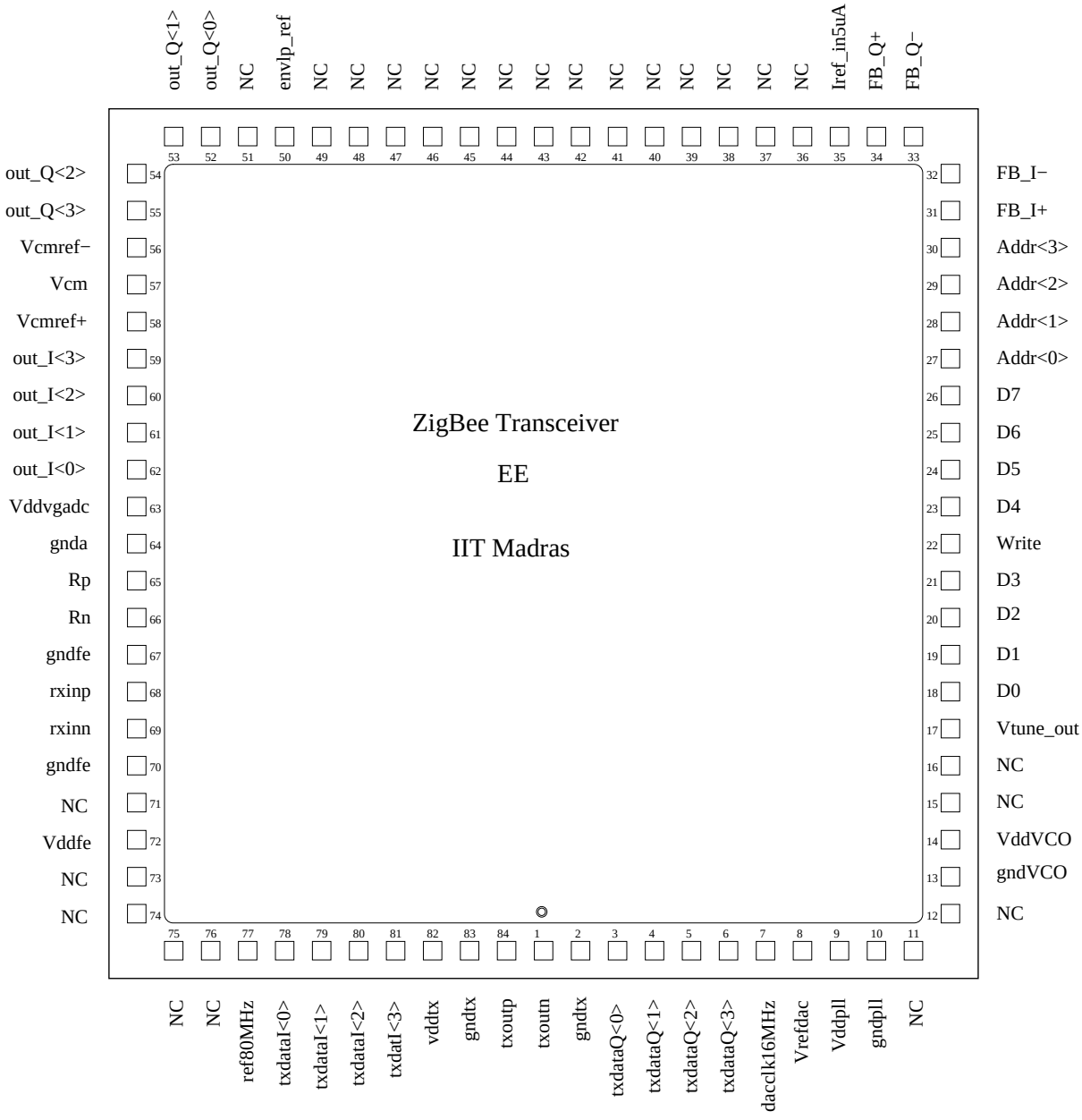

Figure 3.3: Pin description of chip

CHAPTER 4

The Control Register

As the name suggests,the functionality of control register is to control the analog blocks used in the zigbee transceiver digitally.The main tasks performed by the control register is to write data at specified addresses and programme the chip.The data bus is 8-bit wide and address bus is 4 bit wide.

The schematic for memory block is shown in fig.4.1

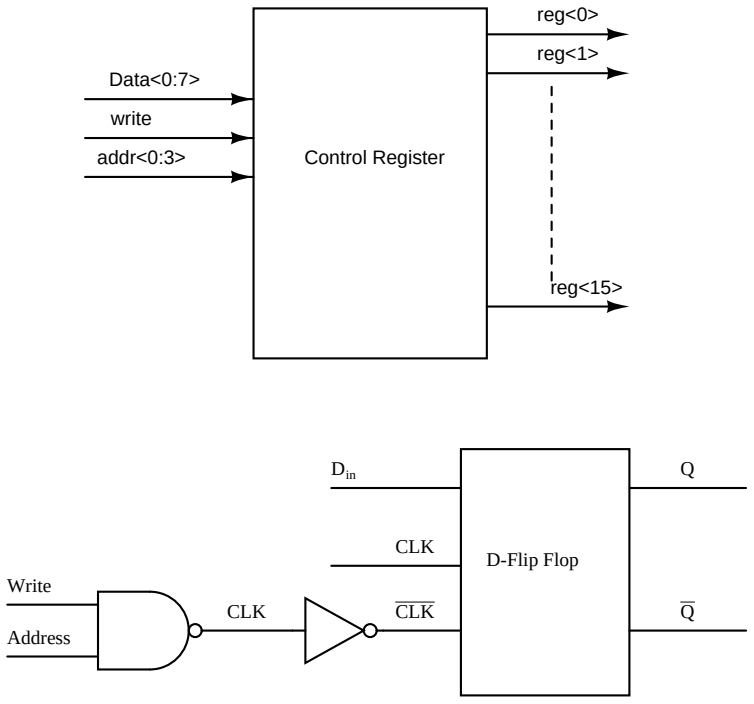

Figure 4.1: The control register and the D-flip flop

4.1 Mechanism of read and write

The D-flip flop used to design the register is shown in fig.4.1.

For writing $\overline{CLK}$ should be high.Data D_{in} is placed at the input,then required address is made high by the decoder.Then a write pulse will produce a positive edge on $\overline{CLK}$.At this edge,data D_{in} is written to the output Q. When write signal is low,$\overline{CLK}$ is also low.D-flip flop is in regenerative mode.Output cannot be changed even if there is a change in input data.

4.2 Registers used for zigbee transceiver

Out of 16 registers available 4 registers are used as control registers.The registers used are described below:

- **Register 11**:

  Its data bus consists of $txdummy < 7 : 5 >$,$txpd$,$txpower < 3 : 0 >$.$txpd$ low is used to power down the transmitter.$txpower < 3 : 0 >$ are used to control the power amplifier(PA).Make $txpower < i >$ low to activate power amplifier(PA).$txdummy < 7 : 5 >$ bits are don't care.

- **Register 12**:

  Its data bus consists of $plldummy < 7 : 5 >$,$modulus < 4 : 0 >$.$Modulus < 4 : 0 >$ sets the divider ratio in divider chain used in PLL.A fixed division ratio of 480 is used in the feedback path.$modulus < 4 : 0 >$ provides an increment over and above 480.So the minimum count is 480 for $modulus < 4 : 0 >$=00000 and

the maximum is 511 for $modulus < 4 : 0 >$=11111.But zigbee specifications limits the divider ratio to 496($modulus < 4 :>= 10000$).Plldummy bits are don't care.

- **Register 13**:

  Its data bus consists of $vcodummy$,$vcoIbias < 2 : 0 >$,$tune\_ctl$,$vcofreq < 2 : 0 >$.$vcoIbias < 0 >$is used to control bias currents used in VCO.If it is 0 VCO consumes 1mA current. If it is 1 VCO current switches to 1.2mA.$vcoIbias < 1 >$,$vcoIbias < 2 >$ are used to control currents in the voltage buffers used after divide by 2 circuit used in PLL.$vcoIbias < 1 >$,$vcoIbias < 2 >$ low switches the current from 60μA to 80μA.$tune\_ctl$ is made high to monitor the control voltage. $vcofreq < 0 >$ is made high to add additional 50fF capacitance in parallel to the varactor.This will reduce the oscillation frequency of VCO.

- **Register 14**:

  Its data bus consists of $rxdummy < 7 : 5 >$,$rxpd$,$rxgain$,$rxbw < 2 : 0 >$.$rxpd$ low is used to power down the receiver.$rxgain$ is made high to switch the gain of amplifier from 1dB to 15dB.$rxbw < 2 : 0 >$ varies the bandwidth of the receiver filter.

4.3 Programming the control register

There are many ways to programme the control register. We used spartan-3 FPGA boards to programme the memory. The design is implemented using behavioral

modeling .The input and output ports of top level module is shown is fig.4.2

- **Input port**:

  rst—-At positive edge of rst,FPGA starts sending the required data to the corresponding registers. At negative edge of rst,it stops sending data.

  $mclk$—-This the master clock used in the design.All other clocks are derived from it.We used a 50MHz onbaord clock available on spartan-3 FPGA board.

  $dacclk$—-This is used to synchronize the transmit data that is generated by spartan-3 FPGA board with the $dacclk$ used in the chip

- **Output port**:

  $data < 0 : 7 >$—-8-bit data bus.

  $addr < 0 : 3 >$—-4-bit address bus.

  $wclk$—-write clock

  $txdataI < 3 : 0 >, txdataQ < 3 : 0 >$—-These are the $I < 3 : 0 >$ and $Q < 3 : 0 >$ inputs for the DAC used in transmitter.

The verilog module is shown in fig.4.2.The data and address bus have a period of 24.41KHz.We generated $wclk$ in such a fashion that for all the four addresses $wclk$ has a pulse at the center of data and address signals.So by the time write pulse comes,data and address lines are stabilized and then on the rising edge of $wclk$ data is written in the chip.Operation of this module is explained below:

1. First identify the data that needs to be passed to the chip.Then type this data in the verilog code.

2. Then reset the whole system by giving a negative edge of rst.

3. After this,on the positive edge of rst , data and address buses write data on the chip.Now one can reprogramme the chip as many times by using rst switch.

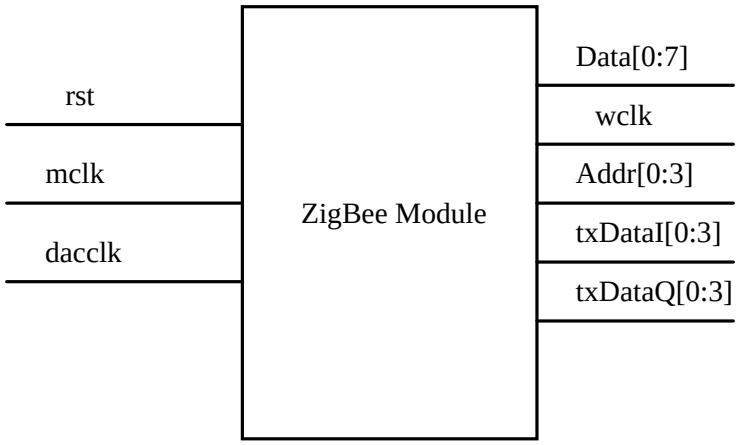

Figure 4.2: Verilog module used for programming control register

Since the output pins of spartan-3 swings from 0V to 3.3V.We used resistive divider network to scale down all the signals to 1.8V.

Timing diagram for the above module is shown in fig.4.3

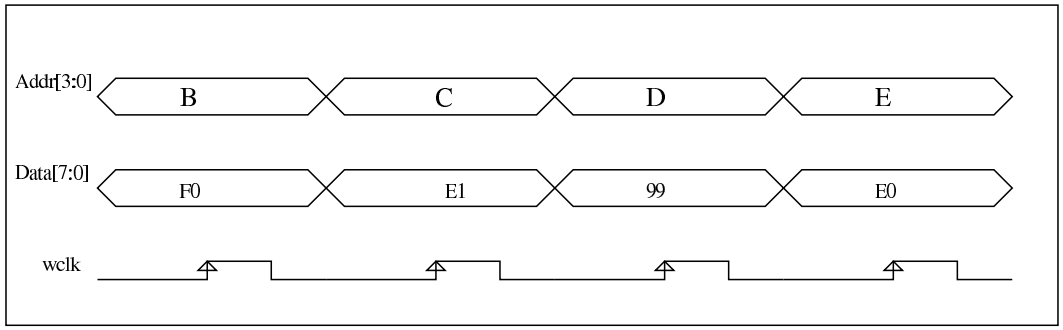

Figure 4.3: Timing diagram

CHAPTER 5

PLL and power amplifier measurements

This section forms the crux of this thesis and deals with the practical testing of frequency synthesizer.It provides a brief description of the architecture used for PLL.After this measurement results of the frequency synthesizer are given.

5.1 Synthesizer architecture

Synthesizer architecture is shown in fig.5.1. Specifications for PLL are shown in table.5.1.

Table 5.1: PLL specifications

Performance metrics	Specifications
Settling time	192us
Accuracy	±40ppm,for a center frequency of 2.5GHz it is ±100KHz
Phase noise	-92dBc/Hz at an offset of 3.5MHz from carrier
Spurs at 5MHz	-20dBc
Spurs at 10MHz	-50dBc

5.1.1 PFD and CP

The schematic is shown in fig.5.2.Standard tri-state PFD architecture was used to design PFD. The operation of the PFD is explained below.The outputs *up* and *dn* can be in any of the four states

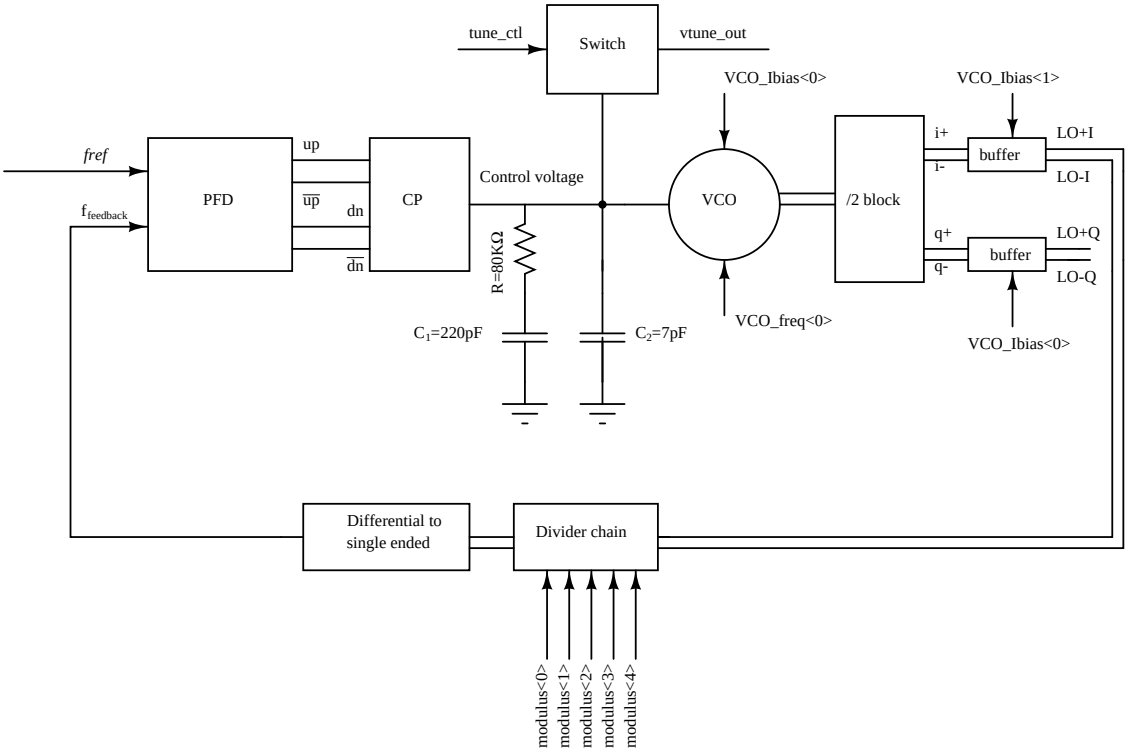

Figure 5.1: Architecture of frequency synthesizer

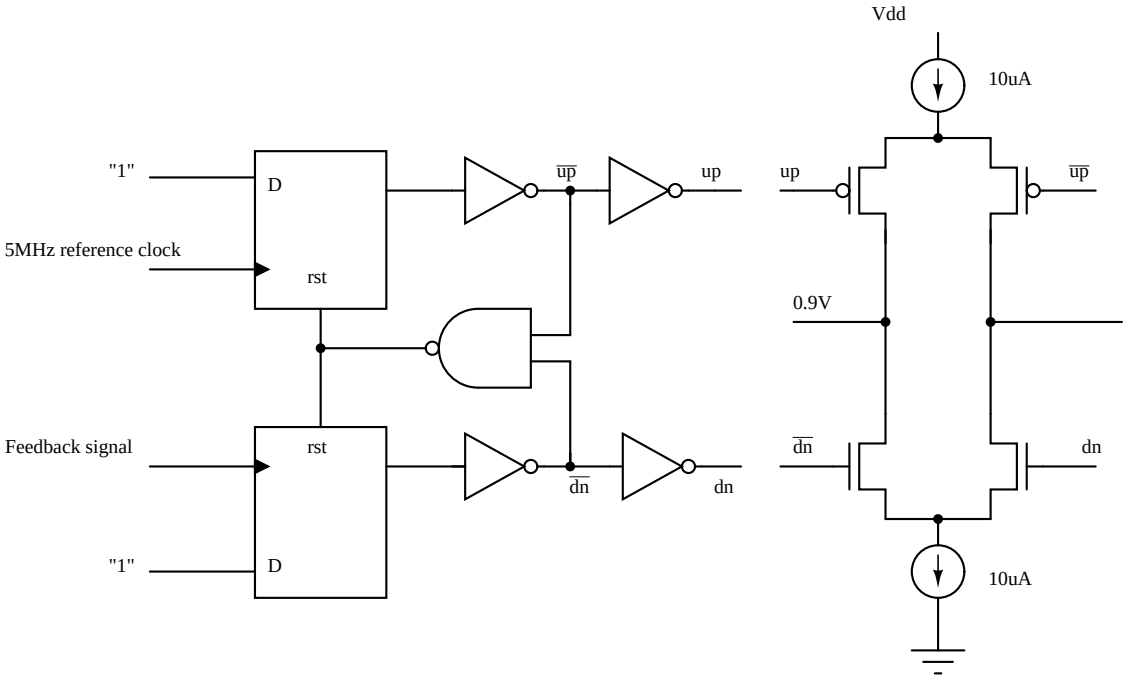

Figure 5.2: PFD and charge pump

- $up = 0, dn = 0$: The output control voltage is in high impedance state.When the PLL is in lock state this is the ideal state that one would expect in theory.But in practice PFD is designed in such a way that control voltage suffers from small ripples at a frequency equal to reference frequecny.This is the reason why output spectrum of PLL shows spurs at multiples of reference frequency.

- $up = 0, dn = 1$:This occurs if frequency of feedback signal is higher than 5MHz reference signal.Under this condition,control voltage decreases and makes VCO to run at a lower frequency.

- $up = 1, dn = 0$:It means reference frequency is higher than feedback signal and control voltage increases to make vco run at a higher frequency.

- $up = 1, dn = 1$:This will never occur because of the reset signal.

5.1.2 Loop filter, VCO and divide by 2 block

The values of R,$C1$ and $C2$ used in the loop filter is shown in fig5.1.Using these values a loop bandwidth of 35KHz is obtained.

VCO is designed using a LC tank and a negative resistance provided by cross - coupled differential pair. Frequency of oscillation is varied by changing the varactor value.To make VCO oscillate at the right frequency,two external control signals,namely $vcoIbias < 0 >$ and $vcofreq < 0 >$ are provided.These values can be set through the control register.$vcoIbias < 0 >$ low switches the tail current of VCO from 1mA to 1.2mA.$vcofreq < 0 >$ high decreases the frequency of oscillation because it adds an additional 50fF capacitor in parallel with the varactor.

A switch is provided at the input of VCO called *tune_ctl*.Make this 1 to monitor the control voltage.VCO output is further divided by two to generate quadrature I and Q components.As explained in [1],since the divider circuit is loaded by mixer and subsequent divider chain,it was taking up a lot of current.Therefore,I and Q signals are passed through buffers. $vcoIbias < 1 >$and $vcobIias < 2 >$ low,switches the current of buffers from 60μA to 80μA.

5.1.3 Programmable divider chain

The divider chain must be programmable from 481 to 496 to switch channels from 2.405GHz to 2.480GHz.The architecture used for this purpose is shown in fig.5.3:

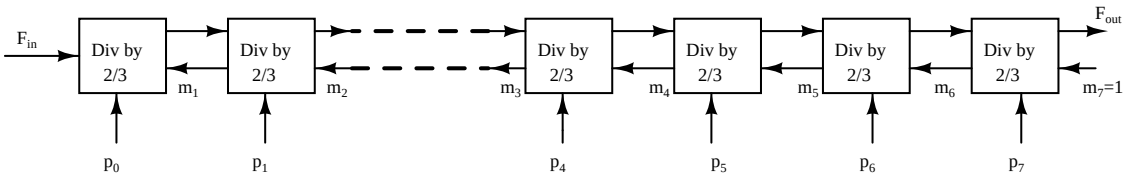

Figure 5.3: Programmable divider chain

Working principle The programming bits control the output frequency. The last cell generates the signal m_7=1.This signal then propagates upwards and divides the input frequency by three if programming input pi is set to 1.Division by 3 will add one more period of each cell's input signal to period of output signal.Since a modulus count of greater than 480 is required.The last three cells of the chain have their programming bits connected to 1.Under these conditions the output frequency

is given by:

$$F_{out} = \frac{F_{in}}{2^8 + 2^7 + 2^6 + 2^5 + 2^4 p_4 + 2^3 p_3 + 2^2 p_2 + 2^1 p_1 + 2^0 p_0} \tag{5.1}$$

Therefore,divider can be programmed from 480 to 511.The programmable bits can be set by programming the $modulus < 0 : 5 >$ bits available in register 12.

5.2 Board description

To test PLL a test board was designed.Orcad software was used to design the PCB.The PCB is manufactured on a copper plate FR-4 dielectric.

Power supply and grounding plane

The performance of the system is hugely affected by power supply noise.For example,control voltage is very sensitive to power supply variations.V_{dd} supply is regulated using TPS7301 power regulator.Before passing supply to chip,it is filtered using parallel bank of surface mount capacitors.A good ground plane is essential for good performance because it helps in minimizing parasitic capacitance.

Reference clock

Spectral purity of PLL output is heavily depends on the reference. Since the PLL loop behaves as low pass ,from reference input to output. Most of the noise from reference is passed to the output. In practice it is necessary to use a crystal with high

accuracy. But for testing purpose we used a 80MHz clock from a signal generator.

Current reference

Due to the unavailability of 5μA reference,we used 100K resistor in place of it. From simulations the drain potential for pmos device was found to be 342mV.The resistance value came out to be 68K for 5μA current. We tested with 68K but we got a drain potential of 420mV.It seems like either V_{th} of pmos has decreased or its mobility has increased. After doing 5 iterations,we found that 100K resistance gives a current of 5μA.

Off chip components

For biasing the output pins of transmitter,10nH inductors are connected from supply to the output pins.SMA connectors are used to feed 80MHz reference clock and tap RF outputs at 2.4GHz.

Some board issues

There seems to be a coupling between control voltage and 16MHz dacclk. While observing control voltage in oscilloscope a waveform was seen with a period of 16MHz.To solve this issue,we cut the trace for dacclk on PCB. After cutting this trace,the coupling was not seen.

5.3 Measurement results

The equipments used for testing are shown in Table.5.3.

The DC bias conditions for the chip are shown in table.5.2

Table 5.2: DC conditions for zigbee chip

Signal	DC value
$txoutn, txoutp$	1.8V
$vrefdac$	0.9V
$envlp\_ref$	1.5V
$vcmref-$	0.15V
vcm	0.9V
$vcmref+$	1.65V

Table 5.3: Equipments used for testing

Equipment used	Purpose
Agilient E4422B signal generator(250KHz-4GHz)	80MHz reference for PLL
HP 8592A spectrum analyzer(50KHz-22GHz)	Output spectrum from power amplifier
GWInstek GDS-840C Digital oscilloscope	Control voltage measurement
GWInstek GDS-4303 4CH DC power supply	Input to the power regulator

5.3.1 Frequency synthesis

The synthesizer is first tested for its basic operation-generation of 16 channel select frequencies. The table.5.5 shows the output frequency observed for each divider ratio ranging from 480-496.We tested in all 8 chips out of which 2 chips seems to work.The data presented below is for chip 4.The reference frequency is set to 80MHz.Other settings for the chip are listed in table.5.4.The supply voltage is 1.8V.During measurements the resolution bandwidth(RBW) is set to 100kHz.All spectrums are observed

single-ended not differentially.

Table 5.4: Chip 4 settings

Signal name	Bit value	Meaning
$txpd$	1	Transmit path is on
$txpower[3:0]$	0000	PA is transmitting maximum power
$vcoIbias[0]$	1	VCO tail current is set to 1mA
$vcoIbbias[2:1]$	00	Buffer currents are set to 80μA
$tune\_ctl$	1	Enable the control voltage monitor
$rxpd, rxgain, rxbw[2:0]$	all 0's	Disable the reciver path

Table 5.5: N vs output frequency data for chip 4 with f_{ref}=80MHz and V_{dd}=1.8V

N_{set}	Output frequency(GHz)	Control voltage(mV)	$N_{measured}$
480	2.39958	52.1	479.916
481	2.39958	52.1	479.916
482	2.40501	145	481.002
483	2.40970	207	481.94
484	2.41448	262	482.896
485	2.41969	306	483.938
486	2.42474	347	484.948
487	2.42969	385	485.938
488	2.43474	422	486.948
489	2.43979	453	487.958
490	2.44484	483	488.968
491	2.44979	514	489.958
492	2.45484	544	490.968
493	2.45989	572	491.978
494	2.46494	603	492.988
495	2.46988	630	493.976
496	2.47494	658	494.988

There is a constant offset of 1 between the divider ratio set through programming and the divider ratio obtained after measurements.Due to this,output frequency is always 5MHz less than what is desired.One reason why this is happening is because reference clock is not exact.Lets say divider is set to 480.Then change in output frequency is given by

$$f_{out} = 480 f_{ref} \tag{5.2}$$

$$\Delta f_{out} = 480 \Delta f_{ref} \tag{5.3}$$

From above equation,if f_{ref} changes by 10KHz.Then output f_{out} changes by 4.8MHz.

We did one more test with chip 4 with reference frequency set to 80.36MHz.The supply voltage is 1.8V.Other settings are the same as shown in table.5.4.The table.5.6 shows the output frequency observed for each divider ratio ranging from 480-496.

Table 5.6: N vs output frequency data for chip 4 with f_{ref}=80.36MHz and V_{dd}=1.8V

N_{set}	Output frequency(GHz)	Control voltage(mV)	$N_{measured}$
480	2.40648	151	479.140
481	2.41159	216	480.157
482	2.41664	271	481.163
483	2.42143	317	482.116
484	2.44264	356	483.106
485	2.43091	392	484.004
486	2.43590	427	484.998
487	2.44088	460	485.989
488	2.44593	492	486.994
489	2.45107	521	488.018
490	2.45599	550	488.998
491	2.46114	580	490.023
492	2.46610	608	491.010
493	2.47106	637	491.998
494	2.47603	665	492.988
495	2.48099	696	493.975
496	2.48595	724	494.963

We increased the supply voltage from 1.8V to 2V to increase the headroom for the transistors in the divider chain.We tested all the chips with 2V.Still only chip 4

was found to work.Table.5.7 shows the output frequency observed for each divider ratio ranging from 480-496.For this test,control voltage became more sensitive.While measurnig control voltage,there were ripples on it as high as 140mV because of the probe capacitance.

Table 5.7: N vs output frequency data for chip 4 with f_{ref}=80MHz and V_{dd}=2V

N_{set}	Output frequency(GHz)	$N_{measured}$
480	2.40670	479.140
481	2.40670	480.157
482	2.40670	481.163
483	2.41008	482.116
484	2.41513	483.106
485	2.42014	484.004
486	2.42509	484.998
487	2.42982	485.989
488	2.43482	486.994
489	2.43983	488.018
490	2.44477	488.998
491	2.45005	490.023
492	2.45506	491.010
493	2.46008	491.998
494	2.46506	492.988
495	2.47015	493.975
496	2.47517	494.963

Fig.5.4 shows the output frequency versus control voltage plot.From these plots K_{VCO} is 164MHz/V.PLL was designed for a K_{VCO} of 140MHz/V.

5.3.2 Phase noise and spurious components

We measured spurs and phase noise for chip 4 under these conditions:

$V_{dd} = 2V, F_{ref} = 80MHz, modulus\ ratio = 480.$

A comparison between the testing results,simulation results and zigbee specifications

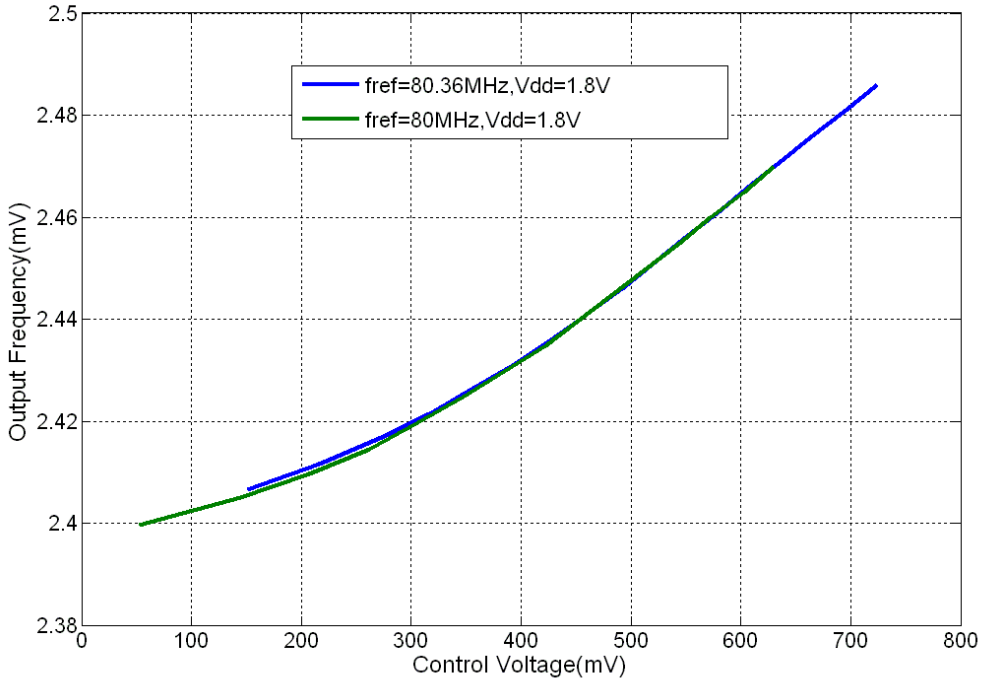

Figure 5.4: VCO characteristics

is shown in table.5.8

Table 5.8: Comparison between phase noise and spurs

Performance metrics	Zigbee specifications	Simulation results	Testing results
Spur at 5MHz	-20dBc	-39dBc	-48dBc
Spur at 10MHz	-50dBc	-50dBc	-56dBc
Phase noise	-92dBc/Hz	-117dBc/Hz	-132dBc/Hz

5.3.3 Output Spectrum

The output spectrum for the above test cases is shown in fig.5.6 and in fig.5.8

From above graphs,we can see the reference spurs which proves that the synthesizer is in locked state.

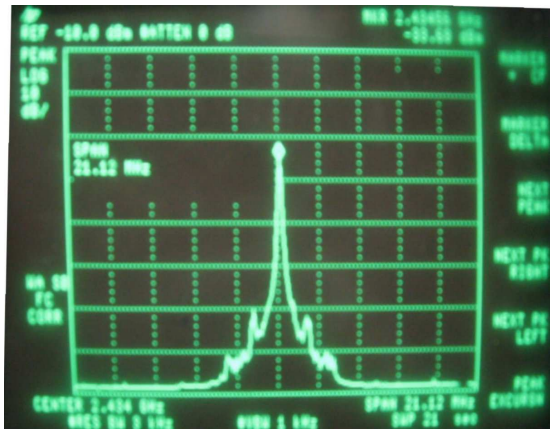

Figure 5.5: f_{ref}=80MHz,V_{dd}=1.8V,N=487

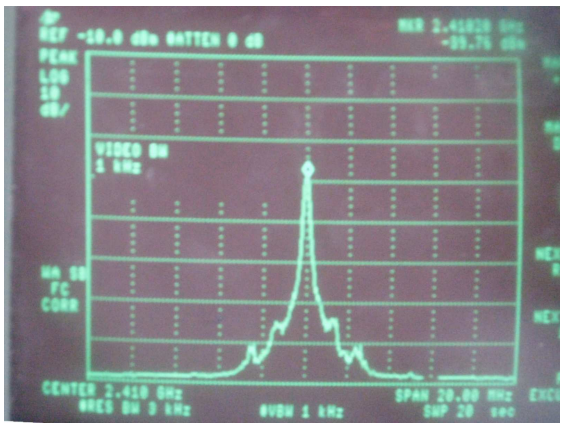

Figure 5.6: f_{ref}=80.36MHz,V_{dd}=1.8V,N=480

Fig.5.8 shows a zoomed in version of the spectrum.A reference spur at 5MHz is

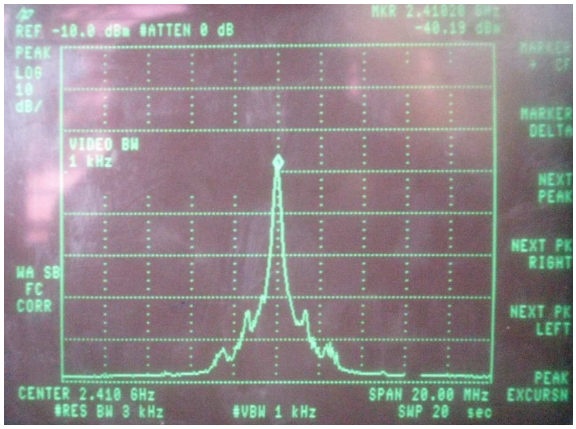

Figure 5.7: f_{ref}=80MHz,V_{dd}=2V,N=482

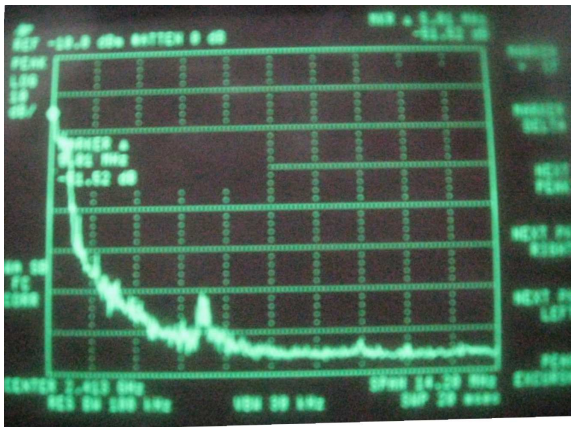

Figure 5.8: f_{ref}=80MHz,V_{dd}=2V,N=480

seen which suggests that PLL is in lock state.

5.4 Power amplifier

5.4.1 Architecture

A class AB differential power amplifier is used here.Its half schematic is shown in fig.5.9.Therefore,to activate a particular branch $txpower<i>$ should be low.

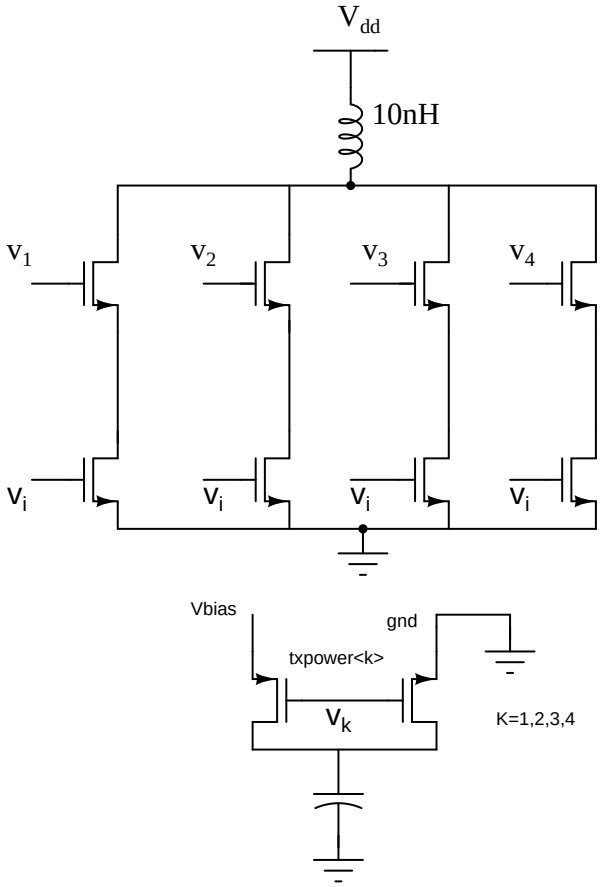

Figure 5.9: PA half-circuit schematic

5.4.2 Power amplifier measurements

We measured the power amplifier output against variations in txpower[3:0] pins for chip 4.The measured values are shown in table.5.9.For this experiment f_{ref}=80MHz,N = 494 and V_{dd}=1.8V was chosen.The noise floor was at -86dbm.

Table 5.9: Power amplifier readings with V_{dd}=1.8V

txpower[3:0]	Power amplifier output(in dbm)
0000	-19.44
0001	-20.11
0010	-20.65
0011	-21.37
0100	-21.92
0101	-22.8
0110	-23.88
0111	-24.58
1000	-25.6
1001	-26.9
1010	-28.6
1011	-30.25
1100	-32.29
1101	-35
1110	-41
1111	-52

We changed the supply from 1.8V to 2V and again measured the output power against $txpower[3:0]$ bits.The measured values are shown in table.5.10.Other settings are the same as for 1.8V.

5.5 Problems encountered with other chips

In all other chips except chip 8,control voltage was not able to settle to a particular value.PLL was not able to synthesize properly.We tried to make control voltage

Table 5.10: Power amplifier readings with V_{dd}=2V

$txpower[3:0]$	Power amplifier output(in dbm)
0000	-19.66
0001	-20.2
0010	-20.92
0011	-21.56
0100	-22.22
0101	-23.07
0110	-23.82
0111	-26
1000	-26
1001	-27.26
1010	-28.82
1011	-30.52
1100	-32.7
1101	-35.76
1110	-41.63
1111	-53.6

settle by changing reference frequency but control voltage either saturates to lower rail or higher rail.We switched off the control voltage monitor and again tested all chips,still PLL was not able to synthesize.

CHAPTER 6

Layout

6.1 Board layout

Layout for antenna and PCB are shown in fig.6.1and fig.6.2

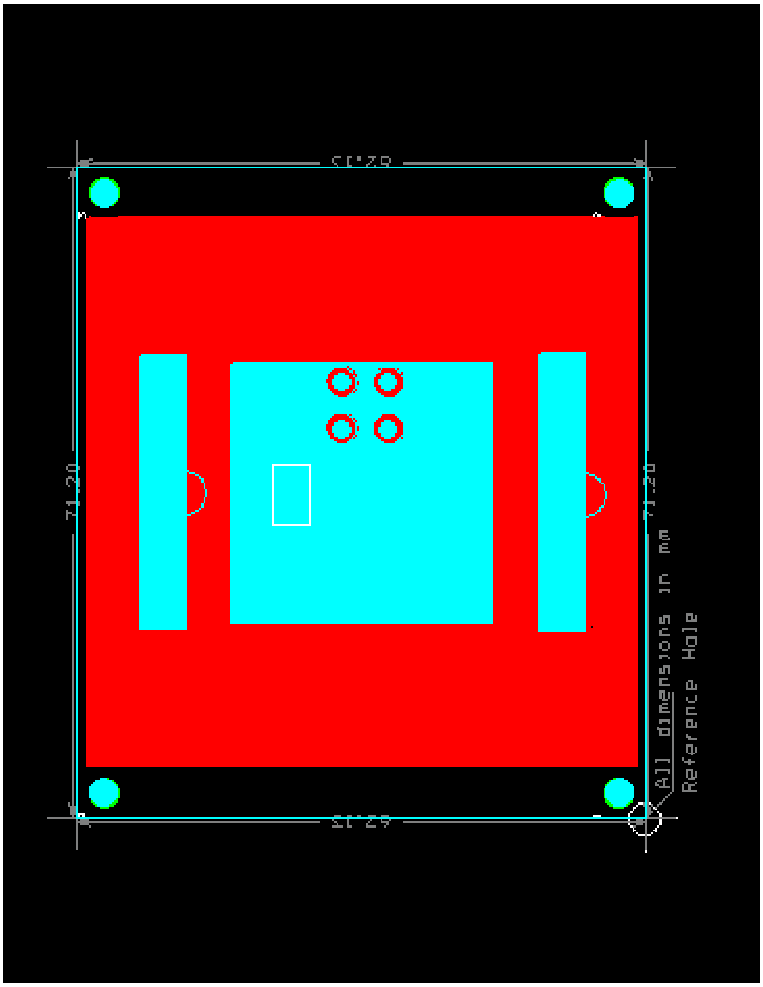

Figure 6.1: Layout for antenna

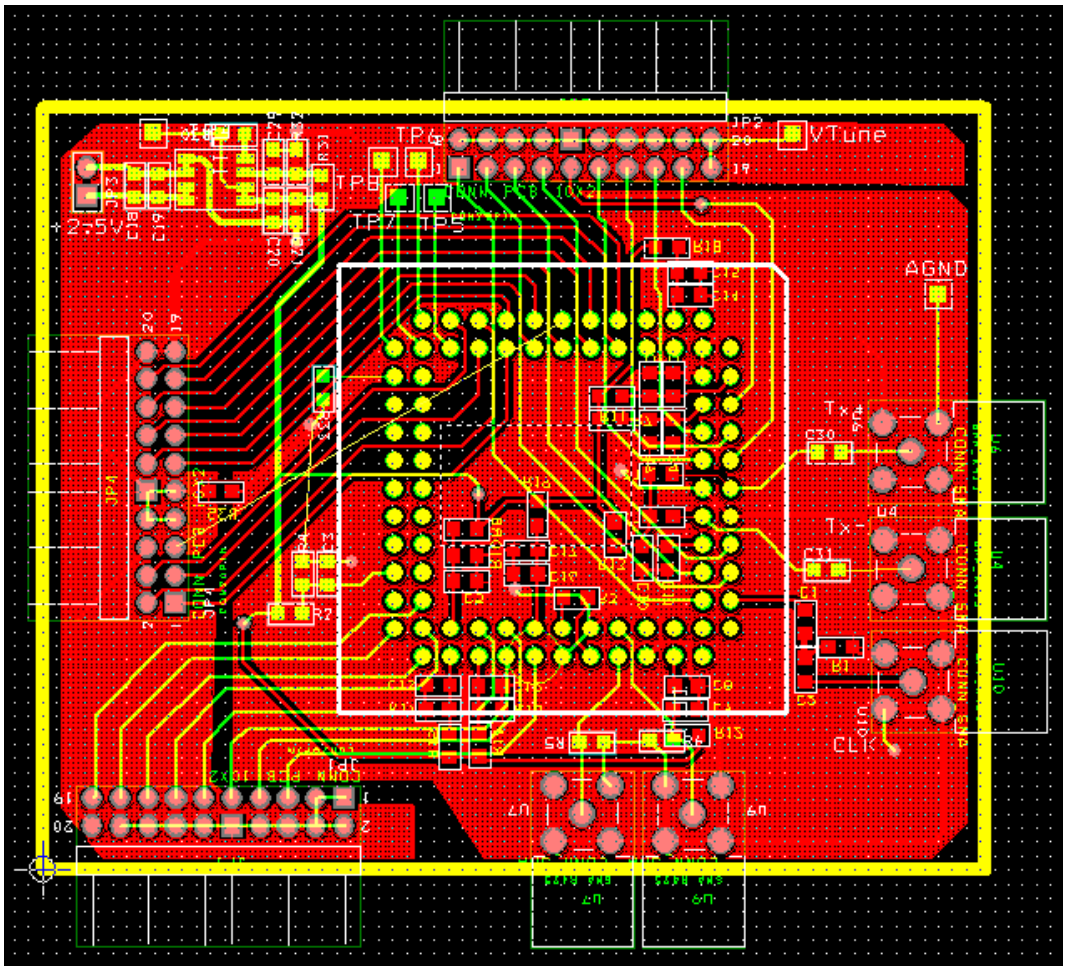

Figure 6.2: Layout for board

CHAPTER 7

Conclusions

An NEGCOMA antenna is implemented for zigbee standard.The antenna is tested with the help of VNA.An impedance bandwidth of 175MHz from 2385MHz-2560MHz is obtained which is good enough for zigbee band(2405MHz-2480MHz).

We tested 8 chips.Only chip 4 and chip 2 are working.PLL in Chip 4 is working fine.By changing $txpower[3:0]$ pins,the magnitude of output power does change.With change in $txdataI[3:0]$ and $txdataQ[3:0]$,output power changes.From above we can say that mixer,PLL and PA in the transmitter chain are working.

In other chips,control voltage does not settle to a particular value.We changed the reference frequency from 70MHz-90MHz,control voltage either saturates to lower rail or higher rail.With change in N,control voltage does not change for these chips.

Transmitter has to be tested with a MSK(minimum shift keying) modulated data to observe its spectrum and checking whether it satisfies the transmit mask specified by zigbee.A setup is to be made to measure the settling time for frequency synthesizer.

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