16 bit Audio band Digital-to-Analog Converter

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled 16-bit Audio-band Digital-to-Analog Converter, submitted by **HARI PRASATH V**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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If I have seen further it is by standing on ye shoulders of Giants – Sir Isaac Newton.

I would like to thank my professor Dr. Nagendra Krishnapura for his guidance throughout my fourth and fifth year at IIT-Madras. He was not only my guide but also an advisor and a friend. I consider myself fortunate to have worked under his guidance. His eye for detail, patientce, meticulous nature, devotion to work are always a source of inspiration for me. I have been introduced to the analog world through various courses and interactions with Dr. Nagendra and Dr. Shanthi Pavan. All the analog courses which encompassed many the analog designs were stimulating. The course lectures were highly informative and interactive with a lot of emphasis on intuitive understanding and ideas. The design level assignments were of a great test of understanding and exploring different design issues. Apart from the coursework, I have learnt a great deal about hobby radio electronics from Dr. Nagendra Krishnapura.

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I cannot thank enough to my parents and maternal uncle for their constant support, understanding and help.

ABSTRACT

A 16bit R-2R ladder based audio band digital-to-analog converter is presented. The R-2R ladder architecture was chosen for minimizing the flicker noise contribution to the output. However, the matching between the resistors is acceptable only for 10bit D/A converter. Therefore, a calibration technique is employed to imporve the mismatch performance in the ladder. Differential R-2R ladder current sources was provide larger SNR and maintain the common-mode of the operational amplifier at 0.9V.

The I-V conversion of the resistor ladder digital-to-analog converter has to be highly linear. The overall design should have a low power consumption. With the reduction in supply voltage and device sizes, many architectures which were feasible in higher supply voltage cannot be used in low supply voltages. Different operational amplifier architectures are examined to obtain the required specification for the D/A Converter.

The I-V conversion is performed by a three stage class AB operational amplifier. Different operational amplifier architectures have been considered for the design. A three stage operational amplifier with following specification has been designed in 0.18μm UMC CMOS 6 metal layer technology. The specifications of the three stage amplifier are as follows. 100dB DC gain, 1.75MHz UGB, 1V/μs Slew rate, -100dB distortion, 2.1μV integrated noise (20Hz-20kHz), 1.6V peak-peak output swing, THD @ 1 kHz full scale input of -96.66 dB, C_{m1}=50 pF, C_{m2} = 1 pF, Area of 239 μm $\times$ 297 μm and power consumption of 340 μW. The integrated noise generated by the voltage reference generator is 22 μV(20 Hz - 20 kHz). The layout of reference generator, operational amplifier, ladder and auxillary ladder occupy an area of 515 μ m $\times$ 419 μ m. Further to reduce compensation

capacitance which in turn reduces area constraint, a current multiplier technique was investigated.

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LIST OF FIGURES

ABBREVIATIONS

MC	Miller Compensation
SMC	Single Miller Compensation
MCNR	Miller Compensation Nulling Resistor
MCFF	Miller Compensation Feedforward
NMC	Nested Miller Compensation
NMCNR	Nested Miller Compensation Nulling Resistor
NMCFF	Nested Miller Compensation Feedforward
DFCFC	Damping Factor Control Frequency Compensation
PM	Phase Margin
GBW	Gain Bandwidth
UGB	Unity Gain Bandwidth
UGF	Unity Gain Frequency

CHAPTER 1

Introduction

The design of 16bit audio band D/A converter is discussed in this thesis. The audio band extends from 20Hz to 22kHz. The Nyquist sampling frequency is 44.1kHz. Apart from Nyquist rate converters, oversampling converters can also be used because of low sampling frequency.

Oversampling sigma-delta architectures are preferred for such low-speed, high dynamic range applications because of their immunity to matching and precision of the components used. The matching and precision required for the components can be orders of magnitude less when compared to Nyquist rate D/A Converters. However the sigma-delta architectures suffer from out of band noise and stability issues.

Nyquist rate architectures can be used for low-speed, high dynamic range application. In modern VLSI fabrication process the matching between components and precision is less. The matching between different components can be anywhere between 1% to 0.1%. This is not acceptable for a converter with 16-bit resolution. Hence calibration techniques have to be utilized to achieve 16-bit performance. Current-steering D/A converters with 16-bit performance have been realized [5] in CMOS. However, current steering D/A converters suffer from flicker noise contribution from MOS transistor current sources. The flicker noise frequency corner for MOS transistors can be as high as 1kHz. The flicker noise can be reduced by circuit optimization.

The resistor ladder can be used as current source instead of MOS transistor current sources. The resistors contribute only thermal noise to the converter. This eliminates the flicker noise contribution from the current sources. However, matching between resistors is 0.1%. Therefore calibration technique has to employed to achieve 16-bit resolution.

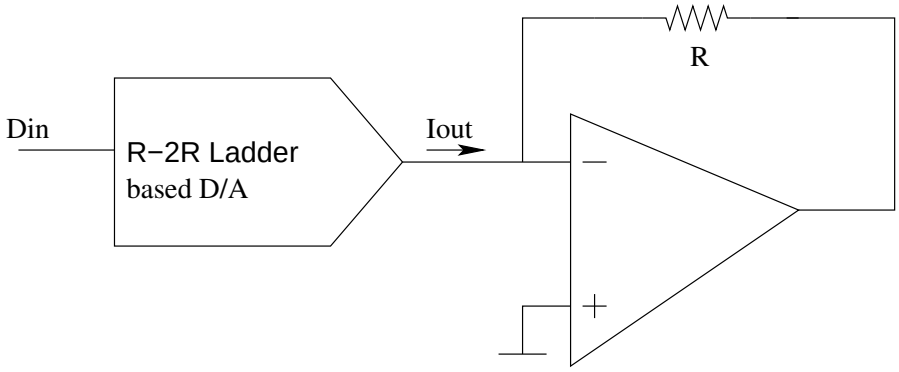


Figure 1.1: R-2R Ladder Generic Architecture

The Current to Voltage converter in the D/A converter has to be highly linear without adding noise. Different operational amplifier architectures are examined to obtain the required specification for the D/A Converter.

Multi-stage amplifiers are needed with the advance in technologies, due to the fact that single-stage cascode amplifier is no longer suitable in low-voltage designs. The reduction of the power supply and the need for a rail-to-rail swing has given rise to multi-stage amplifiers. The short-channel effect of the submicron CMOS transistor causes the output-impedance degradation and hence the amplifier gain is reduced dramatically. Multi-stage amplifiers require frequency compensation techniques to build a stable amplifier with good phase margin. Several other design constraints such as noise performance, power consumption, area, distortion, output swing, slew rate, load variations are considered for the design of multi-stage amplifiers.

Chapter2 discusses different R-2R architectures and their performance.

Chapter3 and 4 discusses opamp architectures, requirements and design of a 3 stage class AB opamp.

Chapter 5 discusses D/A simulation results and layout.

Conlusion and future work are presented in Chapter 6.

CHAPTER 2

System Level Design

The Audio Digital-to-Analog Converter has the following specifications.

Sample Frequency	6.144 MHz
Load	1 kΩ,100 pF
Distortion	<-80 dB
Idle Channel Noise	5μV
Offset	5 mV
Power	$< 2\ mV$

2.1 Opamp Specification

From Appendix A.4, the DC-Gain required for the opamp is greater than 100dB. The Bandwidth required

$$\omega_u = 2f_s ln\left(\frac{LSBf_s}{4A\pi f_{in}}\right)$$

As we can see that the bandwidth required is higher for a system with over-sampling because of the opamp settling time requirement.

The Operational Amplifier bandwidth was fixed at 1.75 MHz for a inband SNDR of 90 dB. This was obtained from simulation of a system level R-2R Ladder with macro-model for the opamp.

The integrated output noise (20 Hz - 20 kHz) is 5 μV. Especially at low frequencies, the major noise contribution is from the MOSFET flicker noise. Hence the optimization strategy is to reduce the flicker noise contribution to the integrated noise output.

2.2 R-2R Ladder Structures

The conventional R-2R ladder structure is shown in figure (2.1). As we can observe from the figure, the output voltage range is between 0 and V_{ref}. The reference voltage is 1.5 V in our application. Hence with a single ended supply of 1.8 V the output voltage and an input common mode voltage of 0.9 V, the output voltage range is from 0.9 V to -0.5 V. Therefore, this ladder architecture is not suitable for our application with single ended power supply. The opamp output stage can accomodate a maximum swing of 1.6 V (0.1 V to 1.7 V) in a singled ended supply of 1.8 V.

The conventional architecture can be modified with a current source whose value is equal -$V_{Ref}/2R$ to produce a dc offset of 0.7 V as shown in the figure(2.2). With this modification the output voltage range is from 0.2 V to 1.6 V. The current source can be implemented using MOSFET. But the current source implemented using MOSFET will add flicker noise to the output. Further, the single ended architectures described will not suppress the even harmonics generated. To supress even harmonics and to work with single ended supply, differential architecture for ladder is used. The differential ladder structure with complementary controls is shown in the figure (2.3).

2.3 Switch-Sizing

MOS transistors are used as control switches. The common mode voltage of 0.9 V is used. To obtain a relatively small value of small signal resistance for a given size, a boosted supply voltage of 2.7 V was used. The ladder resistor was fixed at 20 kΩ to meet distortion and noise specification. The resistor value and MOS switch sizes were fixed through simulations. The MOS switches were sized for a small signal ON resistance of 3.6 Ω. In the ladder, we get binary weighted current in each arm. To maintain, constant voltage drop across the switch, the switch sizes were progressively decreased from MSB. The switch sizes are tabulated.

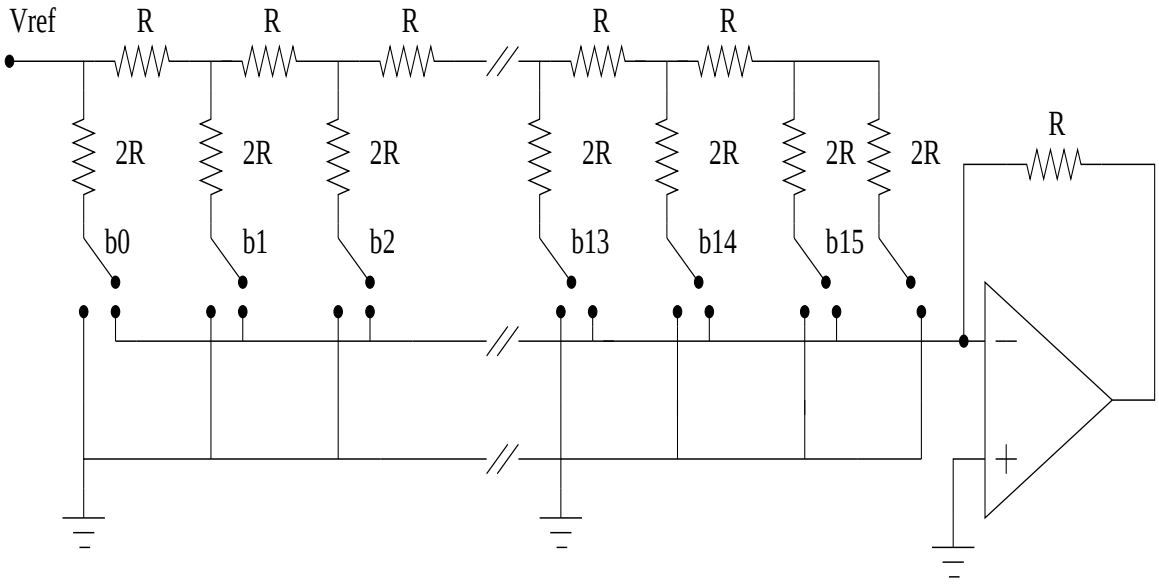


Figure 2.1: R-2R Ladder Conventional Architecture

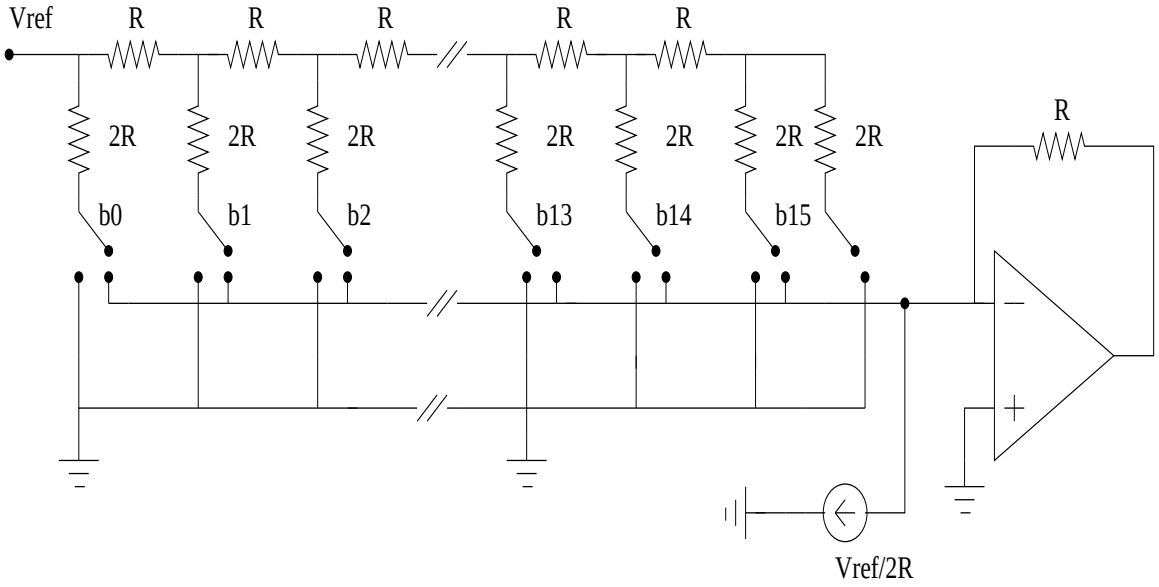


Figure 2.2: R-2R Ladder Architecture with DC offset

Control Bit	Switch Size
MSB	$\frac{128\mu}{0.18\mu}$
MSB-1	$\frac{64\mu}{0.18\mu}$
MSB-2	$\frac{32\mu}{0.18\mu}$
MSB-3	$\frac{16\mu}{0.18\mu}$
MSB-4	$\frac{8\mu}{0.18\mu}$
MSB-5	$\frac{4\mu}{0.18\mu}$
MSB-6	$\frac{2\mu}{0.18\mu}$
MSB-7 to LSB	$\frac{2\mu}{0.18\mu}$

Table 2.1: Ladder Switch Sizes

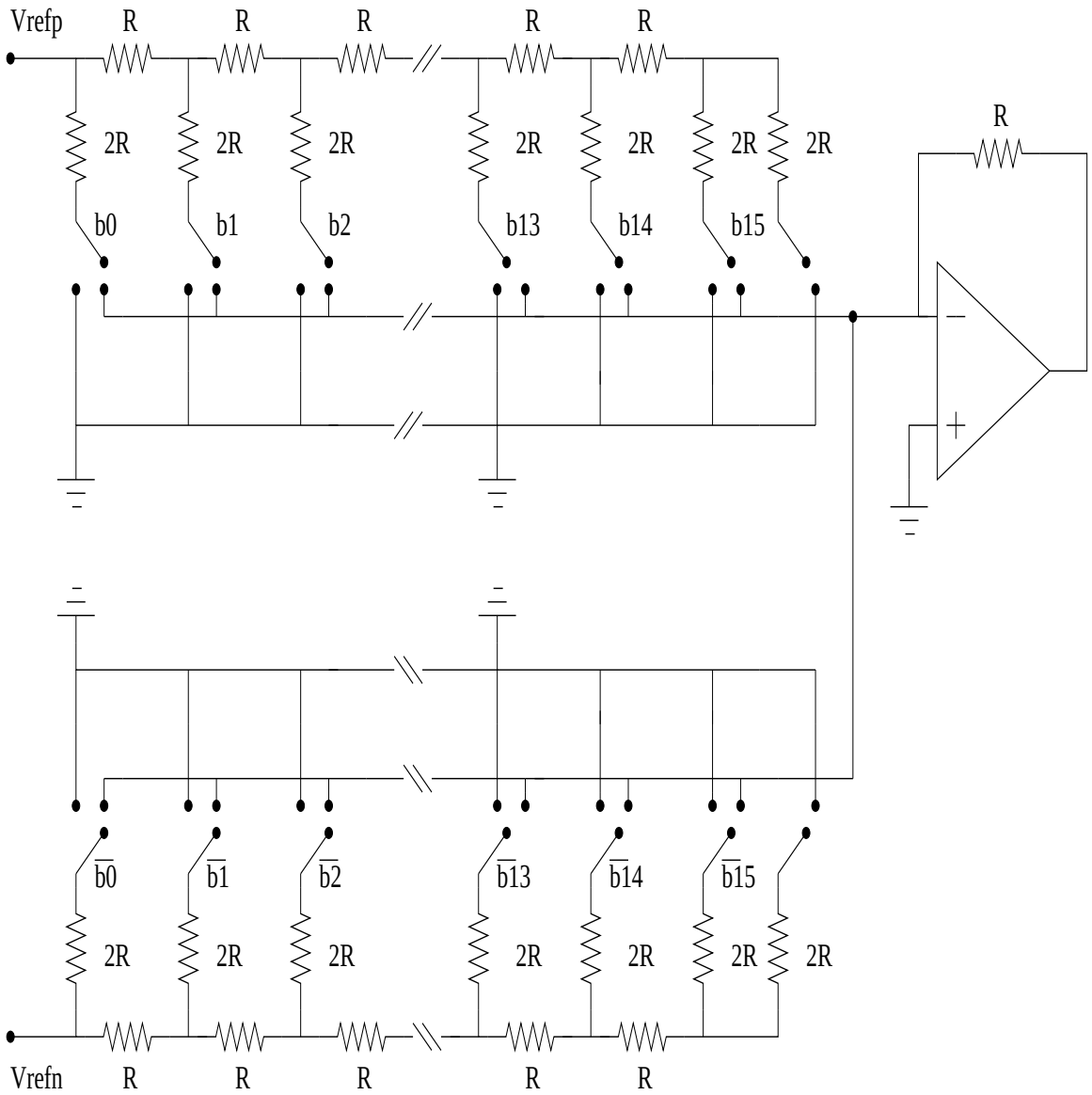


Figure 2.3: R-2R Ladder Differential Architecture

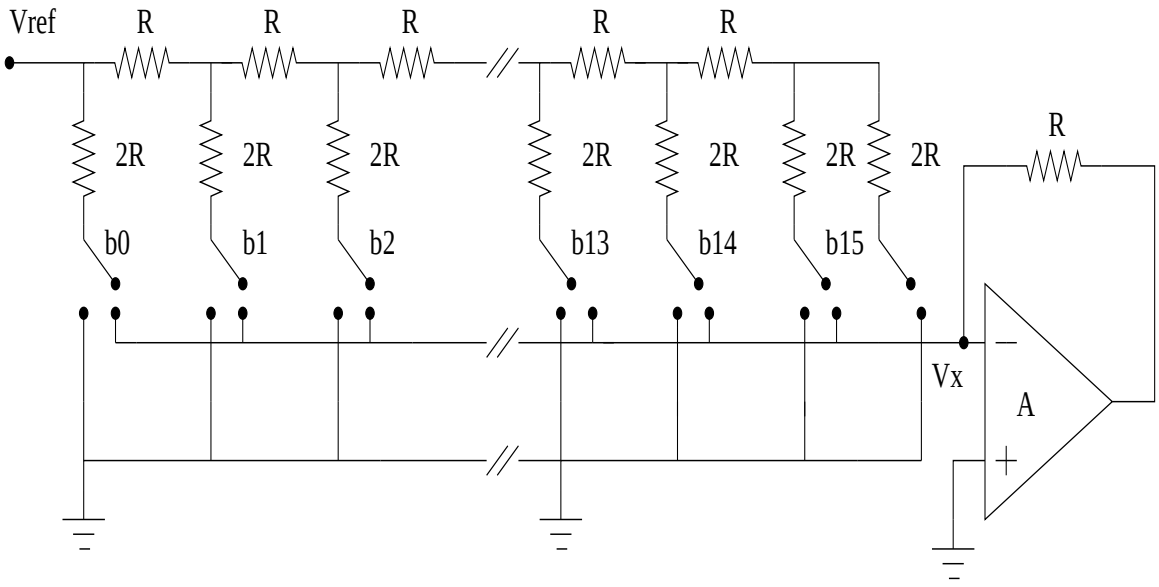


Figure 2.4: R-2R Ladder with Finite Opamp-Gain

2.4 Distortion

The differential ladder rejects even harmonics, with a ideal I-V converter. However the non-ideal I-V converter does not suppress the even harmonics. Consider a single-ended ladder to derive the input dependent variation of the virtual ground. The opamp has finite DC-gain. The virtual ground V_x is at

$$V_x = \frac{V_{ref} D_{in}}{A + D_{in} + 1} \tag{2.1}$$

$$V_{out} = -\frac{V_{ref} D_{in}}{1 + \frac{D_{in}}{A} + \frac{1}{A}} \tag{2.2}$$

As DC-gain (A) tends to infinity, the V_{out} tends to ideal converter. The important inference from the above is the following. Assuming that the differential ladder rejects all even harmonics, the output contains only odd-harmonics. From the expression for V_x(2.2), we see that the virtual ground will have odd-harmonics. The current through the ladder is dependent on the difference $(V_{ref} - V_x)$ times the input code. This will result in producing all harmonics at the output. Thus the output is expected to have all possible harmonics even though we are using a differential ladder.

2.5 Poly-Silicon Resistor Matching

The ladder resistance is 20k Ω. The high-resistance are fabricated using High Resistance Poly-Silicon Resistors.

The resistance model for a given length L and width W is given by the following expression

$$R = 2 \times \frac{R_{contact}}{W + dW} + R_{sheet} \times \frac{L + dL}{W + dW} \left(1 + \alpha(V_1 - V_2) + \beta(V_1 - V_2)^2\right) \quad (2.3)$$

where α, β have appropriate units. dW, dL model the process variations during fabrication. dL=±0.25×L, dW=±0.25×W for maximum and minimum variations.

The Ladder should have the vertical resistor 2R (2×R) matched with the horizontal resistor R. The vertical resistor should be twice as much as horizontal resistor. If we use 2R resistors which are twice as long as the R resistors, the contact resistance is not replicated. Further the difference in voltage $V_1 - V_2$ levels for the resistors gives rise to more mismatches. The variation of the resistor with voltage cannot be fixed because of the different voltage levels in the ladder. However, matching between the horizontal and vertical resistor can be improved by replicating the horizontal resistor twice to capture the contact resistance variation.

2.6 Clock Generation

The non-overlapping clock generation can be obtained using a SR-Latch. The Non-Overlap period can be controlled by the delay of the inverters. The SR-Latch with delay inverters is shown in the figure(2.5). Simulations were performed with trise, tfall set to 1 ns and tdelay as 1ns. This gives rise to 3.5 ns non-overlap period between the clocks. Overlap clock simulations were performed with crossing in the middle.

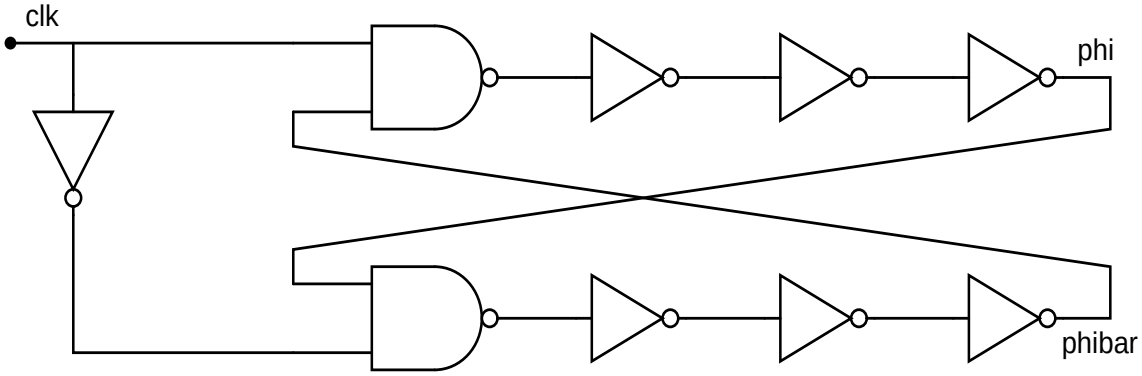
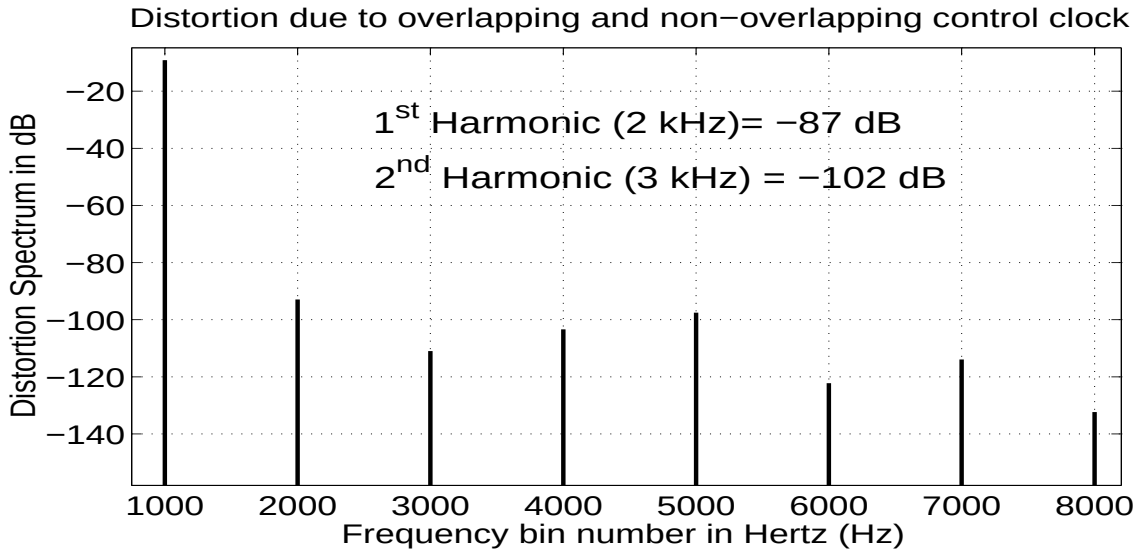


Figure 2.5: Non-Overlap Clock Generator



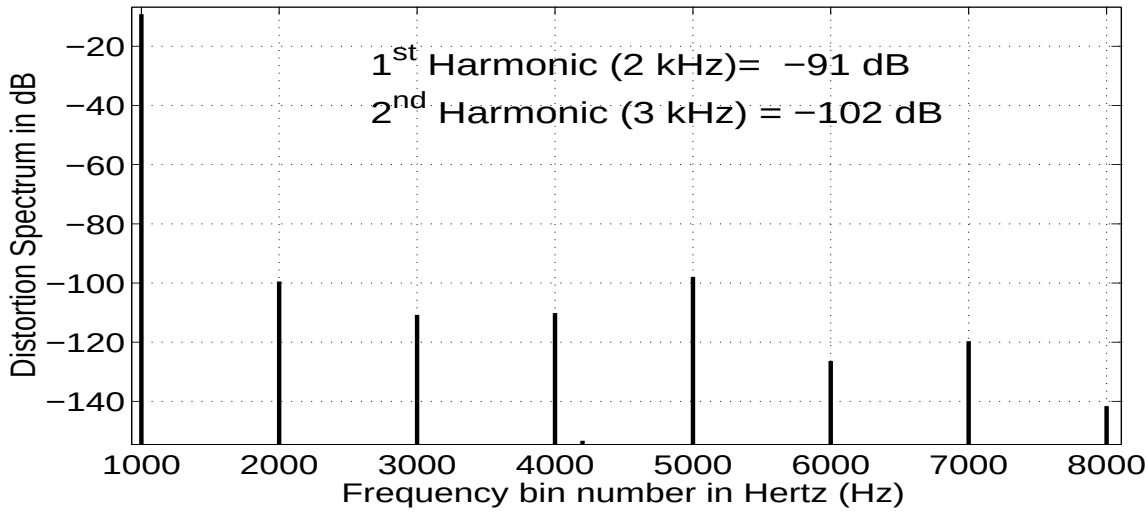


Figure 2.6: Distortion Spectrum of R-2R Ladder, Overlap and Non-Overlap Clocks,$f_{in} = \frac{5}{4096} fs$, fs = 819.2kHz, filtered by 10th Order Butterworth 100kHz cutoff

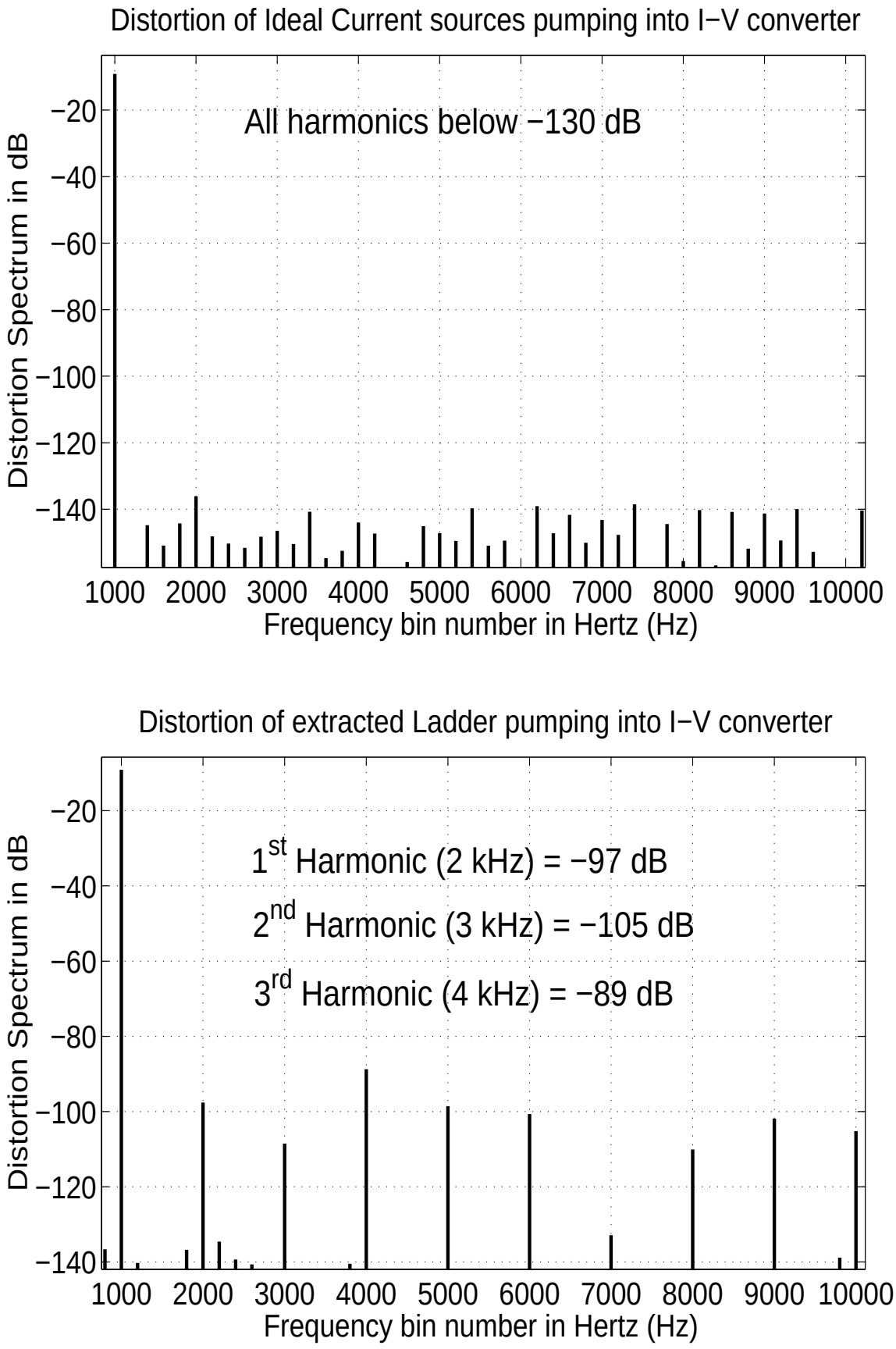


Figure 2.7: Ideal Current Sources and extracted ladder simulation with non-overlapping clock of 2 ns

CHAPTER 3

Opamp Architectures

In this chapter, we analyze various two-stage architectures [3],[2] and three-stage architectures [6],[7],[8],[9],[1],[10],[11]. Through the analysis of two-stage and three-stage architectures, different compensation techniques are re-visited. This chapter mainly concentrates on macro-model small signal analysis with specified approximations.

3.1 Two Stage Amplifier

The Two-Stage architectures are shown in the following figure.

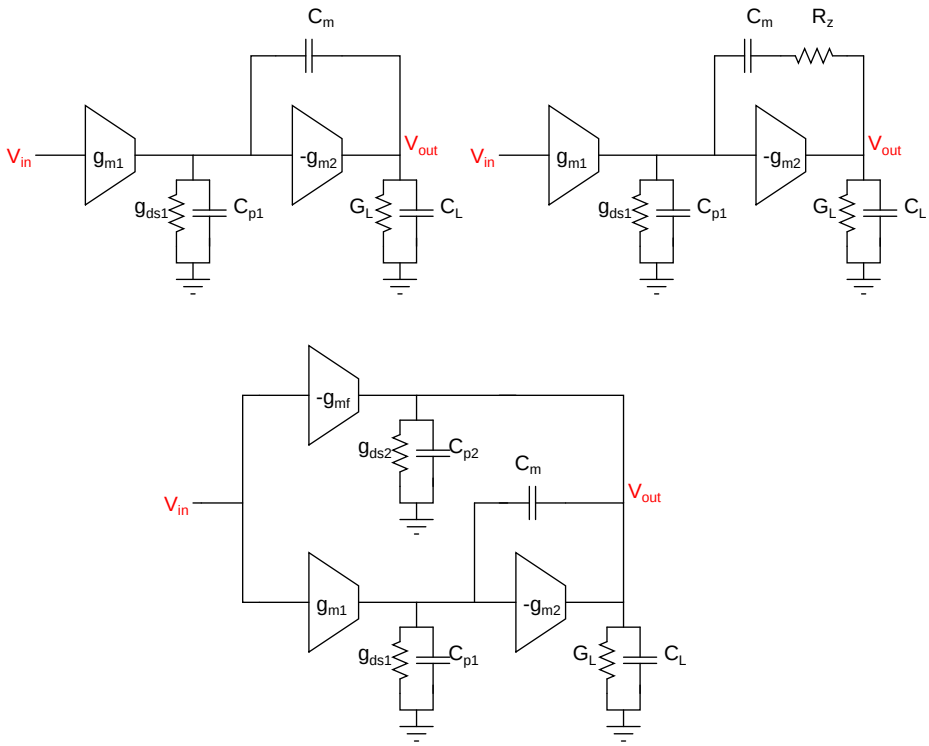


Figure 3.1: Two Stage Amplifier [3], [1], [4]

3.1.1 Miller Compensated Two Stage Amplifier - MC

From the macro-model of two-stage opamp figure 3.1, the following equations are derived.

$$\begin{bmatrix} g_{ds1} + s(C_{p1} + C_m) & -sC_m \\ g_{m2} & G_L + sC_L \end{bmatrix} . \begin{bmatrix} v_x \\ v_o \end{bmatrix} = \begin{bmatrix} g_{m1} v_{in} \\ 0 \end{bmatrix} \tag{3.1}$$

$$\frac{v_o}{v_{in}} = \frac{-g_{m1} g_{m2} (1 - s\frac{C_m}{g_{m2}})}{g_{ds1} G_L (s^2 \frac{C_m C_L}{g_{ds1} G_L} + s\frac{C_m (g_{m2} + G_L)}{g_{ds1} G_L} + 1)} \tag{3.2}$$

Using the quadratic approximation from appendix(A.1), the poles and zeroes are

$$p_1 = -\frac{g_{ds1} g_{ds2}}{g_{m2} C_m} \tag{3.3}$$

$$p_2 = -\frac{g_{m2} + G_L}{C_L} \tag{3.4}$$

$$z_1 = \frac{g_{m2}}{C_m} \tag{3.5}$$

The compensation strategy is to place p_2 at twice the GBW of the amplifier to get good PM.

3.1.2 Miller Compensated with zero Nulling Resistor two stage amplifier - MCNR

From the macro-model of two-stage opamp figure 3.1, [1] the following equations are derived [12],[3],[2].

$$\begin{bmatrix} (g_{ds1} + sC_{p1})(1 + sC_m R_z) + sC_m & sC_m \\ g_{m2} + sC_m(g_{m2} R_z - 1) & (G_L + sC_L)(1 + sC_m R_z) + sC_m \end{bmatrix} \begin{bmatrix} v_x \\ v_o \end{bmatrix} = \begin{bmatrix} g_{m1}(1 + sC_m R_z) v_{in} \\ 0 \end{bmatrix}$$

$$\frac{v_o}{v_{in}} = \frac{-g_{m1}g_{m2}(1 + sC_m(R_z - \frac{1}{g_{m2}}))}{g_{ds1}G_L\left(s^2\frac{C_m(C_L+g_{m2}R_zC_m)}{g_{ds1}G_L} + s\frac{(G_L+g_{m2})}{(C_L+g_{m2}R_zC_m)g_{ds1}G_L} + 1\right)} \tag{3.6}$$

Using the quadratic approximation from appendix(A.1), the poles and zeroes are

$$p_1 \approx -\frac{g_{ds1}g_{ds2}}{g_{m2}C_m} \tag{3.7}$$

$$p_2 \approx -\frac{g_{m2} + G_L}{C_L + C_m g_{m2} R_z} \tag{3.8}$$

$$p_3 \approx -\frac{1}{R_z C_{p1}} \tag{3.9}$$

$$z_1 = \frac{1}{C_m(R_z - \frac{1}{g_{m2}})} \tag{3.10}$$

3.1.3 Miller Compensated two stage amplifier with Feed-Forward - MCF, [1], [2]

$$\begin{bmatrix} g_{ds1} + s(C_{p1} + C_m) & -sC_m \\ g_{m2} - sC_m & G_L + s(C_m + C_L) \end{bmatrix} . \begin{bmatrix} v_x \\ v_o \end{bmatrix} = \begin{bmatrix} g_{m1} \\ g_{mf} \end{bmatrix} .v_{in} \tag{3.11}$$

$$\frac{v_o}{v_{in}} = \frac{-g_{m1}g_{m2}(1 + s\frac{C_m(g_{mf1}-g_{m1})}{g_{m1}g_{m2}})}{g_{ds1}G_L\left(s^2\frac{C_mC_L}{g_{ds1}G_L} + s\frac{C_m(g_{m2}+G_L)}{g_{ds1}G_L} + 1\right)} \tag{3.12}$$

Using the quadratic approximation from appendix(A.1), the poles and zeroes are

$$p_1 = -\frac{g_{ds1}g_{ds2}}{g_{m2}C_m} \tag{3.13}$$

$$p_2 = -\frac{g_{m2}}{C_L} \tag{3.14}$$

$$z_1 = \frac{g_{m2}}{C_m(\frac{g_{mf1}}{g_{m1}} - 1)} \tag{3.15}$$

The compensation strategy is to place $p_2 = z_1$ to get good PM.

$$\gamma = \frac{g_{mf1}}{g_{m1}} \tag{3.16}$$

$$p_2 = z_1 \tag{3.17}$$

$$Cm = \frac{C_L}{\gamma_g - 1} \tag{3.18}$$

3.2 Comparison of Poles and Zeroes

Poles	Miller Compensated(MC)	MC-Nulling Resistor	MCFeedForward
p_1	$-\frac{g_{ds1}g_{ds2}}{g_{m2}C_m}$	$-\frac{g_{ds1}g_{ds2}}{g_{m2}C_m}$	$-\frac{g_{ds1}g_{ds2}}{g_{m2}C_m}$
p_2	$-\frac{g_{m2}+G_L}{C_L}$	$-\frac{g_{m2}+G_L}{C_L+C_m g_{m2} R_z}$	$-\frac{g_{m2}+G_L}{C_L}$
p_3	-	$-\frac{1}{R_z C_{p1}}$	-
Zeros	$\frac{g_{m2}}{C_m}$	$\frac{1}{C_m(R_z-\frac{1}{g_{m2}})}$	$\frac{g_{m2}}{C_m(\frac{g_{mf}}{g_{m1}}-1)}$

Topology	DC Gain	Stability Conditions	GBW	PM
MC	$\frac{g_{m1}g_{m2}}{g_{ds1}G_L}$	$C_m = \frac{2g_{m1}}{g_{m2}}C_L$	$\frac{g_{m2}}{2C_L}$	90-$tan^{-1}(\frac{g_{m1}C_L}{g_{m2}C_m}) - tan^{-1}(\frac{g_{m1}}{g_{m2}})$
MCNR	$\frac{g_{m1}g_{m2}}{g_{ds1}G_L}$	$C_m = \frac{2g_{m1}}{g_{m2}}C_L$	$\frac{g_{m2}}{2C_L}$	90-$tan^{-1}(\frac{g_{m1}C_L}{g_{m2}C_m})$
MCF1	$\frac{g_{m1}g_{m2}}{g_{ds1}G_L}$	$C_m = \frac{2g_{m1}}{g_{m2}}C_L, g_{mf} = g_{m1}$	$\frac{g_{m2}}{2C_L}$	90-$tan^{-1}(\frac{g_{m1}C_L}{g_{m2}C_m})$
MCF2	$\frac{g_{m1}g_{m2}}{g_{ds1}G_L}$	$C_m = \frac{2}{\frac{g_{mf}}{g_{m1}}-1}C_L$	$\frac{g_{m2}}{2C_L}$	90

3.2.1 Inference from poles and zeroes

The MC-Nulling Resistor and MC-FeedForward configurations allow the control of zero. Potentially, the zero could be made a left half-plane zero with the choice of resistor and feedforward transconductance value. Thus giving a better phase margin in comparison to the Miller Compensation with capacitor alone. In other words, for a given bandwidth the compensation capacitor value can be reduced to obtain same phase margin leading to reduction in area.

3.3 Comments on Two Stage Topologies

3.3.1 MCNR and MCF [2]

The transconductance of the output stage can vary depending on the current drawn. So, the nulling resistor compensation method has to be checked for all possible worst case conditions. Whereas, in the feedforward compensation technique, the location of the zero depends only on the first stage transconductance which can be more accurately fixed. The Feedforward compensation also gives a push-pull output stage.

However, the compensation capacitance is directly proportional to the output capacitance. By fixing the ratio of $\frac{g_{m1}}{g_{m2}}$, the value of compensation capacitance can be reduced. This is the trade-off between the power consumption and area. For a smaller value of C_m, g_{m2} must be larger which in turn means more power consumption.

A macro-model simulation result of two-stage amplifiers is shown in figure(3.2). The parameters used for the simulation are

G_m,r_o,C_L, C_m	Value
g_{m1}, g_{m2}, g_{mf}	200 μS
r_{o1}, r_{of}	1 MΩ
R_L	25 kΩ
C_{m1}	31.8 pF
C_L	15.9 pF

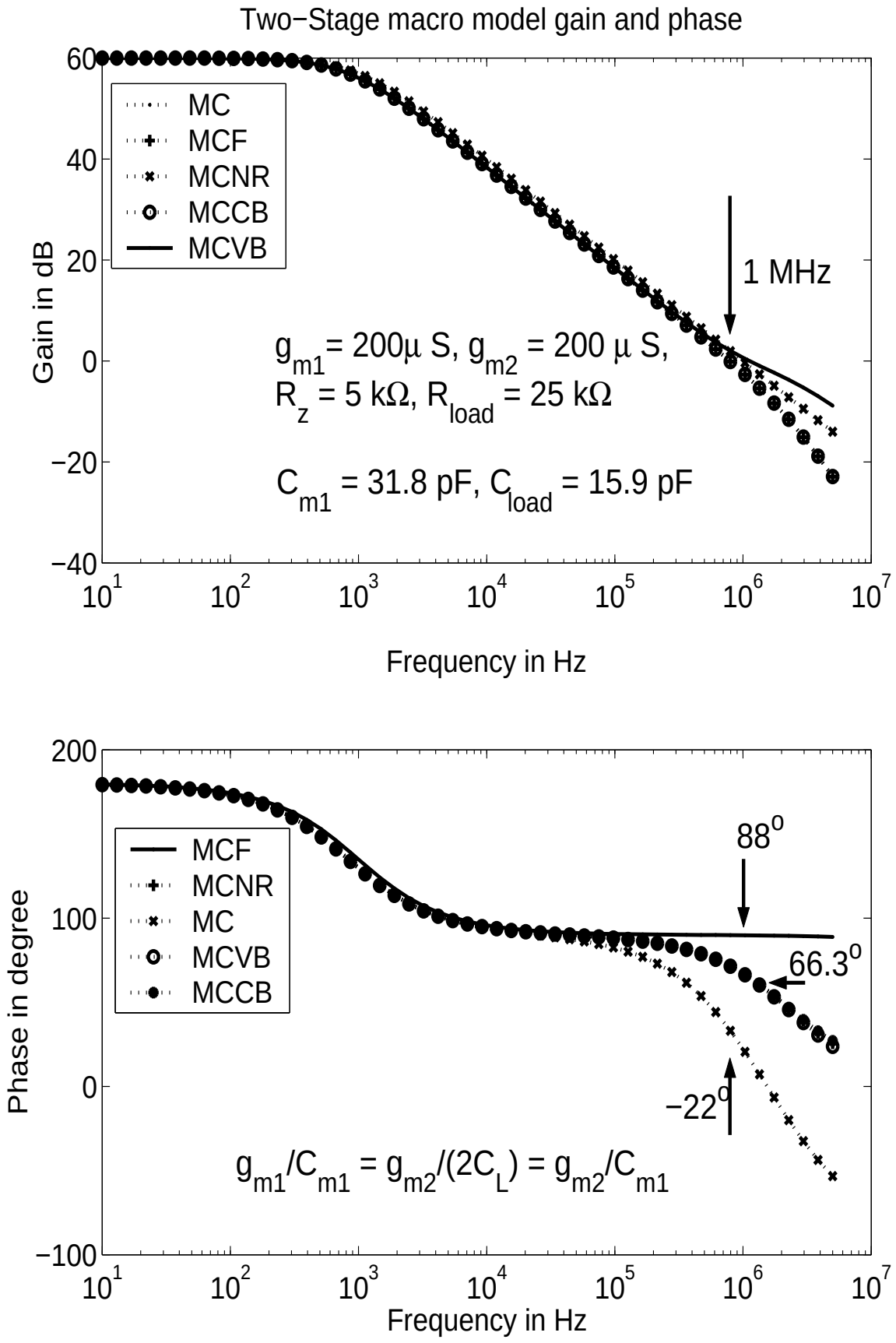


Figure 3.2: Macro-Model simulation result for two-stage macro-model

3.3.2 Miller Compensation - Movement of Poles

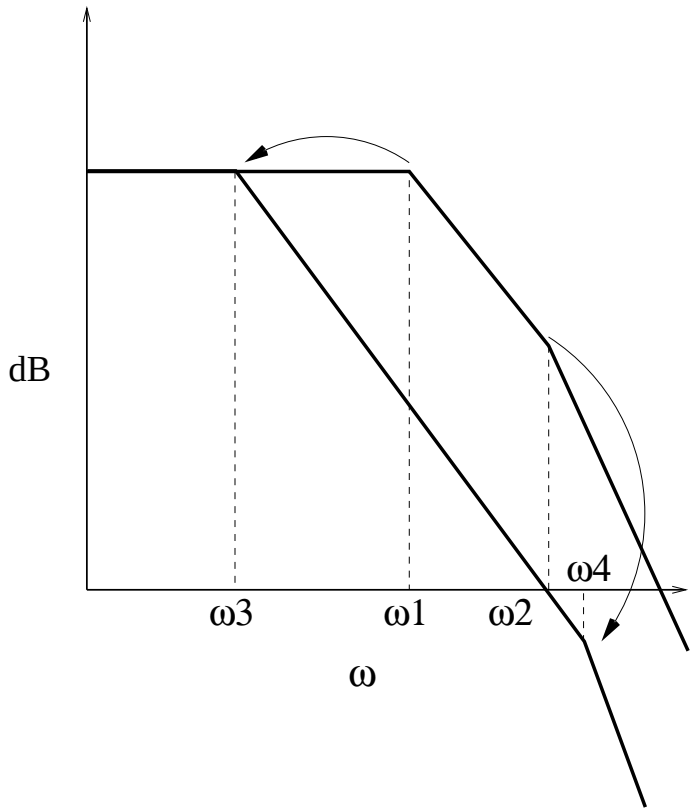


Figure 3.3: Two-Stage Miller - Pole Splitting

$$\omega_1 = \frac{g_{ds1}}{C_p}, \omega_2 = \frac{G_L}{C_L}, \omega_3 = \frac{g_{ds1}}{(1 + \frac{g_{m2}}{G_L})C_m}, \omega_4 = \frac{g_{m2}}{C_L} \tag{3.19}$$

The dominant pole moves to a lower frequency after capacitive feedback and the non-dominant pole moves to a higher frequency. But as we increase the compensation capacitor the high frequency non-dominant pole becomes independant of C_{miller} and stays at $\frac{g_{m2}}{C_L}$. Increase of compensation capacitor after this value will not lead to increase in phase margin. Rather a decrease in unity gain frequency and right half plane zero.

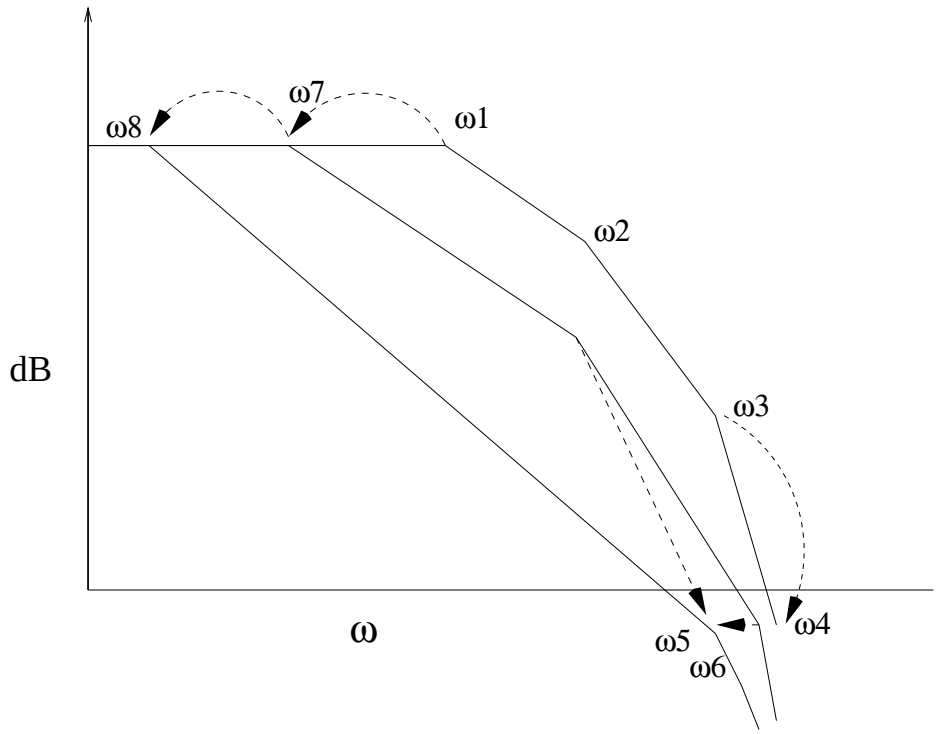


Figure 3.4: Three-Stage Miller - Pole Splitting

3.3.3 Nested Miller Compensation

The second and third Stage can be compensated with C_{m2}. After compensation this can be considered as one stage with one dominant pole.
Again Miller pole splitting can be applied with C_{m1} around first stage and miller compensated second and third stage.

3.4 Three Stage Architectures

This section introduces various three-stage architectures which can be extended from two-stage architectures. The following section describes the small-signal equations and the approximate location of poles and zeroes for the initial design.

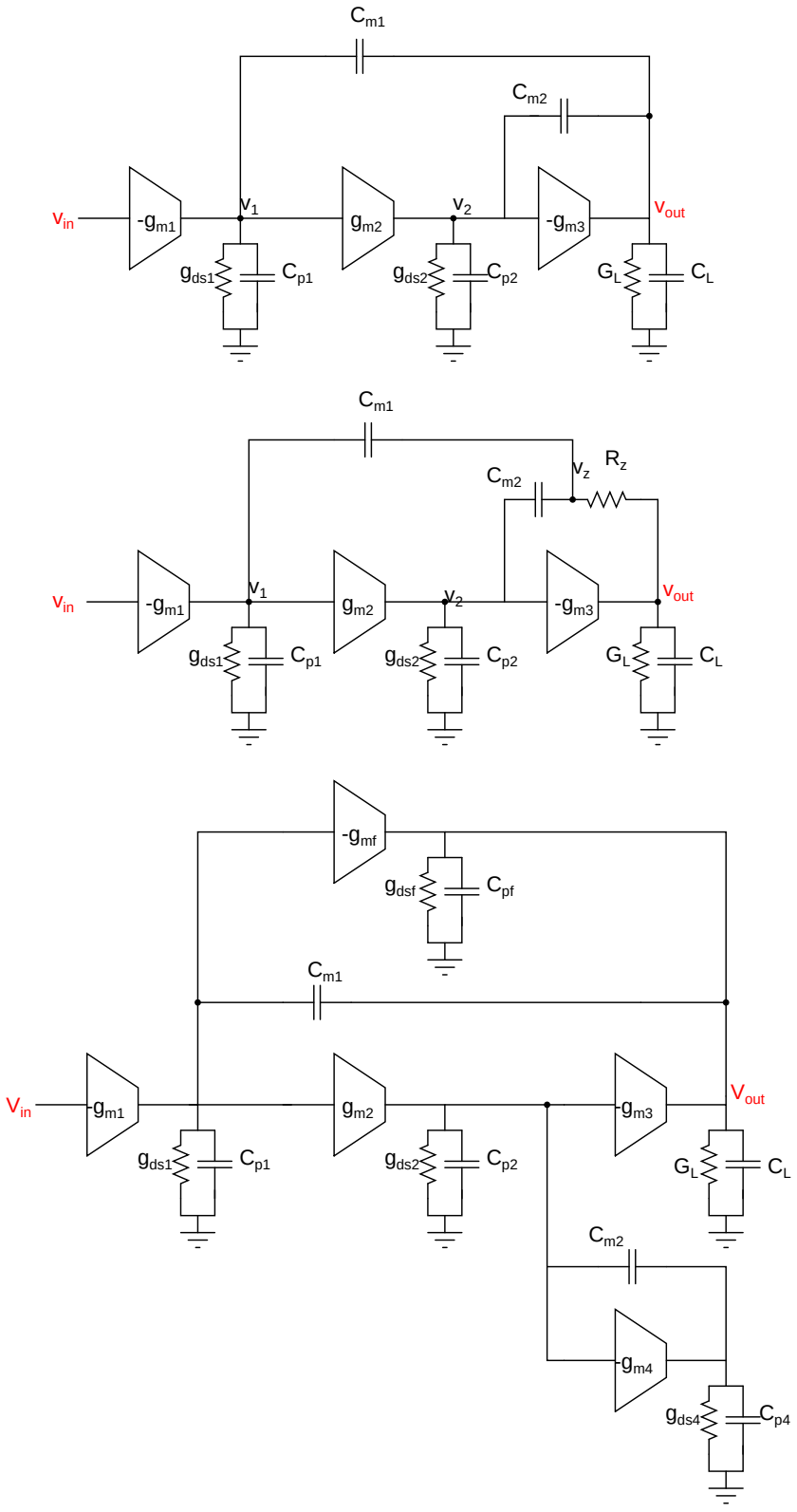


Figure 3.5: Three Stage NMC,NMCNR,DFCFC

The following assumptions are made

$$\frac{g_m}{g_{ds}} \gg 1 \tag{3.20}$$

$$g_{m3} \gg g_{m1}, g_{m2} \tag{3.21}$$

$$C_m, C_L \gg C_p \tag{3.22}$$

3.4.1 NMC

The Three stage NMC expression is derived as follows

$$\frac{V_o(s)}{V_i(s)} = \frac{g_{m1}g_{m2}g_{m3}\left(1 - \frac{sC_{m2}}{g_{m3}} - \frac{s^2C_{m1}C_{m2}}{g_{m2}g_{m3}}\right)}{g_{ds1}g_{ds2}G_L + s(g_{m2}g_{m3}C_{m1}) + s^2C_{m1}C_{m2}(g_{m3} + G_L - g_{m2}) + s^3C_{m1}C_{m2}C_L} \tag{3.23}$$

Applying the approximation A.2 to the above NMC expression

$$\frac{V_o}{V_i} = \frac{g_{m1}g_{m2}g_{m3}\left(1 - s\frac{C_{m2}}{g_{m3}} - \frac{s^2C_{m1}C_{m2}}{g_{m2}g_{m3}}\right)}{g_{ds1}g_{ds2}G_L\left(1 + \frac{sg_{m2}g_{m3}C_{m1}}{g_{ds1}g_{ds2}G_L}\right)\left(1 + \frac{sC_{m2}(g_{m3}+G_L-g_{m2})}{g_{m2}g_{m3}} + \frac{s^2C_{m2}C_L}{g_{m2}g_{m3}}\right)} \tag{3.24}$$

The above three-stage architecture can be compensated in one of the following two ways. The same technique can be applied to other three stage architectures also.

3.4.2 Separate Pole and Complex Pole Compensation

Separate Pole Compensation

Neglecting zeroes based on the assumption $g_{m3} \gg g_{m1}, g_{m2}$

$$A_{vNMC}(s) = \frac{1}{\frac{sC_{m1}}{g_{m1}}\left(1 + \frac{sC_{m2}}{g_{m2}} + \frac{s^2C_LC_{m2}}{g_{m2}g_{m3}}\right)} \tag{3.25}$$

From the above expression GBW, p2, p3 are

$$GBW = \frac{g_{m1}}{C_{m1}}, \quad p_2 = \frac{g_{m2}}{C_{m2}}, \quad p_3 = \frac{g_{m3}}{C_L} \tag{3.26}$$

$$GBW \leq \frac{g_{m2}}{2C_{m2}} \leq \frac{g_{m3}}{4C_L} \tag{3.27}$$

$$PM = 180 - \tan^{-1}\frac{GBW}{p_{3-dB}} - \tan^{-1}\frac{GBW}{p_2} - \tan^{-1}\frac{GBW}{p_3} \tag{3.28}$$

As we can see the C_{m1} and C_{m2} will be large for large C_l

Complex Pole Compensation

In unity gain configuration the amplifier should have a butterworth frequency response

$$H_{NMC}(s) = \frac{A_{vNMC}(s)}{1 + A_{vNMC}(s)} \tag{3.29}$$

$$A_{vNMC}(s) = \frac{1}{s\frac{2}{\omega_0}\left(1 + \frac{s}{\omega_0} + \frac{s^2}{2\omega_0^2}\right)} \tag{3.30}$$

$$A_{vNMC}(s) = \frac{1}{\frac{sC_{m1}}{g_{m1}}\left(1 + \frac{sC_{m2}}{g_{m2}} + \frac{s^2 C_L C_{m2}}{g_{m2}g_{m3}}\right)} \tag{3.31}$$

Comparing the above expressions, we get

$$\frac{2}{\omega_0} = \frac{C_{m1}}{g_{m1}} \tag{3.32}$$

$$\frac{1}{\omega_0} = \frac{C_{m2}}{g_{m2}} \tag{3.33}$$

$$\frac{1}{2\omega_0^2} = \frac{C_L C_{m2}}{g_{m2}g_{m3}} \tag{3.34}$$

The complex second pole is at

$$p_{2,3} = \frac{g_{m3}}{2C_L}(1 \pm \jmath) \tag{3.35}$$

$$\Rightarrow p_{2,3} = \frac{g_{m3}}{\sqrt{2}C_L} \tag{3.36}$$

$$PM = 180 - \tan^{-1}\frac{GBW}{p_{3-dB}} - \tan^{-1}\frac{2\zeta\frac{GBW}{p_{2,3}}}{1 - \frac{GBW^2}{p_{2,3}^2}} \tag{3.37}$$

The complex pole compensation gives a better PM than the Separate pole approach.

3.4.3 NMCNR

We are interested in finding out, how the zeros change with introduction of R_z and the two non-dominant poles relocate.

$$g_{m1}, g_{m2}, g_{m3} \gg g_{ds}; C_{m1}, C_{m2}, C_L \gg C_p$$

$$\begin{aligned} g_{m1}v_{in} + (v_1 - v_z)sC_{m1} &= 0 && (3.38)\\ g_{m2}v_1 - (v_2 - v_z)sC_{m2} &= 0 && (3.39)\\ g_{m3}v_2 + v_{out}(G_L + sC_L) + (v_{out} - v_z)G_z &= 0 && (3.40) \end{aligned}$$

$$v_z = v_{out} + \frac{1}{G_z}\left(g_{m2}v_1 - g_{m1}v_{in}\right) \quad (3.41)$$

After re-arranging and eliminating v_z from the equations, we get

$$\begin{bmatrix} (1 - g_{m2}R_z)sC_{m1} & 0 & -(sC_{m1}) \\ 1 + sR_zC_{m2} & -sC_{m2} & sC_{m2} \\ -g_{m2} & g_{m3} & G_L + sC_L \end{bmatrix} \cdot \begin{bmatrix} v_1 \\ v_2 \\ v_{out} \end{bmatrix} = \begin{bmatrix} -g_{m1}(1 + sC_{m1}R_z) \\ sg_{m1}R_zC_{m2} \\ -g_{m1} \end{bmatrix} \quad (3.42)$$

From the above matrix, sC_{m1} corresponds to the dominant pole. The two non-dominant poles can be derived by removing sC_{m1} from the above matrix.
The two non-dominant poles can be derived from the above equations and the transfer function is described as follows

$$A_{NMCNR}(s) = \frac{g_{m1}g_{m2}g_{m3}\left(s^2\frac{C_{m1}C_{m2}(g_{m3}R_z-1)}{g_{m3}g_{m2}} + s\left[C_{m1}R_z + C_{m2}(R_z - \frac{1}{g_{m3}})\right] + 1\right)}{g_{ds1}g_{ds2}G_L\left(1 + s\frac{C_{m1}g_{m2}g_{m3}}{g_{ds1}g_{ds2}G_L}\right)\left(1 + sC_{m2}\frac{(G_L+g_{m3}-g_{m2}(1+G_LR_z))}{g_{m2}g_{m3}} + s^2C_LC_{m2}\frac{1-g_{m2}R_z}{g_{m2}g_{m3}}\right)} \tag{3.43}$$

Using the approximation A.2, the poles and zeroes can be evaluated.
Placing the second and third pole at twice and four times the unity gain frequency, we get

$$C_{m1} = \frac{4g_{m1}}{g_{m3}}C_L \tag{3.44}$$

$$C_{m2} = \frac{2g_{m2}}{g_{m3}(1-\frac{g_{m2}}{g_{m3}})}C_L \tag{3.45}$$

By setting $R_z = \frac{1}{g_{m3}}$, the RHZ can be eliminated and the phase margin improves. In comparison with NMC, for a given phase margin, the compensation capacitor required for NMCNR is less and hence BW, SR, Ts are higher than NMC model.

3.4.4 DFCFC-Damping Factor Control Frequency Compensation

The C_{m2} across the final stage controls the pole positions of p2, p3. The C_{m2} can be removed and a separate gm4 can be used to control damping factor [7].
The expression derived based on the assumptions $g_{m3} \gg g_{m1}, g_{m2}, C_L, C_m \gg C_p$

$$A_{DFCFC} = \frac{1}{\frac{sC_{m1}g_{m2}g_{m3}}{G_{o1}G_{o2}G_L}\left(1 + \frac{sC_Lg_{m4}}{g_{m2}g_{m3}+g_{m4}g_{mf2}} + \frac{s^2C_LC_{p2}}{g_{m2}g_{m3}+g_{m4}g_{mf2}}\right)} \tag{3.46}$$

Using Complex pole compensation

$$GBW = \frac{g_{m1}}{C_{m1}} \tag{3.47}$$

$$\frac{1}{\omega_0} = \frac{C_L g_{m4}}{g_{m2}g_{m3} + g_{m4}g_{mf2}} \tag{3.48}$$

$$\frac{1}{2\omega_0^2} = \frac{C_L C_{p2}}{g_{m2}g_{m3} + g_{m4}g_{mf2}} \tag{3.49}$$

Eliminating ω_o from the last two expressions

$$\frac{C_L}{C_{p2}} g_{m4}^2 - 2g_{m3}g_{m4} - 2g_{m2}g_{m3} = 0 \tag{3.50}$$

$$g_{m4} = \beta g_{m3} \frac{C_{p2}}{C_L} \tag{3.51}$$

$$C_{m1} = \frac{1}{\beta} \frac{4g_{m1}C_L}{g_{m3}} \tag{3.52}$$

$$\beta = \left(1 + \sqrt{1 + \frac{2g_{m2}C_L}{g_{m3}C_{p2}}}\right) \tag{3.53}$$

$$GBW_{DFCFC} = \beta GBW_{NMC} \tag{3.54}$$

A macro-model simulation result of three-stage amplifiers is shown in figure(3.6). The parameters used for the simulation are

G_m,r_o,C_L, C_m	Value
g_{m1}, g_{m2}	200 μS
g_{m3}, g_{mf1}	200 μS
g_{m4}	50 μS
r_{o1}, r_{of}	1 MΩ
R_L	1 kΩ
$C_{m1,NMC}$	80 pF
$C_{m2,NMC}$	40 pF
$C_{m1,DFCFC}$	8 pF
$C_{m2,DFCFC}$	8 pF
C_L	100 pF

3.4.5 Comparison of Gain, Bandwidth and Stability

The stability conditions indicate that the value of compensation capacitors are directly proportional to C_L. In DFCFC the compensation capacitor is proportional to square root of the load capacitor. The assumption that $g_{m3} \gg g_{m1}, g_{m2}$ may not be satisfied for small resistive loads. This might lead to increase in power consumption. Larger the load capacitor, larger is the compensation capacitor which leads to increase in the area and power. Also the bandwidth decreases with higher order architectures. The following comparison is from [1]

Topology	DC Gain	Stability Conditions	GBW	PM(degree)
SMC	$\frac{g_{m1}g_{m2}}{g_{ds1}G_L}$	$C_{m1} = 2\frac{g_{m1}}{g_{m2}}C_L$	$\frac{g_{m2}}{C_L}$	63-$tan^{-1}(\frac{g_{m1}}{g_{m2}})$
SMCNR	$\frac{g_{m1}g_{m2}}{g_{ds1}G_L}$	$C_{m1} = 2\frac{g_{m1}}{g_{m2}}C_L$	$\frac{g_{m2}}{C_L}$	63
SMCF	$\frac{g_{m1}g_{m2}}{g_{ds1}G_L}$	$C_{m1} = 2\frac{g_{m1}}{g_{m2}}C_L, g_{mf} = g_{m1}$	$\frac{g_{m2}}{C_L}$	63
NMC	$\frac{g_{m1}g_{m2}g_{m3}}{g_{ds1}g_{ds2}G_L}$	$g_{m3} \gg g_{m1}, g_{m2}$ $C_{m1} = 4\frac{g_{m1}}{g_{m3}}C_L$ $C_{m2} = 2\frac{g_{m2}}{g_{m3}}C_L$	$\frac{g_{m3}}{4C_L}$	60
NMCNR	$\frac{g_{m1}g_{m2}g_{m3}}{g_{ds1}g_{ds2}G_L}$	$g_{m3} \gg g_{m1}, g_{m2}, R_z = \frac{1}{g_{m3}}$ $C_{m1} = 4\frac{g_{m1}}{g_{m3}}C_L$ $C_{m2} = 2\frac{g_{m2}}{g_{m3}(1-k_g)}C_L$ $k_g = \frac{g_{m2}}{g_{m3}}$	$\frac{g_{m3}}{4C_L}$	> 60
DFCFC	$\frac{g_{m1}g_{m2}g_{m3}}{g_{ds1}g_{ds2}G_L}$	$g_{m3} \gg g_{m1}, g_{m2}$ $g_{m4} = \beta g_{m3}\frac{C_{p2}}{C_L}$ $C_{m1} = \frac{1}{\beta}\frac{4g_{m1}C_L}{g_{m3}}$ $\beta = \left(1 + \sqrt{1 + \frac{2g_{m2}C_L}{g_{m3}C_{p2}}}\right)$	$\beta\frac{g_{m3}}{4C_L}$	>60

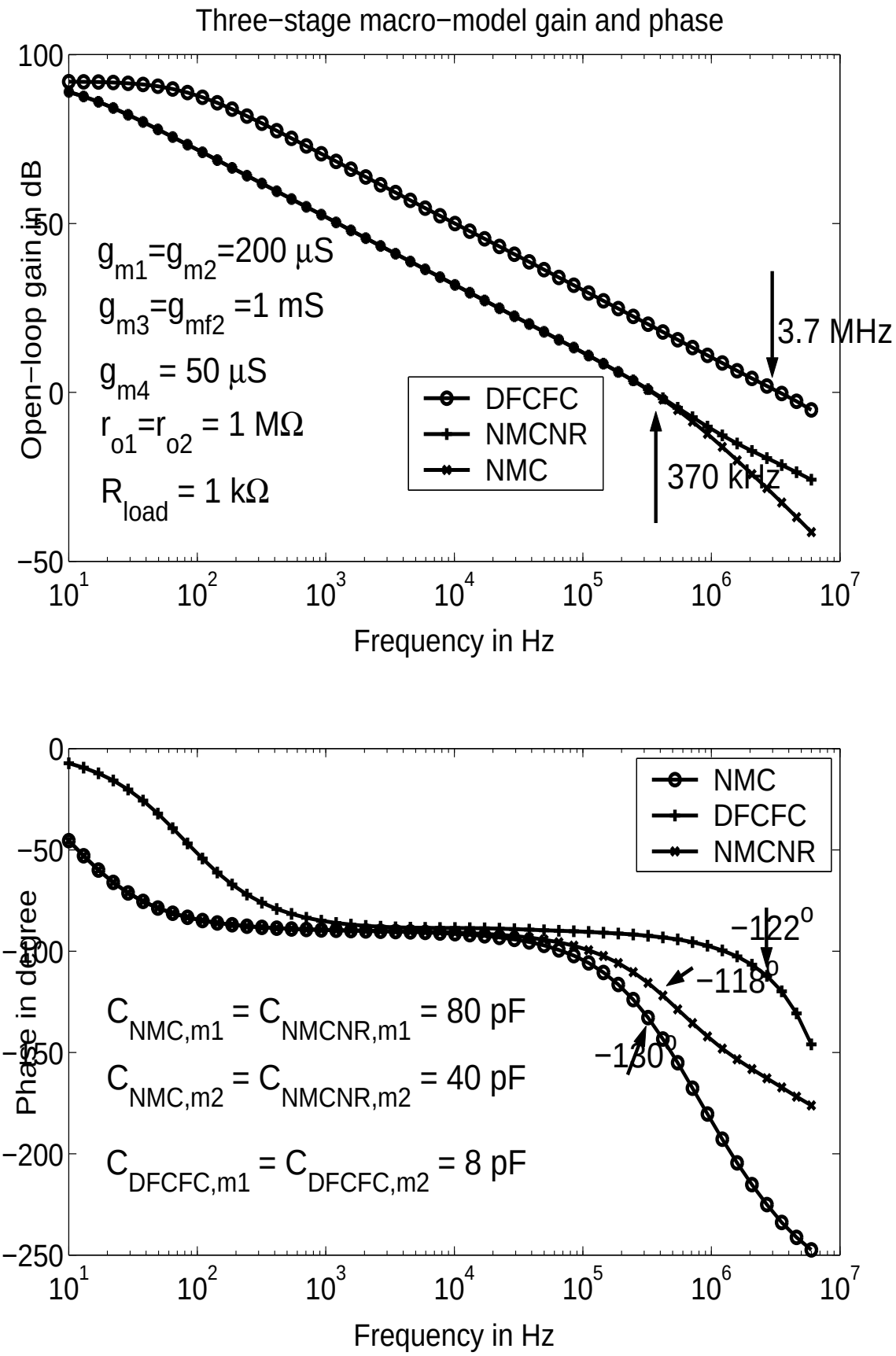


Figure 3.6: Macro-Model simulation result for three-stage macro-model

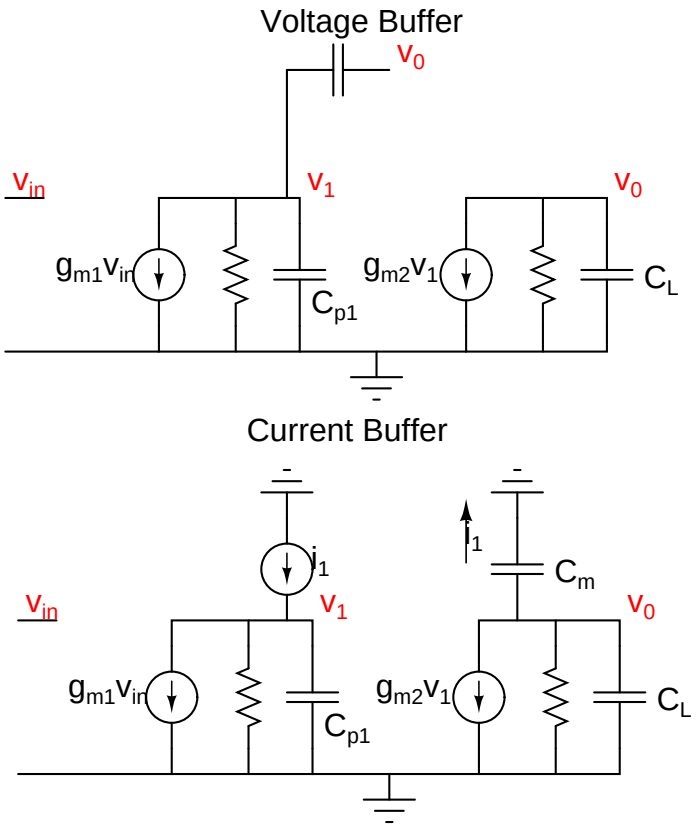


Figure 3.7: Voltage and Current Buffer Feedback

3.5 Two Stage Amplifier - Voltage and Current Buffer Architectures

3.5.1 Miller Compensated Two Stage Amplifier with Voltage Buffer

This section re-visits the two stage compensation technique using voltage and current buffers in the feedback path [12].

$$\begin{bmatrix} g_{ds1} + s(C_{p1} + C_m) & -sC_m \\ g_{m2} & G_L + sC_L \end{bmatrix} . \begin{bmatrix} v_x \\ v_o \end{bmatrix} = \begin{bmatrix} g_{m1} v_{in} \\ 0 \end{bmatrix} \tag{3.55}$$

$$\begin{bmatrix} s(C_m) & -sC_m \\ g_{m2} & G_L + sC_L \end{bmatrix} . \begin{bmatrix} v_x \\ v_o \end{bmatrix} = \begin{bmatrix} g_{m1} v_{in} \\ 0 \end{bmatrix} \tag{3.56}$$

By neglecting g_{ds} and removing sCm from the above matrix the second pole is

$$p_2 = -\frac{g_{m2} + G_L}{C_L} \tag{3.57}$$

Conclusion Voltage buffer compensation capacitor αC_L

3.5.2 Miller Compensated Two Stage Amplifier with Current Buffer

$$\begin{bmatrix} -(g_{ds1} + sC_{p1}) & sC_m \\ g_{m2} & G_L + s(C_L + C_0) \end{bmatrix} . \begin{bmatrix} v_x \\ v_o \end{bmatrix} = \begin{bmatrix} g_{m1} v_{in} \\ 0 \end{bmatrix} \tag{3.58}$$

$$\begin{bmatrix} sC_{p1} & -sC_m \\ g_{m2} & s(C_L + C_m) \end{bmatrix} . \begin{bmatrix} v_x \\ v_o \end{bmatrix} = \begin{bmatrix} g_{m1} v_{in} \\ 0 \end{bmatrix} \tag{3.59}$$

By neglecting g_{ds} and removing sCm from the above matrix the second pole is

$$p_2 = -\frac{g_{m2}}{C_p(\frac{C_L}{C_m} + 1)} \tag{3.60}$$

By placing UGF at half the frequency of the second pole the compensation capacitor value is calculated

$$\frac{g_m}{C_m} = \frac{1}{2}\frac{g_{m2}}{C_p(\frac{C_L}{C_m} + 1)} \tag{3.61}$$

Rearranging

$$2g_{m1}C_p(C_L + C_m) = g_{m2}C_m^2 \tag{3.62}$$

$$C_m^2 - 2\frac{g_{m1}}{g_{m2}}C_pC_m - 2\frac{g_{m1}}{g_{m2}}C_pC_L = 0 \tag{3.63}$$

The roots are

$$C_m = 2\frac{g_{m1}}{g_{m2}}C_p\left(1 + \sqrt{1 + \frac{4C_Lg_{m2}}{2g_{m1}C_p}}\right) \tag{3.64}$$

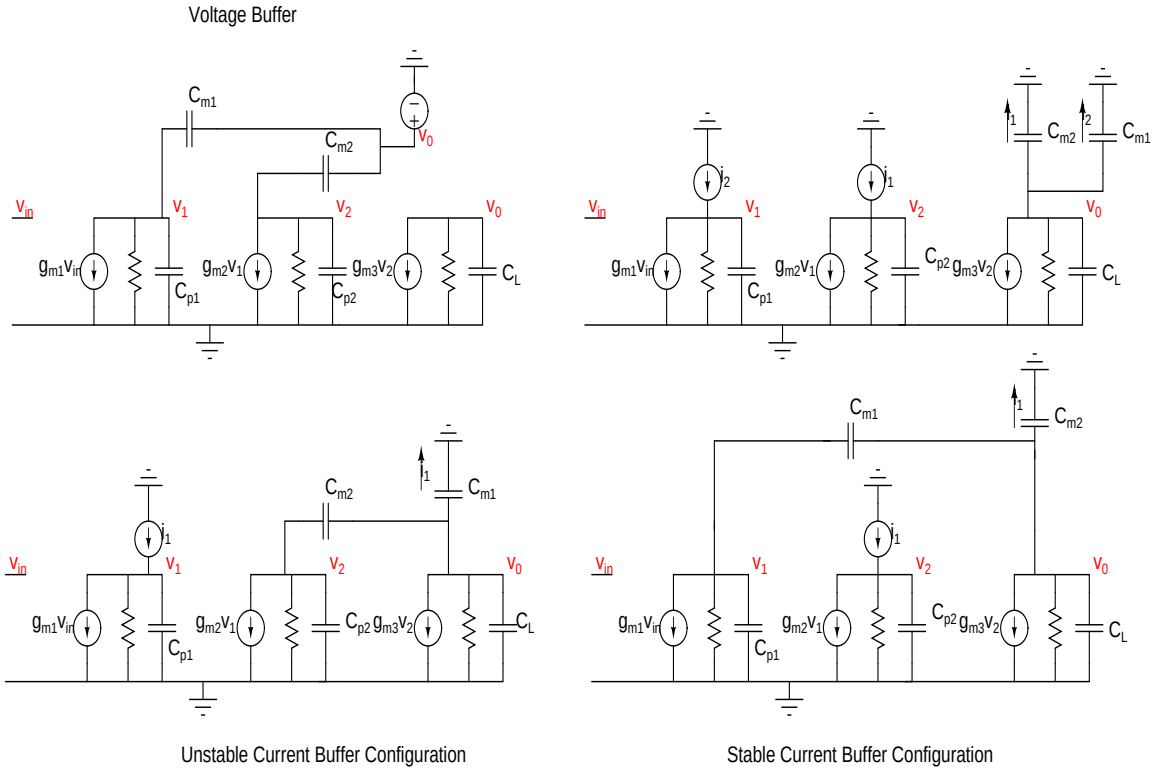


Figure 3.8: Three Stage Voltage Buffer

Conclusion Cm $\alpha\sqrt{C_L}$

3.5.3 Three Stage with Voltage Buffer Compensation

Neglecting gds the higher order poles can be found from the following matrix

$$\begin{bmatrix} -sC_{m1} & 0 & sC_{m1} \\ g_{m2} & -sC_{m2} & sC_{m2} \\ 0 & g_{m3} & sC_L \end{bmatrix} \cdot \begin{bmatrix} v_1 \\ v_2 \\ v_o \end{bmatrix} = \begin{bmatrix} g_{m1}v_{in} \\ 0 \\ 0 \end{bmatrix} \tag{3.65}$$

The second order expression obtained from simplifying the determinant is

$$s^2 \frac{C_{m2}C_L}{g_{m2}g_{m3}} + s\frac{C_{m2}(g_{m3}+G_L)}{g_{m2}g_{m3}} + 1 \tag{3.66}$$

The poles are -b/a and -c/b for $ax^2 + bx + c$

$$p_3 = -\frac{g_{m3} + G_L}{C_L} \tag{3.67}$$

$$p_2 = -\frac{g_{m2}g_{m3}}{C_{m2}(G_L + g_{m3})} \tag{3.68}$$

Conclusion The voltage buffer compensation capacitor is proportional to load capacitor

3.5.4 Three Stage with Current Buffer-Configuration 1

The higher order poles and zeros are obtained from the following matrix

$$\begin{bmatrix} -sC_{p1} & 0 & sC_{m1} \\ g_{m2} & -sC_{m2} & sC_{m2} \\ 0 & g_{m3} - sC_{m2} & s(C_L + C_{m1} + C_{m2}) \end{bmatrix} \cdot \begin{bmatrix} v_1 \\ v_2 \\ v_o \end{bmatrix} = \begin{bmatrix} g_{m1}v_{in} \\ 0 \\ 0 \end{bmatrix} \tag{3.69}$$

Re-arranging and simplifying the determinant by removing sC_{m1}

$$p_2 = -\frac{g_{m2}g_{m3}C_{m1}}{(g_{m3}C_{p1} - g_{m2}C_{m1})C_{m2}} \tag{3.70}$$

$$p_3 = -\frac{g_{m3}}{C_L + C_{m1}}(1 - \frac{C_{m1}g_{m2}}{g_{m3}C_{p1}}) \tag{3.71}$$

by placing ugf at half the frequency of p2 and one fourth of p3 to obtain the stability condition

$$\frac{g_{m1}}{C_{m1}} = \frac{1}{2}\frac{g_{m2}C_{m1}}{C_{p1}C_{m2}(1 - \alpha C_{m1})} \tag{3.72}$$

$$\frac{g_{m1}}{C_{m1}} = \frac{g_{m3}}{4(C_L + C_{m1})}(1 - \alpha C_{m1}) \tag{3.73}$$

After solving for C_{m1} the quadratic expression leads to imaginary Capacitors.The conditions for real roots depends on Cp1 and it cannot be controlled.

Conclusion The two non-dominant poles cannot be controlled.

3.5.5 Three Stage with Current Buffer - Configuration 2

The higher order poles and zeros are obtained from the following matrix

$$\begin{bmatrix} -sC_{p1} & 0 & sC_{m1} \\ g_{m2} & -sC_{p2} & sC_{m2} \\ 0 & g_{m3} & s(C_L + C_{m1} + C_{m2}) \end{bmatrix} \cdot \begin{bmatrix} v_1 \\ v_2 \\ v_o \end{bmatrix} = \begin{bmatrix} g_{m1}v_{in} \\ 0 \\ 0 \end{bmatrix} \tag{3.74}$$

Re-arranging and simplifying the determinant by removing sC_{m1}

$$p_2 = -\frac{g_{m3}C_{m2}}{C_{p2}(C_L + C_{m1} + C_{m2})} \tag{3.75}$$

$$p_3 = -\frac{g_{m2}C_{m1}}{C_{m2}C_{p1}} \tag{3.76}$$

by placing ugf at half the frequency of p2 and one fourth of p3 to obtain the stability condition

Solving for C_{m1} and C_{m2} gives

$$C_{m1} = \sqrt{\frac{32g_{m1}^2 C_L C_{p2}}{g_{m2}g_{m3}}} \tag{3.77}$$

$$C_{m2} = \sqrt{\frac{8g_{m2}C_L C_{p2}}{g_{m3}}} \tag{3.78}$$

Conclusion The compensation capacitors are proportional to the square root of load capacitor

3.6 Two Stage with Current Amplifier

The Transfer function is

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}g_{m2}}{s^2C_{p1}(C_L + \frac{C_m}{k}) + s(C_{p1}g_{ds2} + C_L g_{ds1} + C_m(g_{m2} + \frac{g_{ds1}}{k})) + g_{ds1}g_{ds2}} \tag{3.79}$$

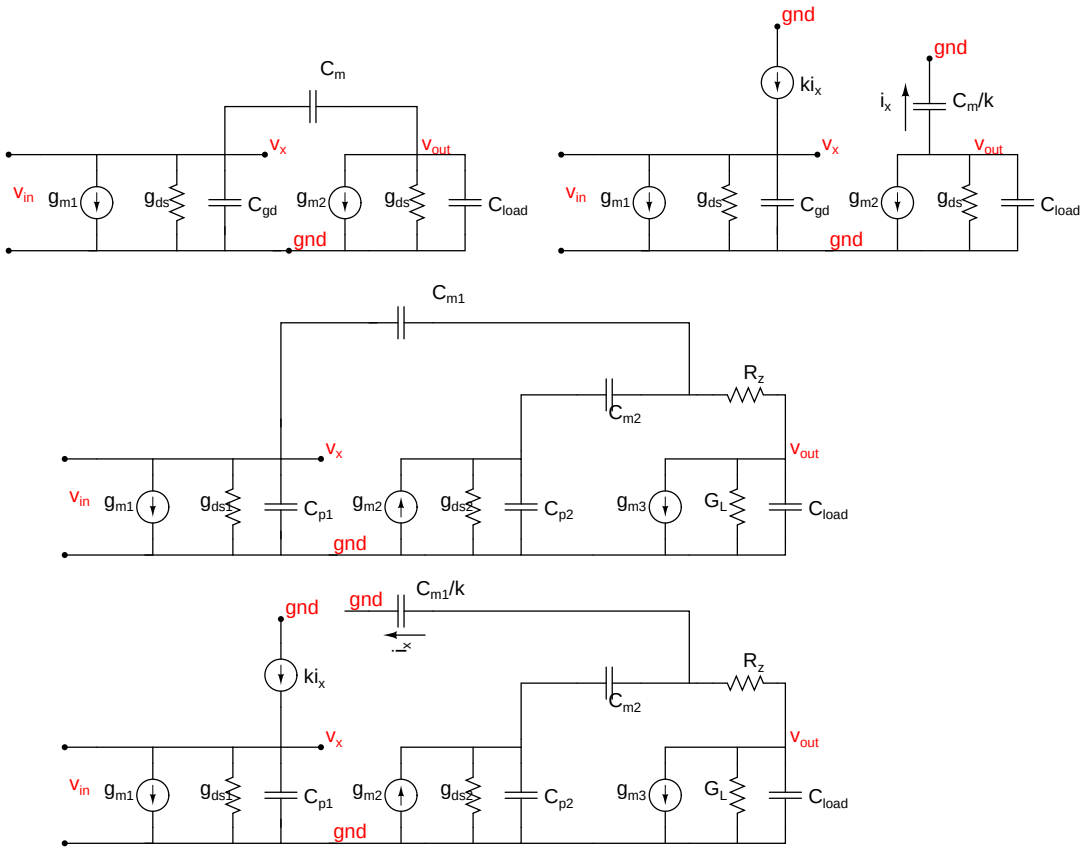


Figure 3.9: CS ,CS with Current Multiplier,NMCNR,NMCNR with Current Multiplier

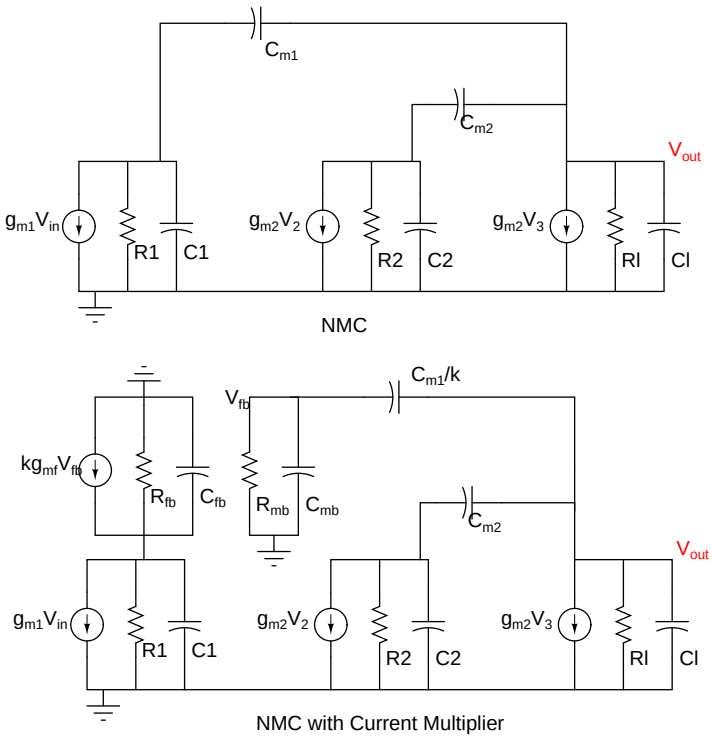


Figure 3.10: NMC,NMC-Current Multiplier

The poles of the above equation are

$$p_1 = -\frac{C_{p1}g_{ds2} + C_L g_{ds1} + C_m(g_{m2} + \frac{g_{ds1}}{k})}{C_{p1}(C_L + \frac{C_m}{k})} \approx \frac{C_m g_{m2}}{C_{p1}(C_L + \frac{C_m}{k})} \quad (3.80)$$

$$p_2 = -\frac{g_{ds1}g_{ds2}}{C_{p1}g_{ds2} + C_L g_{ds1} + C_m(g_{m2} + \frac{g_{ds1}}{k})} \approx \frac{g_{ds1}g_{ds2}}{C_m g_{m2}} \quad (3.81)$$

UGB is still the same whereas the condition for non-dominant pole is

$$\frac{g_{m1}}{C_{m1}} = \frac{C_m g_{m2}}{2C_{p1}(C_L + \frac{C_m}{k})} \approx \frac{C_m g_{m2}}{2C_{p1}C_L} \quad (3.82)$$

Comparing the Cm for the Two Stage Amplifier and the Current Multiplier

$$C_{m1} = \frac{2g_{m1}C_L}{g_{m2}} \quad (3.83)$$

$$C_{m2} = \sqrt{\frac{2g_{m1}C_L C_{p1}}{g_{m2}}} \quad (3.84)$$

3.7 Comment on Voltage Buffer and Current Buffer Architectures

The Compensation capacitor required for the current multiplier is proportional to square root of the load capacitor. Hence for a given load capacitor current buffer architecture will have higher bandwidth in comparison to voltage buffer architecture. Current Multiplier will give a reduction in the compensation capacitor value at the cost of power dissipated in mirroring the feedback small signal current from the output. The trade off is between power and area. Feedforward architectures also provide control of compensation capacitor values. The trade off here is between power and input noise performance. The non-ideal feedback current mirror introduces additional poles and it has to taken into account for determining compensation capacitors.

The Current Multiplier was simulated with the NMCNR Macro-model and NMCNR Transistor level model. We can see that by using k times lesser capacitor

depending on the power budget similar or better phase margin is obtained. The Simulation was performed with macro-model NMCNR. The compensation capacitors used were 80 pF and 13.6 pF. With Current Multiplier (Ideal) 36pF and 8pF were used for the same NMCNR macro-model with ideal current buffer. This was verified with the transistor level model and ideal current buffer, the compensation capacitors used are 36pF and 8pF as supposed to 80 pF and 13.6 pF for normal NMCNR without current buffer. A current multiplier can also be used to reduce the capacitance value. The small signal compensation current pumped into the second and first stage outputs will be the same, but the capacitor required to produce this compensation will be reduced by a factor of the current mirror.

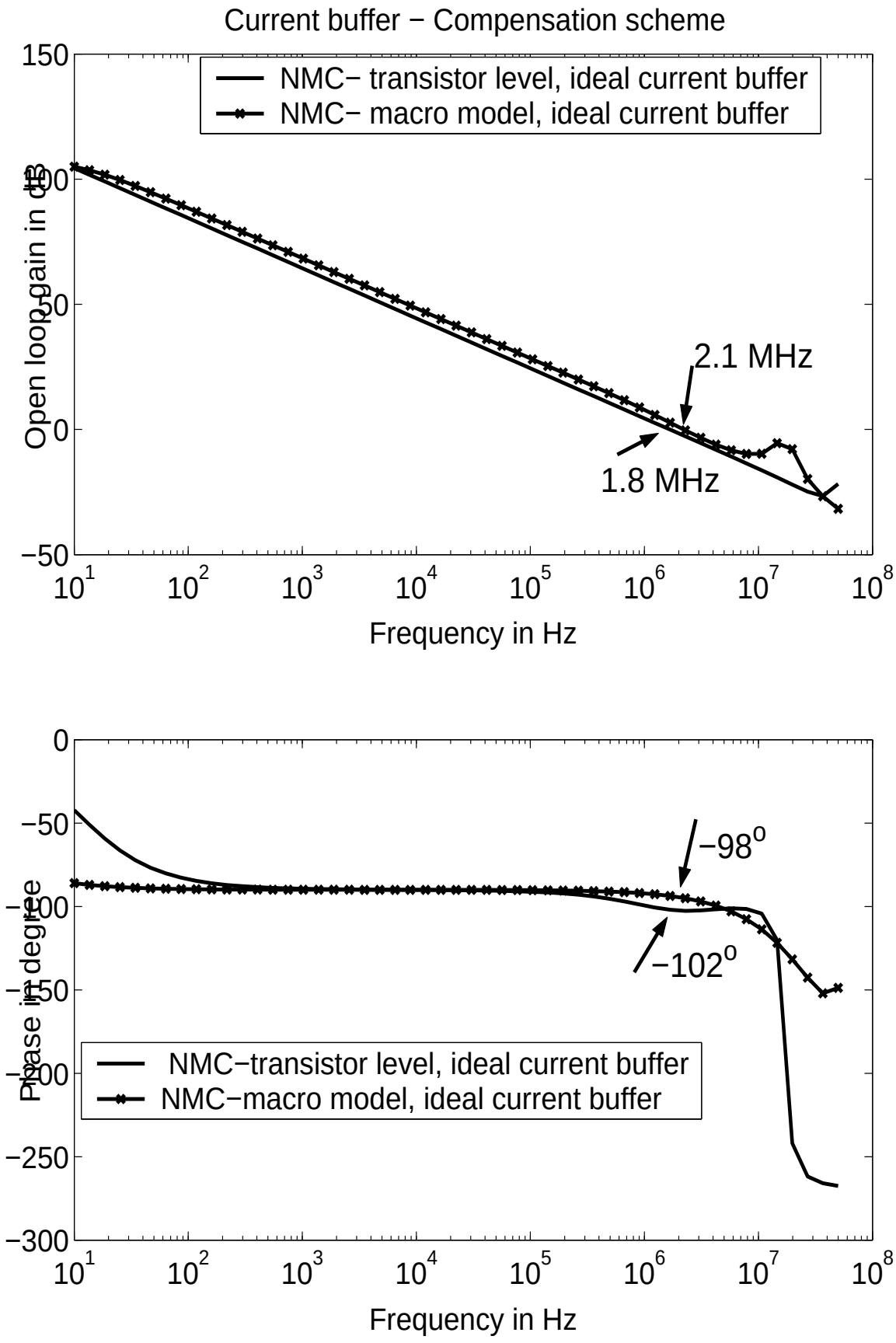


Figure 3.11: Three-stage current buffer compensation

CHAPTER 4

Operational Amplifier - Design

Design of a three stage class AB operational amplifier is discussed in this chapter. Multi-stage architecture was chosen to obtain the high gain required for the I-V conversion of the R-2R ladder current source. Miller compensation technique is used for compensating the three stage amplifier. The design involves optimization of noise, power, distortion and bandwidth. The following sections discusses the above in detail.

4.1 Specification

Supply	1.8V $\pm$5%
Sample Rate	6.144MHz
Single-ended Output	0.5V RMS
Load	1kΩ & 100pF
Idle Channel Noise	5μV (20Hz-96kHz)
THD + N	-80dB
DC Offset	$\leq$ 5mV
Power	$\leq$ 2mW
Gain	$\geq$ 100dB A.4

4.1.1 Opamp Architectures

In this chapter, Two-Stage, Three Stage architectures are analyzed for the above mentioned performance criterion. Nested Miller Compensation technique with and without Nulling Resistor, Damping Factor Technique, Feedforward compensation are analyzed. Class-AB output stage was chosen for power consideration.

First Stage of the amplifier was optimized for noise performance. Nested Miller compensation with nulling resistor gives smaller compensation capacitance and hence larger slew rate and smaller area, thus giving a better overall performance as compared to Damping Factor compensation.

4.1.2 Two Stage Architecture

First stage can be telescopic cascode and second stage ass common source stage. To obtain maximum gain from the first stage, increase gate length to 1 μm.

$$A_{dc} \approx (\frac{g_m}{g_{ds}})^2 \times \frac{g_{m2}}{G_L} \approx 10 \times 2^{16} \tag{4.1}$$

$$say\ \frac{g_m}{g_{ds}} \approx 100 \tag{4.2}$$

Its not feasible to get $\frac{g_{m2}}{G_L} = 65.53$. Since the output has to drive a resistive load of 1 kΩ, the power consumption for this architecture will be huge.

4.1.3 Three Stage Architecture

The three stage architectures can be considered as an extenstion of two stage architecture. In other words, the two stage opamp after compensation can be considered as a system with one dominant pole and can be used to build another two stage architecture, thus leading to higher order. The negative gain amplifier can be anyone of the three, two stage architectures. The following figure explains the idea.

4.1.4 Flicker noise optimization

At very low frequencies (20-20 kHz), the flicker noise contribution from MOSFET is maximum. Hence, this should be minimized.

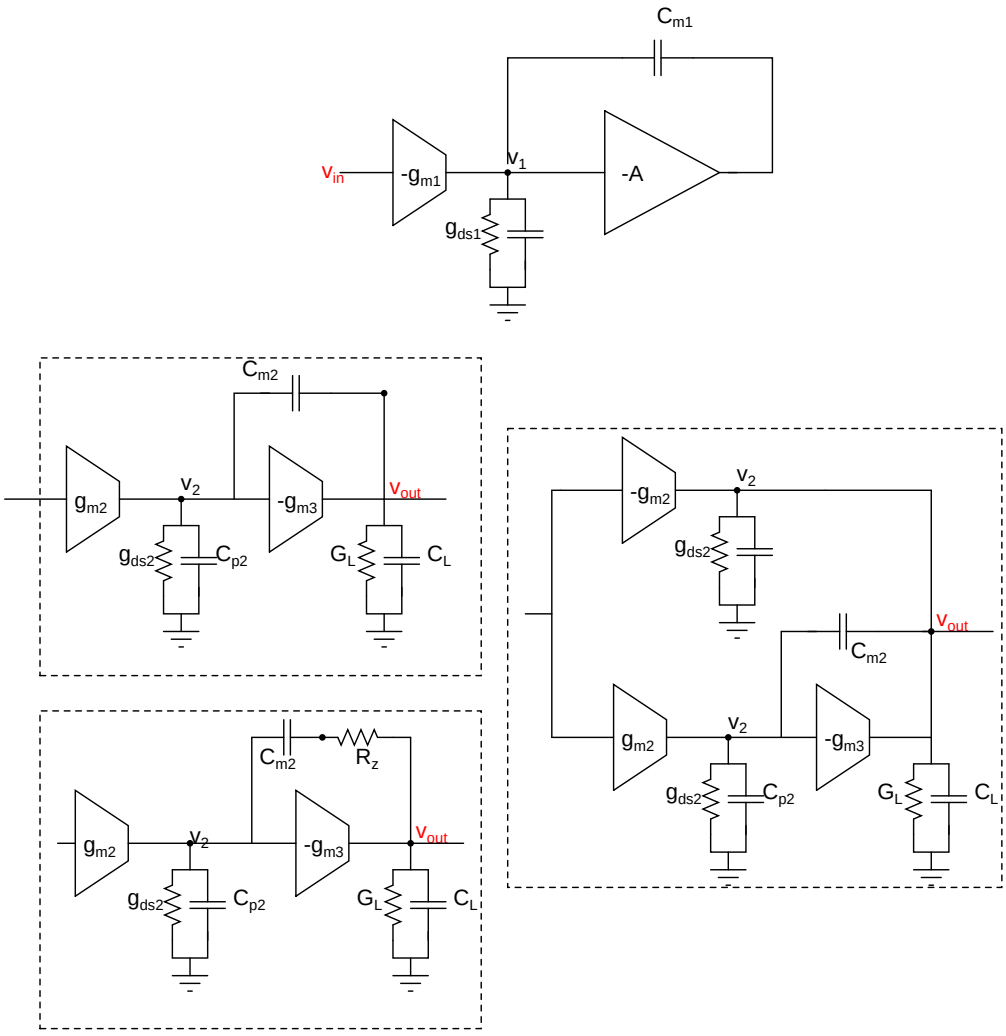


Figure 4.1: Three Stage Architecture

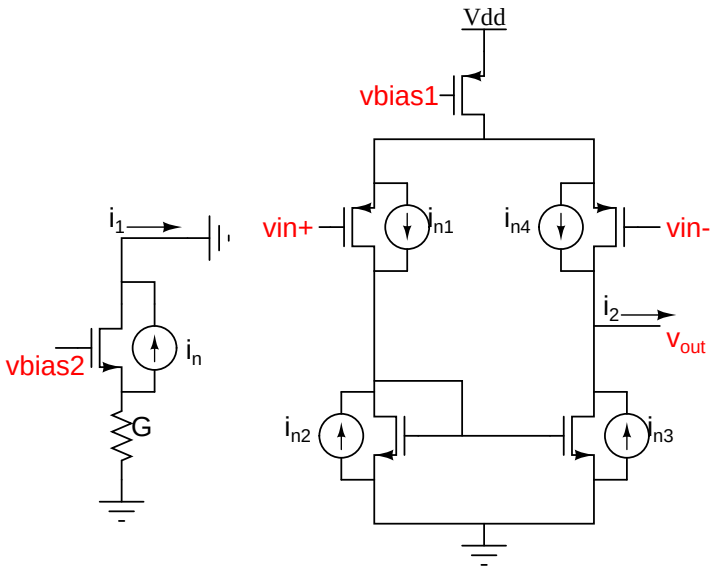


Figure 4.2: Single Stage Noise Currents

$$\bar{i_n^2} = \frac{8}{3}kTg_m + \frac{KF \times I_D}{fC_{ox}L^2} \tag{4.3}$$

$$\bar{v_n^2} = \frac{8}{3g_m}kT + \frac{K}{C_{ox}WL} \tag{4.4}$$

Let us consider the flicker noise alone

$$\bar{i_{n,out}^2} = \frac{KF_nI_d}{fC_{ox}L_n^2} + \frac{KF_pI_d}{fC_{ox}L_p^2} \tag{4.5}$$

$$\bar{v_{in}^2} = \frac{1}{g_m^2}\left[\frac{KF_nI_d}{fC_{ox}L_n^2} + \frac{KF_pI_d}{fC_{ox}L_p^2}\right] \tag{4.6}$$

$$= \bar{v_p^2}\left[\frac{L_p^2K_n'}{L_n^2K_p'} + 1\right] \tag{4.7}$$

So Ln > Lp to reduce relative contribution and Lp must be large enough to meet noise specification independantly.

The noise current flowing out of a source degenerated transistor is

$$i_{out} = \frac{G + g_{ds}}{g_m + G + g_{ds}}i_n \tag{4.8}$$

4.2 NMC,NMCNR

The following assumptions are made

$$\frac{g_m}{g_{ds}} \gg 1 \tag{4.9}$$

$$g_{m3} \gg g_{m1}, g_{m2} \tag{4.10}$$

$$C_m, C_L \gg C_p \tag{4.11}$$

The Three stage NMC expression is

$$\frac{V_o}{V_i} = \frac{g_{m1}g_{m2}g_{m3}\left(1 - s\frac{C_{m2}}{g_{m3}} - \frac{s^2C_{m1}C_{m2}}{g_{m2}g_{m3}}\right)}{g_{ds1}g_{ds2}G_L\left(1 + \frac{sg_{m2}g_{m3}C_{m1}}{g_{ds1}g_{ds2}G_L}\right)\left(1 + \frac{sC_{m2}(g_{m3}+G_L-g_{m2})}{g_{m2}g_{m3}} + \frac{s^2C_{m2}C_L}{g_{m2}g_{m3}}\right)} \tag{4.12}$$

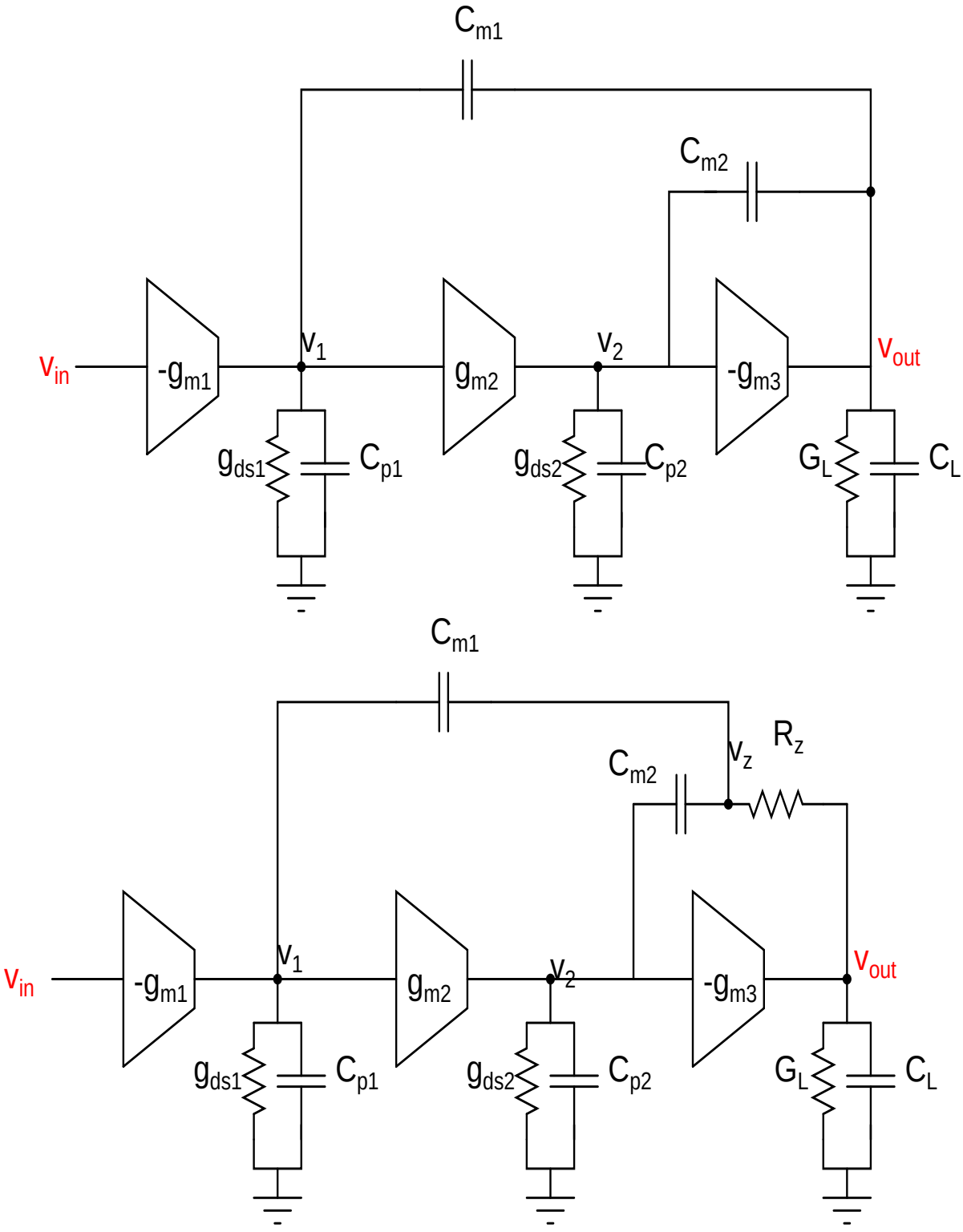


Figure 4.3: NMC,NMCNR

4.2.1 Separate Pole Compensation

$$A_v(s) = \frac{A_{dc}}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)\left(1+\frac{s}{p_3}\right)} \tag{4.13}$$

$$A_v(s) = \frac{1}{\frac{s}{\omega_u}\left(1+\frac{s}{p_2}\right)\left(1+\frac{s}{p_3}\right)} \tag{4.14}$$

$$PM = 180 - \tan^{-1}\frac{\omega_u}{p_1} - \tan^{-1}\frac{\omega_u}{p_2} - \tan^{-1}\frac{\omega_u}{p_3} \tag{4.15}$$

$$\omega_u = \frac{p_2}{2} = \frac{p_3}{4}$$

then PM =49.4^o

Neglecting Zeros based on the assumption $g_{m3} \gg g_{m1}, g_{m2}$

$$A_{vNMC}(s) = \frac{1}{\frac{sC_{m1}}{g_{m1}}\left(1+\frac{sC_{m2}}{g_{m2}}+\frac{s^2C_LC_{m2}}{g_{m2}g_{m3}}\right)} \tag{4.16}$$

From the above expression ω_u ,p2 ,p3 are

$$\omega_u = -\frac{g_{m1}}{C_{m1}}, p_2 = -\frac{g_{m2}}{C_{m2}}, p_3 = -\frac{g_{m3}}{C_L} \tag{4.17}$$

$$\omega_u = \frac{g_{m2}}{2C_{m2}} = \frac{g_{m3}}{4C_L} \tag{4.18}$$

$$PM = 180 - \tan^{-1}\frac{\omega_u}{p_1} - \tan^{-1}\frac{\omega_u}{p_2} - \tan^{-1}\frac{\omega_u}{p_3} \tag{4.19}$$

4.2.2 Complex Pole Compensation

In Unity gain configuration the amplifier should have a Butterworth response

$$H_{NMC}(s) = \frac{A_{vNMC}(s)}{1+A_{vNMC}(s)} \tag{4.20}$$

$$= \frac{1}{1+s\frac{2}{\omega_0}+s^2\frac{2}{\omega_0^2}+s^3\frac{1}{\omega_0^3}} \tag{4.21}$$

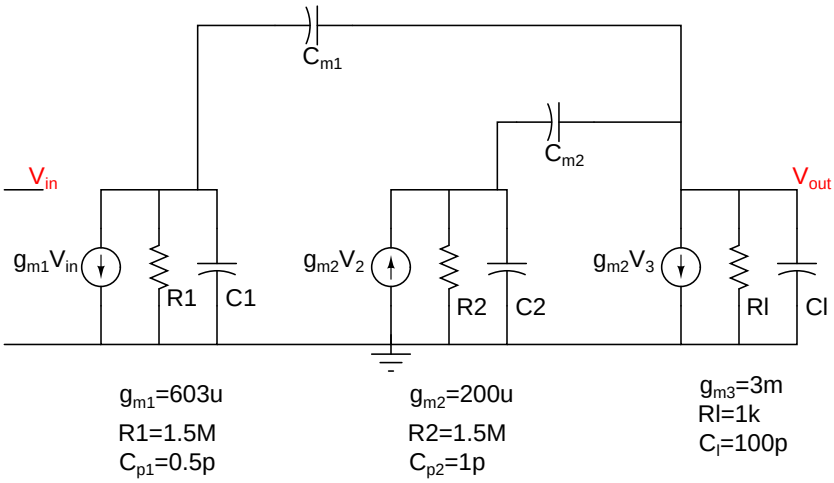


Figure 4.4: NMC- Macro Model

$$A_{vNMC}(s) = \frac{1}{s\frac{2}{\omega_0}\left(1+\frac{s}{\omega_0}+\frac{s^2}{2\omega_0^2}\right)} \tag{4.22}$$

$$A_{vNMC}(s) = \frac{1}{\frac{sC_{m1}}{g_{m1}}\left(1+\frac{sC_{m2}}{g_{m2}}+\frac{s^2C_LC_{m2}}{g_{m2}g_{m3}}\right)} \tag{4.23}$$

$$\Rightarrow \frac{2}{\omega_0}=\frac{C_{m1}}{g_{m1}}, \quad \frac{1}{\omega_0}=\frac{C_{m2}}{g_{m2}}, \quad \frac{1}{2\omega_0^2}=\frac{C_LC_{m2}}{g_{m2}g_{m3}} \tag{4.24}$$

$$p_{2,3} = -\frac{g_{m3}}{2C_L}(1\pm\jmath) \tag{4.25}$$

$$\Rightarrow p_{2,3} = -\frac{g_{m3}}{\sqrt{2}C_L} \tag{4.26}$$

$$PM = 180-\tan^{-1}\frac{\omega_u}{p_1}-\tan^{-1}\frac{2\zeta\frac{\omega u}{p_{2,3}}}{1-\frac{\omega_u^2}{p_{2,3}^2}} \tag{4.27}$$

The complex pole compensation gives a better PM than the Separate pole approach.

$$\zeta=\frac{1}{\sqrt{2}}, \omega_u=-\frac{g_{m3}}{4C_L}, p_{2,3}=-\frac{g_{m3}}{\sqrt{2}C_L}$$

PM $= 60^o$

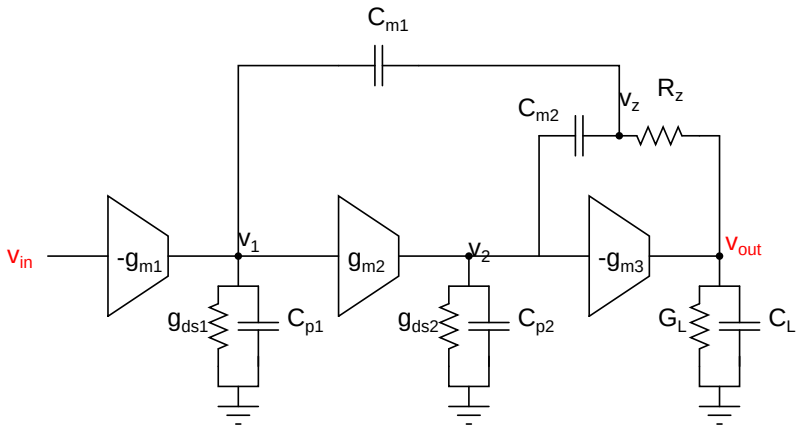


Figure 4.5: NMCNR

$$C_{m1} = \frac{4g_{m1}}{g_{m3}} C_L = 80pF \tag{4.28}$$

$$C_{m2} = \frac{2g_{m2}}{g_{m3}} C_L = 13.3pF \tag{4.29}$$

The Compensation capacitor required is proportional to the load capacitor. Further we have assumed that $g_{m3} \gg g_{m1}, g_{m2}$. The reason is clear as we examine the transfer function of NMC.

$$\frac{V_o}{V_i} = \frac{g_{m1}g_{m2}g_{m3}\left(1 - s\frac{C_{m2}}{g_{m3}} - \frac{s^2 C_{m1}C_{m2}}{g_{m2}g_{m3}}\right)}{g_{ds1}g_{ds2}G_L\left(1 + \frac{sg_{m2}g_{m3}C_{m1}}{g_{ds1}g_{ds2}G_L}\right)\left(1 + \frac{sC_{m2}(g_{m3}+G_L-g_{m2})}{g_{m2}g_{m3}} + \frac{s^2 C_{m2}C_L}{g_{m2}g_{m3}}\right)} \tag{4.30}$$

$$\omega_u = -\frac{g_{m1}}{C_{m1}}, p_2 = -\frac{g_{m2}}{C_{m2}}, p_3 = -\frac{g_{m3}}{C_L} \tag{4.31}$$

$$z_1 = -\frac{g_{m2}}{C_{m1}}, z_2 = \frac{g_{m3}}{C_{m2}} \tag{4.32}$$

The previous design was assuming that the right half plane zero does not cause any phase shift. This will happen when the $g_{m3} \gg g_{m1}, g_{m2}$. The Right half plane zero can be cancelled by zero nulling resistor which leads to NMCNR.

4.2.3 NMCNR - Nested Miller Compensation Nulling Resistor

$$\frac{v_o}{v_i} = \frac{g_{m1}g_{m2}g_{m3}\left(s^2\frac{C_{m1}C_{m2}(g_{m3}R_z-1)}{g_{m3}g_{m2}} + s\left[C_{m1}R_z + C_{m2}(R_z - \frac{1}{g_{m3}})\right] + 1\right)}{g_{ds1}g_{ds2}G_L\left(1 + s\frac{C_{m1}g_{m2}g_{m3}}{g_{ds1}g_{ds2}G_L}\right)\left(1 + s\frac{C_{m2}(G_L+g_{m3}-g_{m2}(1+G_LR_z))}{g_{m2}g_{m3}} + s^2\frac{(1-g_{m2}R_z)C_LC_{m2}}{g_{m2}g_{m3}}\right)} \tag{4.33}$$

It is clear that by choosing $R_z = \frac{1}{g_{m3}}$, the RHP zero can cancelled.
By applying the approximation A.2, the poles and zeroes are

$$p_1 = -\frac{g_{m2}}{C_{m2}(1 - \frac{g_{m2}}{g_{m3}})} \tag{4.34}$$

$$p_2 = -\frac{g_{m3}}{C_L} \tag{4.35}$$

$$z_1 = -\frac{g_{m3}}{C_{m1}} \tag{4.36}$$

So Phase Margin is approximately

$$PM = 90 - tan^{-1}\frac{\omega_u}{p_1} - tan^{-1}\frac{\omega_u}{p_2} + tan^{-1}\frac{\omega_u}{z_1} \tag{4.37}$$

$$\approx 62^o \tag{4.38}$$

4.2.4 Output Stage- Translinear Driver

Class AB output stage was chosen to minimize the quiescent power consumption. The following translinear stage was implemented for the output stage. The sum of the gate-source voltage of M7,M8 is constant and is equal to sum of M2 and M4. This allows control of the quiescent current of the output stage and also the peak current gate-source voltage required.

$$V_{gs7} + V_{gs8} = V_{gs2} + V_{gs4} \tag{4.39}$$

$$V_{gs6} + V_{gs5} = V_{gs3} + V_{gs1} \tag{4.40}$$

The output stage is a translinear circuit by Monticelli [10].

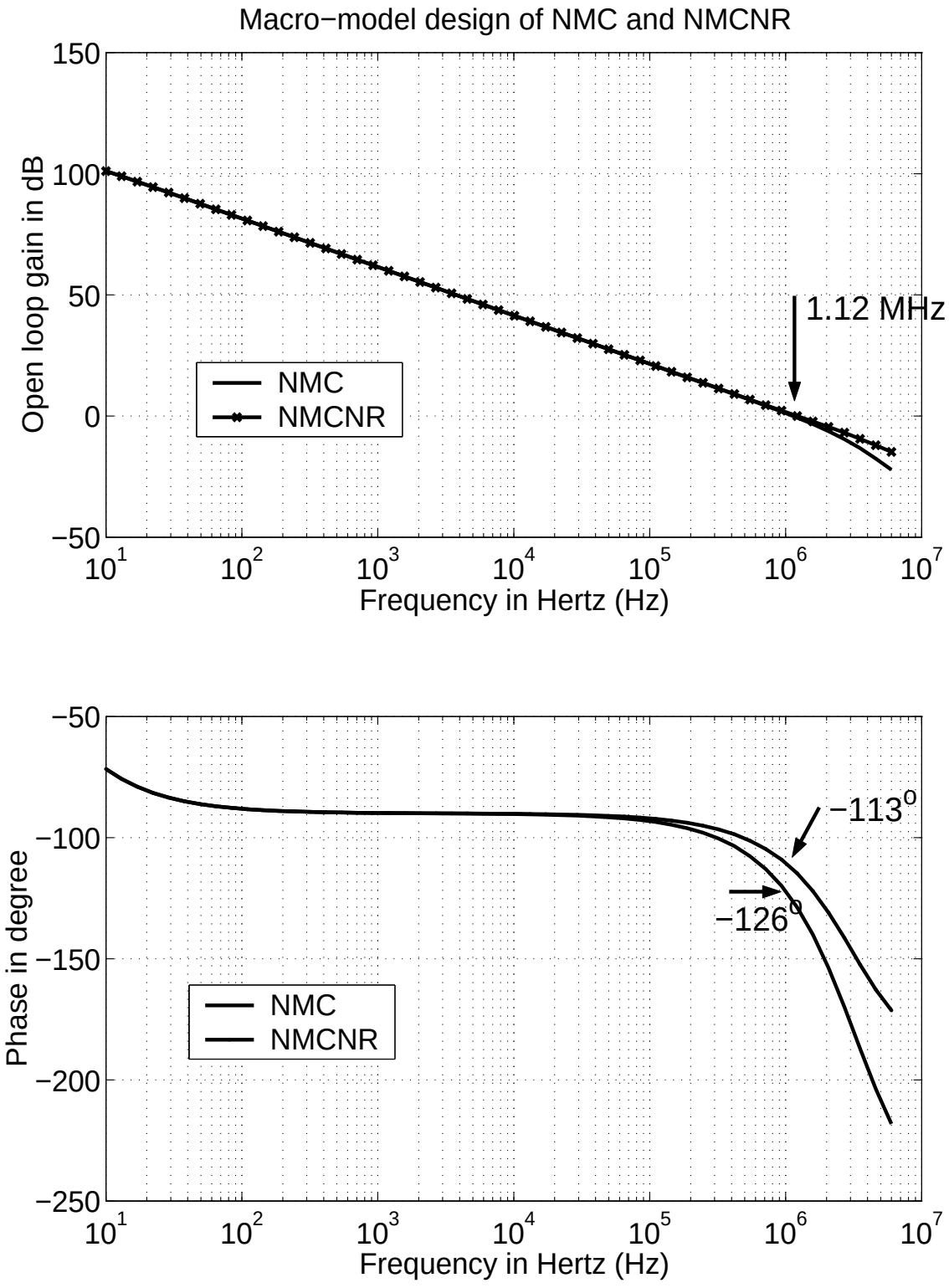


Figure 4.6: NMC,NMCNR - Macro-model design

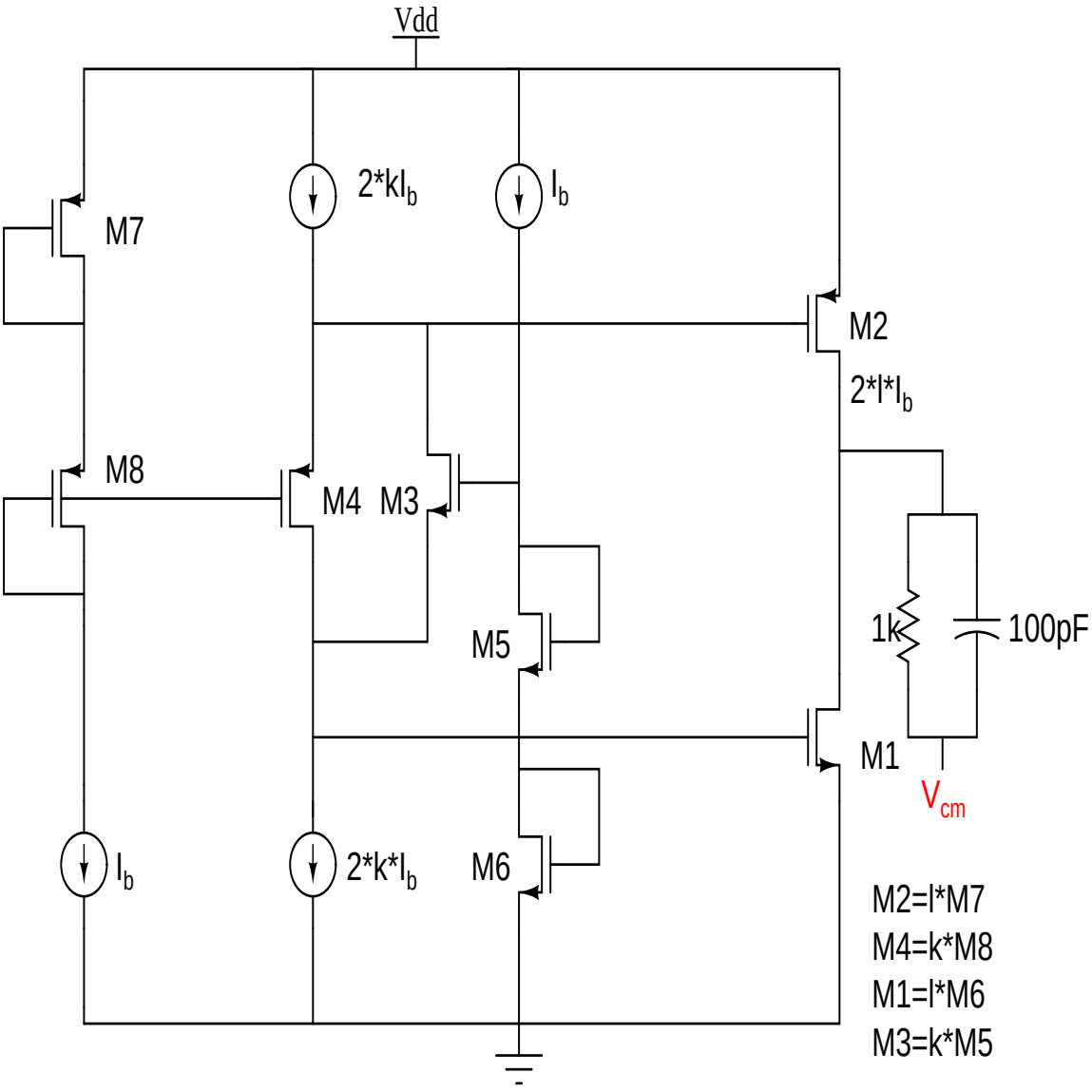


Figure 4.7: Monticelli Driver

4.2.5 Random-Mismatch Analysis

No two components fabricated in an Integrated Circuit are identical. They suffer from a variety of mismatches. Threshold gradient, current factor gradient, dimension mismatch and several other mismatches arise during the process of fabrication.

We are interested in threshold mismatch and current factor (β) mismatch of the two transistors.

The threshold mismatch has been modelled as a random variable with standard deviation as

$$\sigma_{v_{th}} = \frac{A_{v_{th}}}{\sqrt{WL}} \tag{4.41}$$
$$= \frac{3.5}{\sqrt{100}} \tag{4.42}$$
$$= 0.35\ mV \tag{4.43}$$

$A_{V_T} = 3.5$ mV μm. W, L are the dimensions of the device.

The current factor (β) has been modelled as a random variable with standard deviation as

$$\sigma_{\frac{\Delta I}{I}} = \frac{A_{\frac{\Delta I}{I}}}{\sqrt{WL}} \tag{4.44}$$
$$= \frac{1}{100\sqrt{100}} \tag{4.45}$$
$$= \frac{1}{1000} \tag{4.46}$$

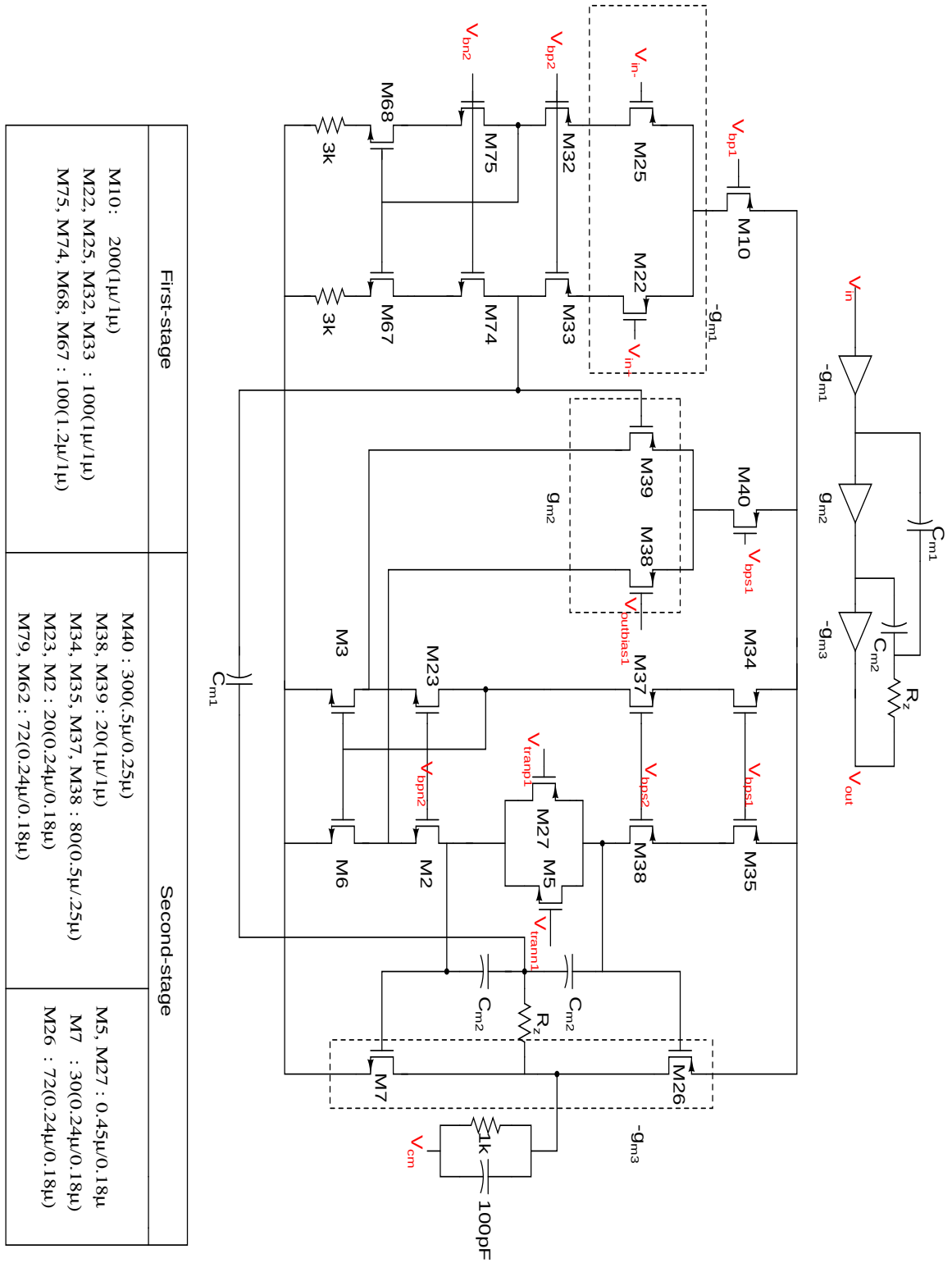
So, the variation in current due to mismatch between the input devices is 0.05 μA. $A_\beta = 1$ %μm. W, L are the dimensions of the device.

Since the first stage gain is very high, the random offsets from the second and

third stage do not contribute to the input referred offset. The input referred random offset is mainly contributed by the input differential pair PMOS transistors.

4.3 Transistor level - Opamp

Thus, the first stage was optimized for noise performance and gain. The output stage was chosen to minimize the quiescent power consumption and to meet distortion specification. The choice of second stage transconductance allows us to decide on the second stage compensation capacitor. The second stage was implemented as a folded cascode opamp with a translinear output stage. A current mirror biasing scheme was followed to bias the operational amplifier. The transistor level circuit with first stage optimized for noise performance and a translinear output stage is given below.



First-stage	Second-stage
M10: 200(1µ/1µ) M22, M25, M32, M33 : 100(1µ/1µ) M75, M74, M68, M67 : 100(1.2µ/1µ)	M40 : 300(.5µ/0.25µ) M38, M39 : 20(1µ/1µ) M34, M35, M37, M38 : 80(0.5µ/.25µ) M23, M2 : 20(0.24µ/0.18µ) M79, M62 : 72(0.24µ/0.18µ)
	M5, M27 : 0.45µ/0.18µ M7 : 30(0.24µ/0.18µ) M26 : 72(0.24µ/0.18µ)

Figure 4.8: Three Stage NMCNR Opamp

CHAPTER 5

Simulation and Layout Results

5.1 Resistor Matching and Distortion

Using resistors of value 10 kΩ and 20 kΩ poly-silicon resistors. Instead of single 20 kΩ resistors two 10 kΩ poly-silicon resistors were used for better matching

Corner	SNR(20 kΩ Resistor)	SNR (2× 10 kΩ Resistor)
typical	85.88	85.88
max	58.2	89.88
min	51.85	85.8

Current variation between 20 kΩ poly-silicon resistor and 2×10 kΩ poly-silicon resistor

Corner	I(Vres=1 V)	I(Vres=1 V)
typical	50.08 μA	50.08 μA
minimum	69.53 μA	71.09 μA
maximum	38.81 μA	38.32 μA

There is a variation of 2.24 % in the current through the minimum resistor and 1.25 % variation in the current through the maximum resistor when compared with the current through the typical resistor. This causes a severe SNR degradation. For Better matching between R and 2R segments two poly resistors of nominal value R is used

5.2 Poly-Silicon resistor, Ideal Switch Ladder

The R-2R DAC was simulated with ideal switches and poly-silicon resistors to determine the best possible SNR. The SNR value was 96.18dB for this case. After introducing MOS switches the SNR degrades to 87.8dB.

5.3 Resistor Distortion

20 kΩ resistors with 2 V_{p-p} sinusoid applied across the resistor

	min	typ	max
Distortion	-82 dB	-80 dB	-84.58 dB

5.4 Harmonic Distortion

The Overlap-Clocks generated higher harmonics compared to non-overlapping clocks. The Non-Overlap clock performance was better than the Overlap-Clock performance for similar bandwidth and slew rate.

Harmonic(1 kHz input)	Overlapping Clock	1 ns Non-Overlapping
2kHz	-87.52	-91.61
3kHz	-102.4	-102.45

5.5 Opamp - macro model results

A macro-model of the opamp with specified unity gain frequency and slew rate was used to arrive upon specifications for the opamp.

Macro-Model	3^{rd} Harmonic	5^{th} Harmonic	2^{nd} Harmonic	Dead-Time
$f_u = 7M, SR = 1V/\mu s$	-104dB	-94dB	-	-
$f_u = 1.75M, SR = 1V/\mu s$	-104dB	-92.4dB	-87.72	900p
$f_u = 7M, SR = 1V/\mu s$	-111dB	-103.4dB	-95.72	500p

5.6 Opamp - Results

The three stage class AB stage operational amplifier was laid out in UMC 0.18μm 6 metal poly technology. The extracted capacitance only netlist was simulated for supply and process variation. The following parameters were considered for the performance of the operational amplifier.

- Open-Loop gain and phase.
- Transient response.
- Positive and negative slew rate.
- Distortion.
- Noise.
- Area.
- Power.

5.6.1 Open-Loop gain and phase

The operational amplifier was simulated in a open-loop configuration with 1kΩ and 100 pF load. The unity gain frequency of the three stage amplifier is 1.76 MHz with a phase margin of 78^o.

5.6.2 Transient Response and Distortion

The operational amplifier was connected in a inverting gain configuration with feedback resistors equal to the ladder resistance. A full swing sinusoid of 0.7 V

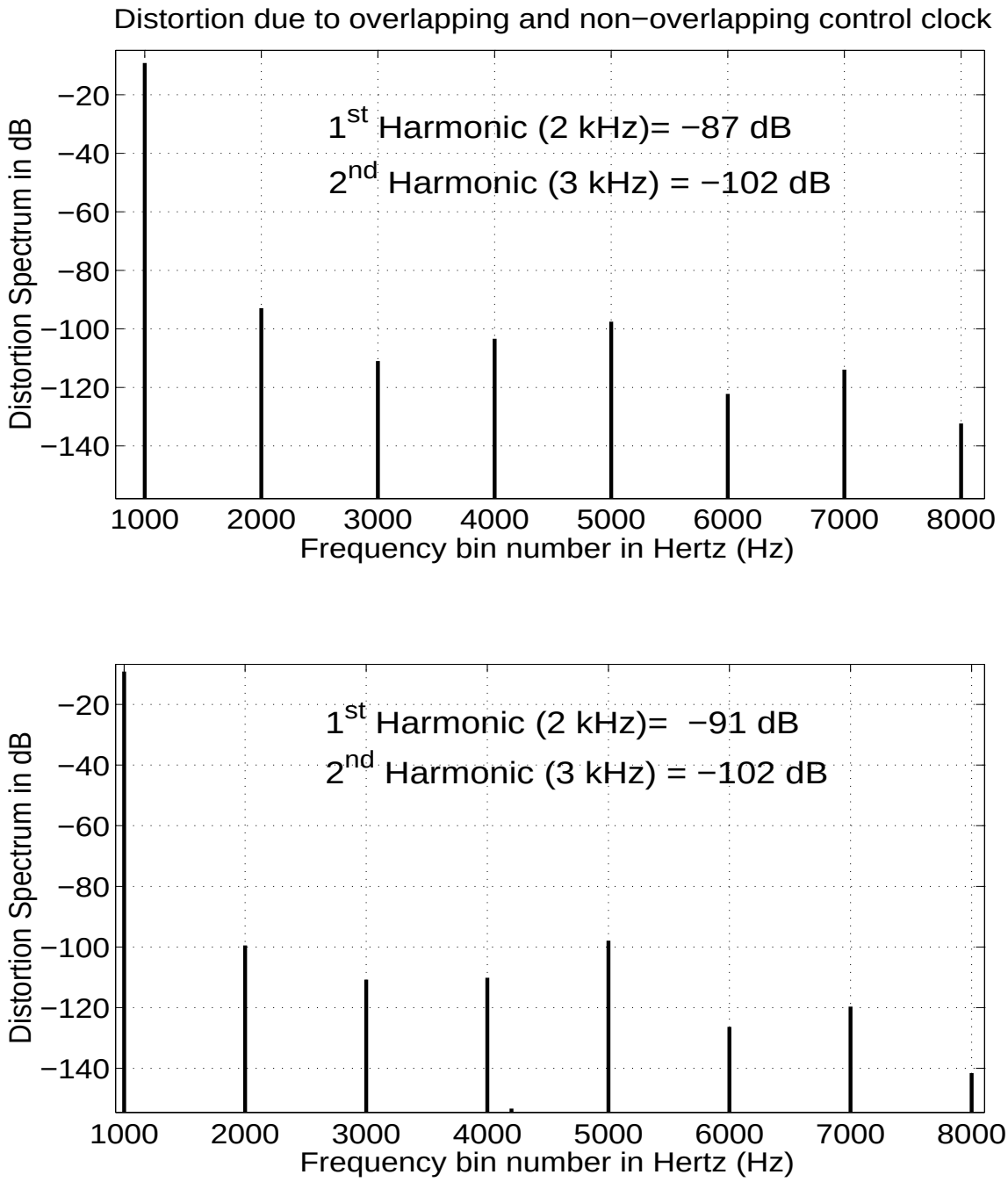


Figure 5.1: Distortion Spectrum of R-2R Ladder, Overlap and Non-Overlap Clocks,$f_{in} = \frac{5}{4096} fs$, fs = 819.2kHz, filtered by 10th Order Butterworth 100kHz cutoff

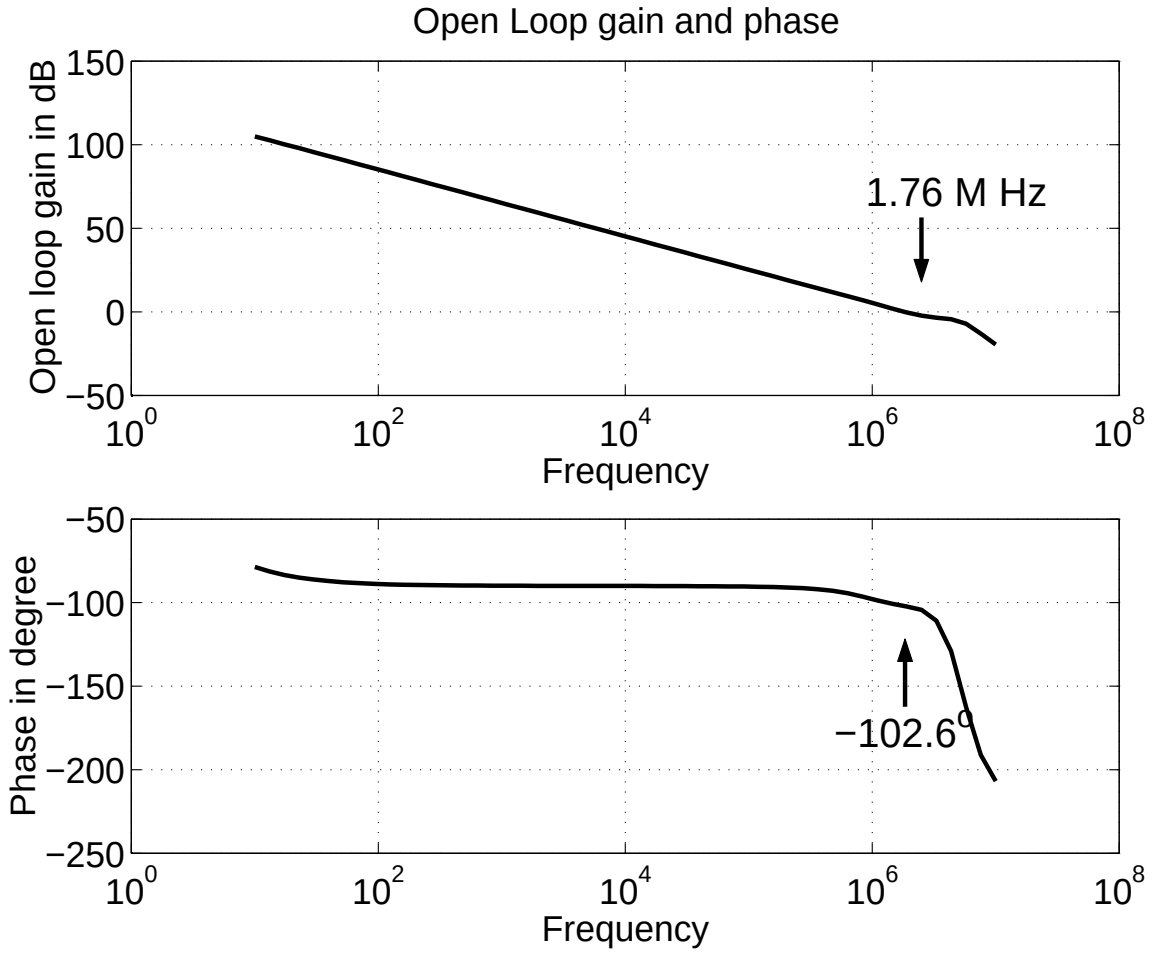


Figure 5.2: Open-Loop gain and phase, UGF=1.76 MHz, PM = 77.2^o

peak at 1 kHz was given as input. The PMOS gate voltage(5.3) drops to supply the necessary current required by the load and the NMOS. During the output negative cycle the NMOS gate voltage increases to sink the necessary current required by the load and the PMOS.

The three transconductance cells are the primary sources of distortion. Since we have chosen class AB architecture for the output stage, the cross over distortion is eliminated. The class AB output stage is the largest contributor to the distortion due to its expanding characteristics. The voltage swing at the input of the first and second transconductors is minimum. Therefore, the first and second transconductors operate in the linear region. By fixing the $\frac{I_{peak}}{I_Q}$, the distortion(5.4) can be adjusted to meet the required specification. As we can observe from the figure(5.5), the quiescent current of NMOS and PMOS is 45 μA . The NMOS sinks the necessary current required by the load and the PMOS and vice verse. When simulated for a 16 Ω load, the gate voltage of the PMOS and NMOS reach the maximum $(V_{gs,bias1} + V_{gs,bias2})$. This gives the limitation for the maximum current supplied by the output stage. The output voltage Vs drain current figure(5.6) clearly shows this phenomenon.

$$I_{peak,NMOS} = I_{Q,PMOS} + I_{peak,load} \tag{5.1}$$

$$I_{peak,PMOS} = I_{Q,NMOS} + I_{peak,load} \tag{5.2}$$

The figure(5.3) shows the transient response and the gate voltage variation.

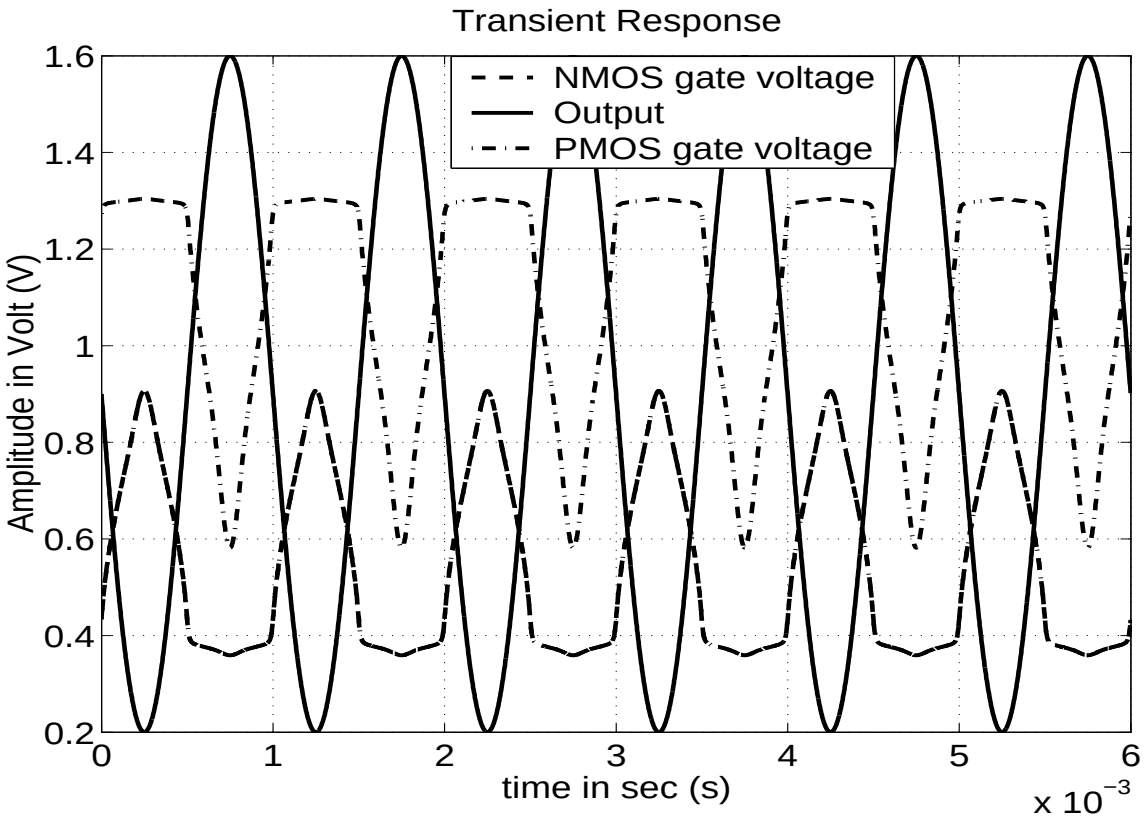


Figure 5.3: Transient Response, Input is 0.5 V RMS, 1 kHz sinusoid

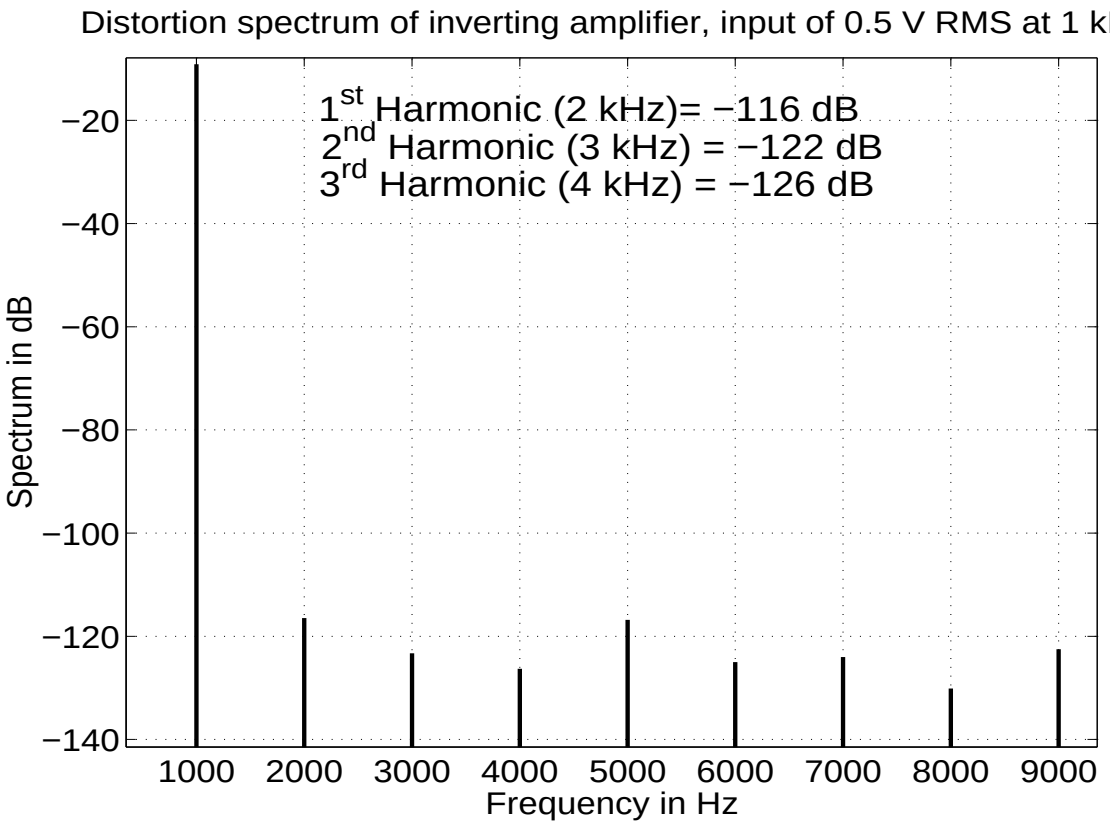


Figure 5.4: Distortion Spectrum, Input is 0.5 V RMS, 1 kHz sinusoid, THD = -96.65 dB

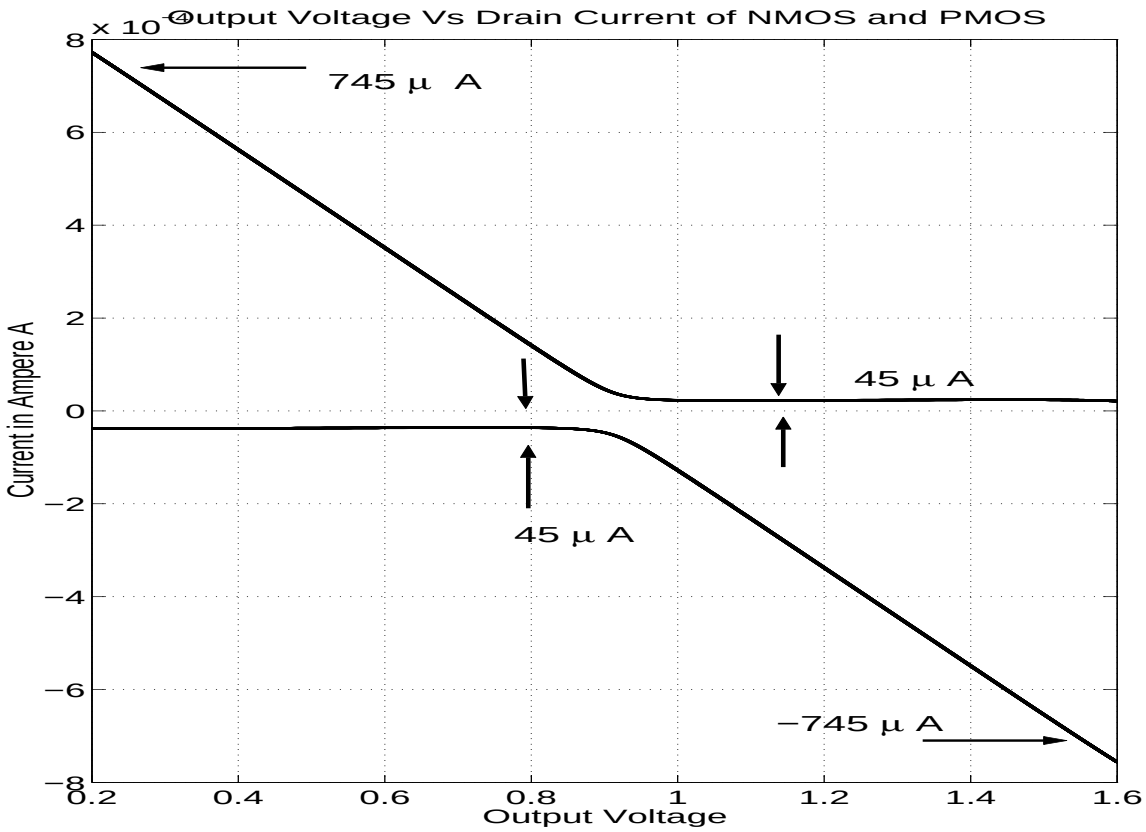


Figure 5.5: Drain current Vs Output Voltage, Input is 0.5 V RMS, 1 kHz sinusoid, 1 kΩ load

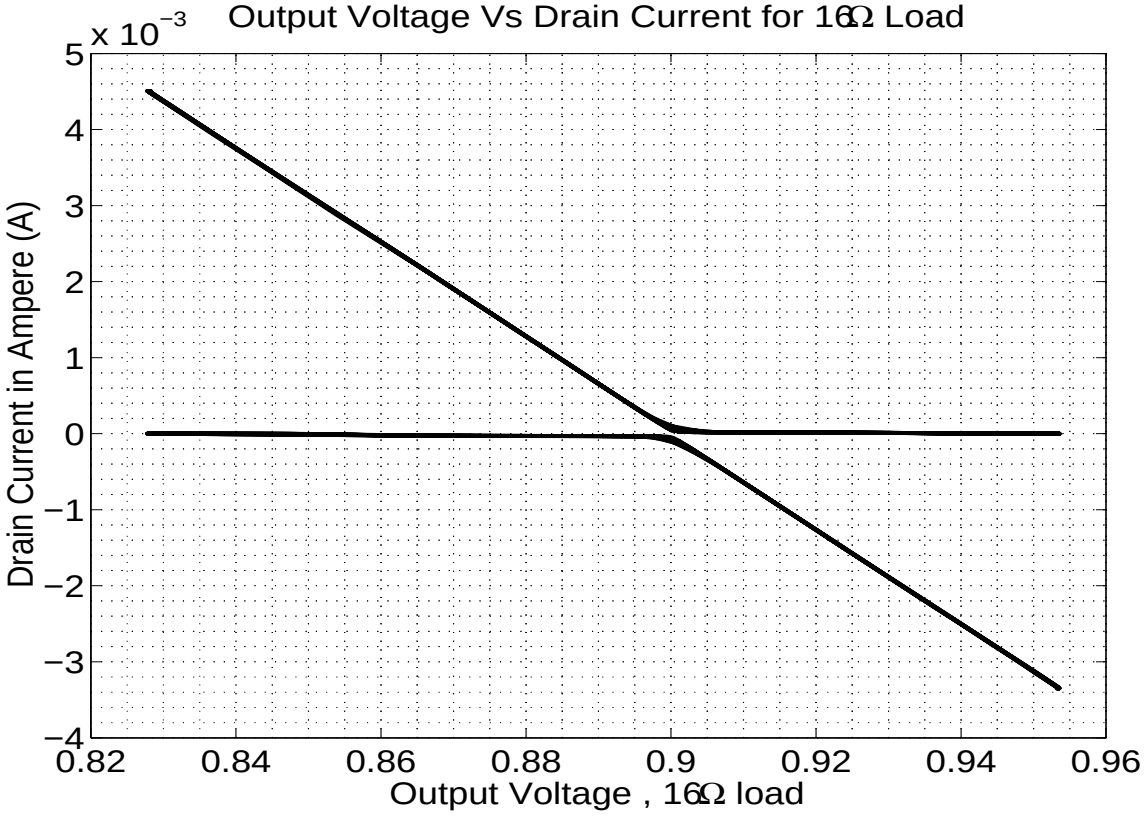


Figure 5.6: Drain current Vs Output Voltage, Input is 0.5 V RMS, 1 kHz sinusoid, 16Ω load

Supply	I_{bias} (μA)	DC-Gain(dB)	PM	Noise(20-20kHz)	V_{th}
1.7	194.1	104.8	64.32^o	1.55μ V	-567.4m V
1.8	189.7	105.7	63.32^o	1.4775μ V	-547m V
1.9	198.5	100.8	65.34^o	2.2μ V	-586m V

Table 5.1: Supply voltage variation

5.7 Process Variation

5.7.1 DC- Bias, Gain, Phase Margin and Integrated Noise

The operational amplifier was simulated for different process corners. At 1.7 V supply, 100^o in combination with ss, tt and ff, the positive output voltage saturates at 1.52 V. The opamp requires a minimum of 150-200 mV overdrive for the output stage PMOS. The table (5.2) lists the specification of the three stage class AB operational amplifier.

Specification	Value
Supply	1.8 V ($\pm$5%)
Loading Condition	100 pF // 1 kΩ
Technology	0.18-μm CMOS
DC-gain	105 dB
Phase Margin	77.4^o
UGF(MHz)	1.76
Output Swing	$0.2 \leq V_{out} \leq 1.6$
Slew Rate	$\pm$ 1 V/μs
THD @ 1 kHz input	-96.65 dB
C_{m1}	50 pF
C_{m2}	1 pF
Power(μW)	349 μW
Total Area	237$\times$297 μm^2 (70389μm^2)
Operational Amplifier Area	10109μm^2
Compensation Capacitance Area	60280μm^2

Table 5.2: Opamp- Specifications

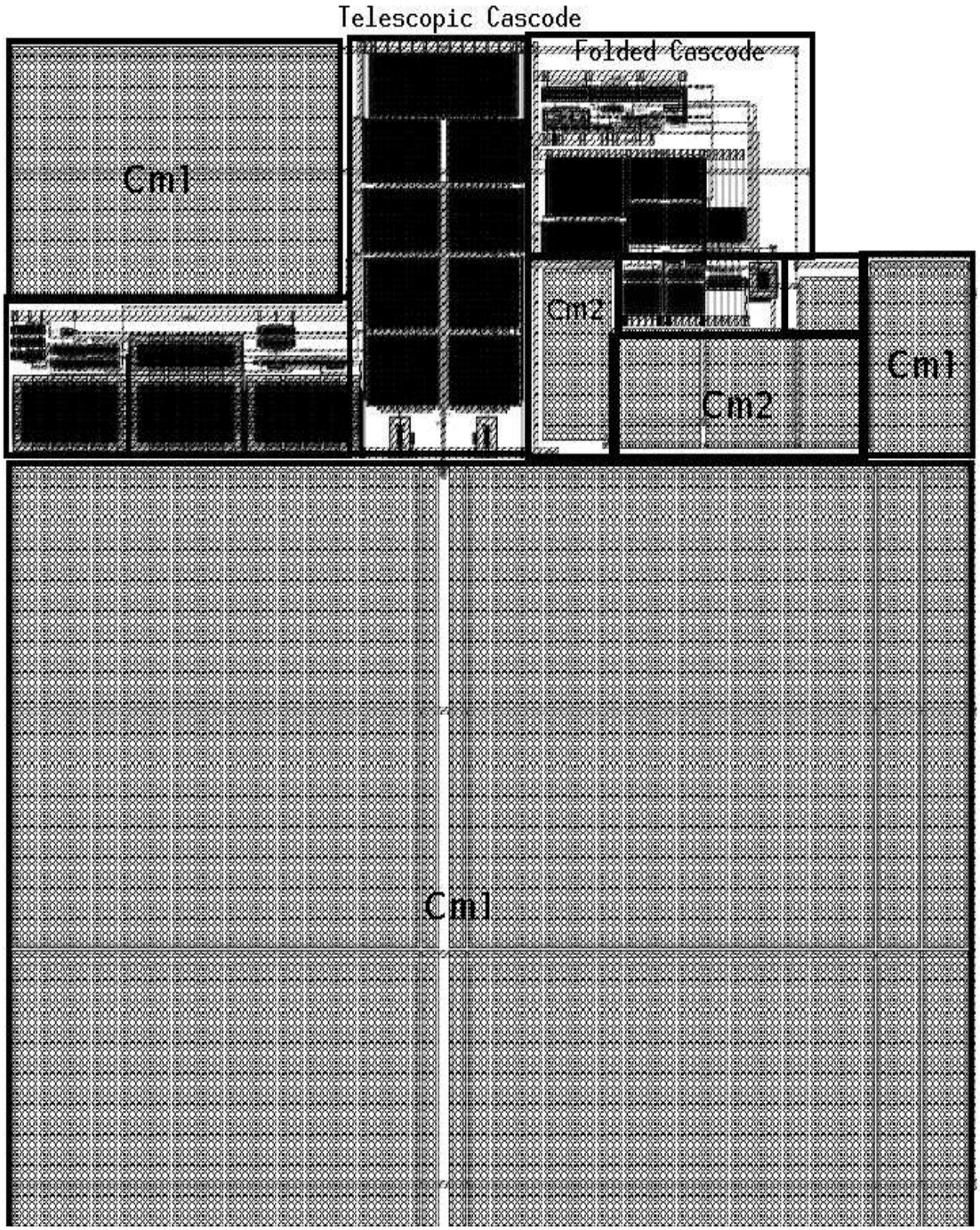


Figure 5.7: NMCNR Layout, width=237μm,height=297μm

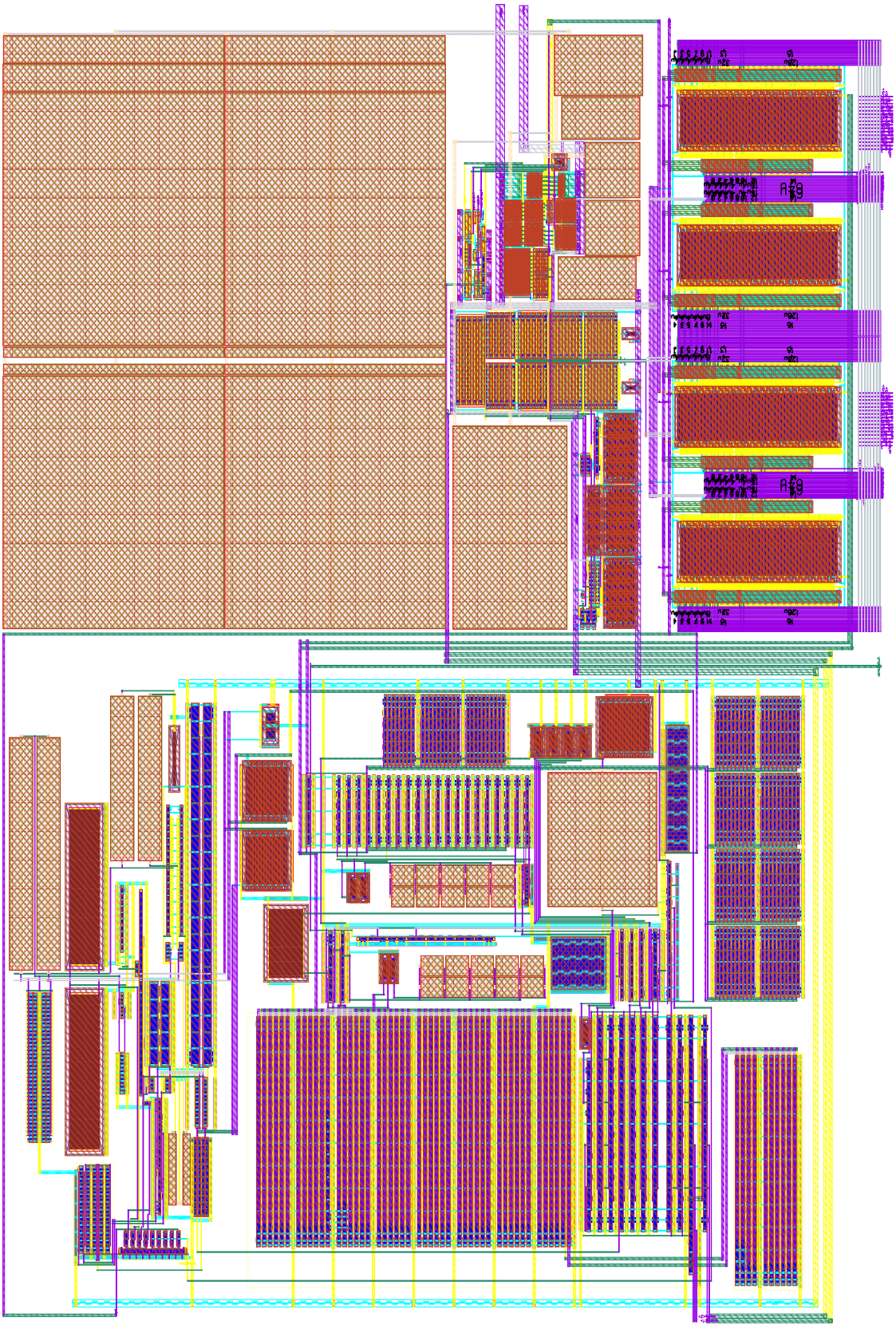


Figure 5.8: R-2R Ladder, Opamp, References, width=515μm,height=419μm

CHAPTER 6

Conclusion and Future Work

The 16bit Digital to Analog Converter was simulated with Resistor Ladder,MOS Switches and Operational Amplifier. The operational amplifier was optimized for noise,power. The Miller Compensation with Nulling Resistor architecture was used to obtain high gain. However, the load capacitance of 100pF required compensation capacitors to be as large as 50pF. The total bias current consumption was 200uA. The bandwdith of the opamp is 1.75MHz. The distortion introduced by the opamp is less than -100dB. The ratio of peak current to the quiescent current controls the distortion.

The extracted RC-netlist of the first stage telescopic opamp has a output offset of 100mV at the quiescent state. However it is within the limits of the input referred offset of 5mV. The integrated input noise of the opamp is 2.1μV. The peak driving current required by the load is 700uA. The feedback resistor and ladder requires a maximum of 70uA. The peak driving capability of the opamp is around 1.1mA.

The translinear stage bias current do not split equally because of the difference in Drain-Source between the bias and the output stage. Other Class AB architectures examined includes reduction of output resistance by a local feedback opamp. The difficulty in this method is the variation of the quiescent current because of the offset error between the two opamps used for feedback.

Other Opamp architectures like current buffer feedback reduces the compensation capacitor value. The compensation capacitor is proportional to square root of the load capacitor in this architecture. However the small signal current buffer implemented should have enough bandwidth. The current buffer technique can be extended as current multiplier which reduces the compensation capacitor size at

the expense of increased power consumption in the feedback mirror. The above operational amplifier was designed for a driver load of 1 kΩ. The output stage can be scaled to modify the driver for a 16 Ω resistor. The sum of the gate-source voltage of the translinear bias is approximately 1.2 V. This can be further increased in addition to the transistor sizes for modifying the operational amplifier. The distortion produced by the operational amplifier is below -100 dB. Hence the output stage quiescent current can be reduced further to optimize for power reduction.

APPENDIX A

APPENDIX

A.1 Quadratic Equation Roots - Approximation

Approximation on Quadratic Equation

$$ax^2 + bx + c = 0 \tag{A.1}$$

When one of the roots is far away from the other the following approximation can be used

$$x_1 + x_2 = -\frac{b}{a} \tag{A.2}$$

$$x_1 x_2 = \frac{c}{a} \tag{A.3}$$

$$x_1 \gg x_2 \Rightarrow x_1 \approx -\frac{b}{a} \tag{A.4}$$

$$\Rightarrow x_2 \approx -\frac{c}{b} \tag{A.5}$$

$$\tag{A.6}$$

A.2 Polynomial - Approximation

Comparing the two expression,

$$\alpha_0 + \alpha_1 s + \alpha_2 s^2 + \alpha_3 s^3 \tag{A.7}$$

$$k_0 \left(1 + \frac{s}{p_1}\right)\left(1 + a_1 s + a_2 s^2\right) \tag{A.8}$$

$$\Rightarrow \alpha_0 = k_0, p_1 = \frac{\alpha_0}{\alpha_1}, a_i = \frac{\alpha_{i+1}}{\alpha_1} \tag{A.9}$$

$$\tag{A.10}$$

A.3 Two Stage Miller Compensation - Complete Expression

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1} \times (g_{m2} - sC_m)}{s^2(C_l C_{gd} + C_{gd} C_m + C_L C_m) + s(C_m(g_{ds} + G_L + g_{m2}) + C_L g_{ds} + C_g G_L) + g_{ds} G_L} \tag{A.11}$$

The poles of the above equation are

$$p_1 = -\frac{C_m(g_{ds} + G_L + g_{m2}) + C_L g_{ds} + C_{gd} G_L}{C_l C_{gd} + C_{gd} C_m + C_L C_m} \approx -\frac{g_{m2}}{C_L} \tag{A.12}$$

$$p_2 = -\frac{g_{ds} G_L}{C_m(g_{ds} + G_L + g_{m2}) + C_L g_{ds} + C_{gd} G_L} \tag{A.13}$$

To Keep the non-dominant pole at twice the unity gain frequency

$$\frac{g_{m1}}{C_m} = \frac{g_{m2}}{2C_L} \tag{A.14}$$

The Phase Margin requirements is

$$\phi_{PM} = 90 - \tan^{-1} \frac{\frac{g_{m1} C_L}{C_m g_{m2}} + \frac{g_{m1}}{g_{m2}}}{1 - \frac{g_{m1}^2 C_L}{g_{m2}^2 C_m}} \tag{A.15}$$

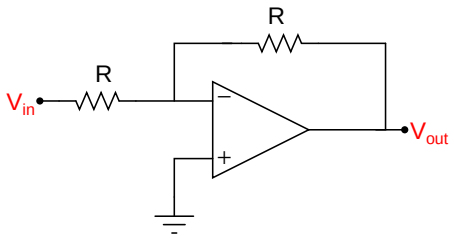


Figure A.1: Inverting Gain Amplifier

A.4 DC Gain and Bandwidth

Consider the opamp with Finite DC gain and single pole

$$A(s) = \frac{A_{dc}}{1+\frac{s}{\omega_d}} \tag{A.16}$$

$$= \frac{1}{\frac{1}{A_{dc}}+\frac{s}{\omega_u}} \tag{A.17}$$

The Inverting Gain Amplifier Solving for Vout

$$V_{out} = \frac{-V_{in}}{1+\frac{2}{A_{dc}}}\left(1-e^{-\frac{\omega_u}{2}\ 1+\frac{2}{A_{dc}}\ t}\right) \tag{A.18}$$

Let us assume that the exponential is insignificant

DC error ,i.e it should settle to a value within 0.1LSB

$$\left|\frac{\frac{V_{ref}}{2}}{1+\frac{2}{A_{dc}}}-\frac{V_{ref}}{2}\right| < 0.1\times\frac{V_{ref}}{2^{16}} \tag{A.19}$$

$$\Rightarrow A_{dc} > 10\times 2^{16} \tag{A.20}$$

Let us ignore the $1+\frac{2}{A_{dc}}$ in the exponential

$$e^{-\frac{\omega_u}{2}t} = 0.01 \tag{A.21}$$

$$\Rightarrow \omega_u = \frac{4ln(10)}{Ts} \tag{A.22}$$

$$\omega_u = 1.76Mrad/s \tag{A.23}$$

Assuming the inverting gain configuration, the input-output relationship is

$$V_{out} = -V_{in}(1 - e^{-\frac{\omega_u}{2}t}) + V_{out}(0)e^{-\frac{\omega_u}{2}t} \tag{A.24}$$

For the output to settle within 0.5LSB.

$$T_s \frac{dV_{in}}{dt} e^{-\frac{\omega_u}{2}t} = \frac{LSB}{2} \tag{A.25}$$

$$\Rightarrow \omega_u = 2f_s ln\left(\frac{LSBf_s}{4A\pi f_{in}}\right) \tag{A.26}$$

where f_{in}, f_s are the input sinusoid and sampling frequency respectively.

This gives $f_u = 14.36$MHz.

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