

Digital Calibration Algorithms for R-2R DACs

A Project Report

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CERTIFICATE

This is to certify that the thesis titled **Digital Calibration Algorithms for R-2R DACs** , submitted by **Manideep Gande**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor and Master of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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I remember my third year very well, when back then all I had for the field of Analog Design was detest. But now, not only has my liking towards Analog taken a complete 180° turn, but also persuaded me to go for higher studies. This dramatic change can be attributed to Dr. Nagendra Krishnapura and Dr. Shanthi Pavan. I don't think I need to say anything more to mention the influence they had on me. I would like to thank Dr. Nagendra once again for his constant encouragement and valuable inputs throughout the project. I would also like to thank for his numerous suggestions not only in academia, but also outside it.

I would like to thank IIT for providing me with some of the most memorable moments of my life and also friends whom I will remember forever.

I would also like to thank my family for the constant support they provided.

On a lighter note, I would like to thank the HRD minister in 2003, Mr. Murali Manohar Joshi, for not having reservations back then.

ABSTRACT

This project involves the development of different digital calibration techniques which could be used to calibrate a 16 bit R-2R ladder DAC. The motivation to develop a 16 bit R-2R DAC over other architectures is driven by the fact that flicker noise is absent in resistors and consequently, the R-2R DAC would need lesser power.

Each of the different digital calibration techniques developed, has its own set of limitations and the final calibration technique implemented is a self calibration technique where the main R-2R ladder (16-bit) is calibrated with the help of auxiliary R-2R ladders (each of 11-bits). This project involves the development of a high performance comparator which would be able to detect voltage differences in the order of microvolts. The project also includes the implementation of the calibration algorithm in Verilog so that it could be synthesized to give the layout of the digital part.

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ABBREVIATIONS

LSB	Least Significant Bit
INL	Integral Non-Linearity
DNL	Dynamic Non-Linearity
LRST	Latch Reset

CHAPTER 1

Introduction

1.1 Motivation

Digital to Analog Converters, familiarly known as DACs are used in virtually every modern electronic system. The necessity for them is because all real world signals are invariably analog and this is where digital to analog converters come into the picture. They convert digital numbers into a physical quantity, usually a voltage. For example, most audio signals are stored in digital form and in order to listen through speakers, one would need to convert them into analog signals using a DAC. Therefore one would find a DAC digital music players, sound cards etc...

1.2 R-2R DAC

The most simplest of all DACs is the R-2R DAC. The R-2R DAC works on the principle that the resistance looking in at any node is equal to $2R$ in both the directions. This concept is shown in the figure [1.1](#)

Since the resistance looking in at any node is equal to $2R$ in either directions, the current would split equally in both of them, thereby giving the binary division of the current as required by a DAC.

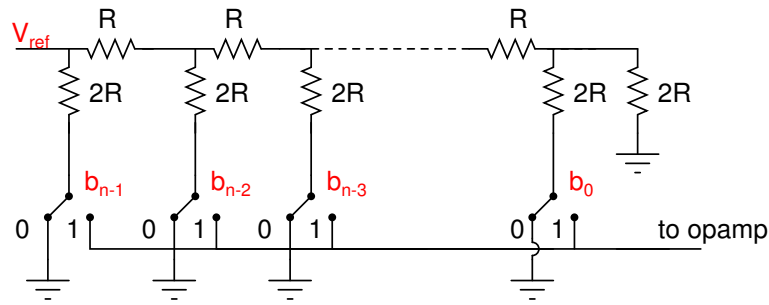


Figure 1.1: Ladder Structure

An important point to be noted in this case is that the current division occurs perfectly if and only if the resistances looking into both the directions is equal to $2R$. If this is not the case, the whole purpose is defeated and hence the DAC ceases to operate as it is expected to.

1.3 Measure of Performance of a DAC

The fact that practical DACs output a sequence of piecewise constant values or rectangular pulses, means that there is an inherent loss of data in a DAC. Therefore a DAC is characterized by how finely it can resolve the output. In other words, the resolution of the DAC tells you how good the DAC is. Therefore, higher the resolution, the better is the performance.

Apart from the resolution of the DAC, two other important performances of merit for a DAC are INL and DNL. For a DAC to work as expected, one would need $|INL| \leq 0.5LSB$ and $|DNL| \leq 1LSB$. Both INL and DNL are discussed in detail in [A](#).

CHAPTER 2

Digital Calibration

2.1 Existing DAC architectures

2.1.1 R-2R DAC

Different topologies of DAC have been proposed and R-2R DAC architectures are also available. Since the problem in high resolution R-2R DAC is the accuracy of resistors, different architectures deal with it in different fashions. In (1), the inaccuracies in the resistors are taken care of by modifying the vertical resistance (i.e 2R). Another variation of the regular R-2R ladder is presented in (2). In some of the other architectures, the resistances are replaced with MOSFET's (3) and the ladder is then calibrated.

2.1.2 Current Source Based DAC

A current source based DAC works on the principle of equal current sources being switched on/off depending on the input bit sequence (4). The following circuit shows implementation of a current source DAC.

It consists of an array of current sources, all delivering the same output current. To increase the resolution, one of the coarse currents is further divided using passive

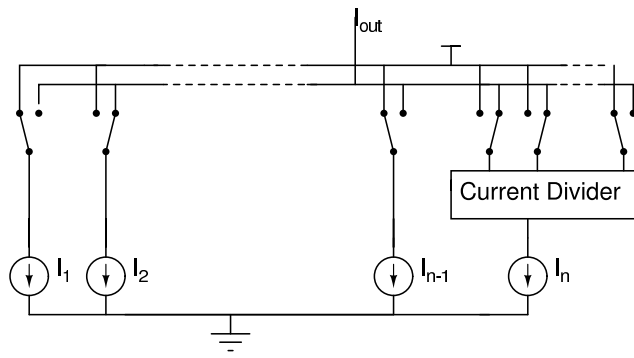


Figure 2.1: Basic circuit diagram for a current dividing DAC

current divider as shown in the figure. Depending on the input, the current sources are correspondingly connected to the output terminal I_{out} .

In practice, the current sources are implemented using MOSFET's as shown below :

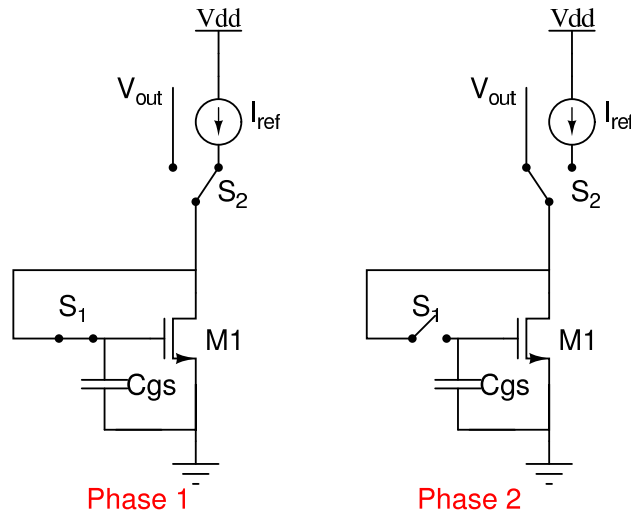


Figure 2.2: Calibrating current sources

Initially, all the MOSFET's are calibrated to carry the same currents I_{ref} . But

since the switches S_1 and S_2 are MOS transistors and when S_1 is switched off, its channel charge q_{ch} is partly dumped on the gate of M1. Therefore, we would have $\Delta V_{gs,q} = \frac{q_{ch}}{C_{gs}}$. Another problem arising due to this architecture is that, even though the switch is turned off, the reverse-biased diode D, between its source and the substrate is still present. Therefore, we would have a current leakage and hence a drop in the voltage which is given by $V_{gs,leak} = V_{gs}(0) - \frac{I_{leak}}{C_{gs}}t$. All these effects change the voltage V_{gs} , which would thereby change the reference current. Therefore and hence limit the operation of a current steering DAC. The only solution to this problem is to continuously keep replenishing the charge so that V_{gs} remains constant. But as the resolution keeps increasing, this becomes more and more difficult.

Modern approaches for current steering DACs is presented in (5), where a 14-bit DAC is proposed, which uses the help of an external 16-bit ADC for calibrating purposes.

2.2 Resistive Ladder DAC

2.2.1 Need for Calibration

As mentioned earlier, the working of an R-2R DAC very much depends on the accuracy of the resistors available. On an IC, obtaining resistors beyond a particular accuracy is impossible. So in order to avoid the inaccuracies present in the resistors available one needs to look to various means for calibration. For example : The typical values of the mean of variation i.e. $\sigma(\frac{\Delta R}{R})$ is 0.01. These resistors when used

to build the DAC without calibration give an INL of upto 200 LSB. This can be seen in the following graph :

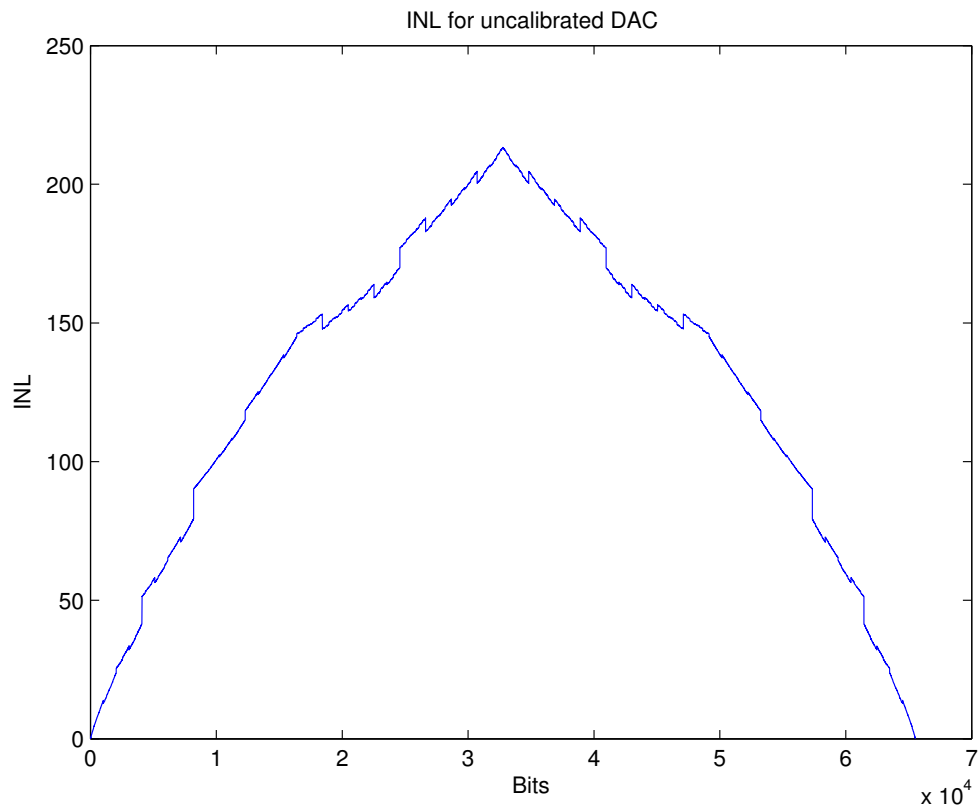


Figure 2.3: RMS of INL for a uncalibrated R-2R DAC

The above figure gives the rms value of INL for an uncalibrated DAC which is averaged over 50 cases. The INL plot shows that the DAC fails to function as required in the absence of calibration, as the INL is required to be less than 0.5 LSB for DAC to work as intended.

The table shown below gives the average value of rms value of INL for different values of $\sigma(\frac{\Delta R}{R})$.

$\sigma(\frac{\Delta R}{R})$	0	0.0025	0.05	0.01	0.02
Max. INL_{rms}	0	0.0025	0.05	0.01	0.02

2.3 Calibration Scheme

2.3.1 Modified R-2R Ladder

The modified R-2R ladder has the following structure

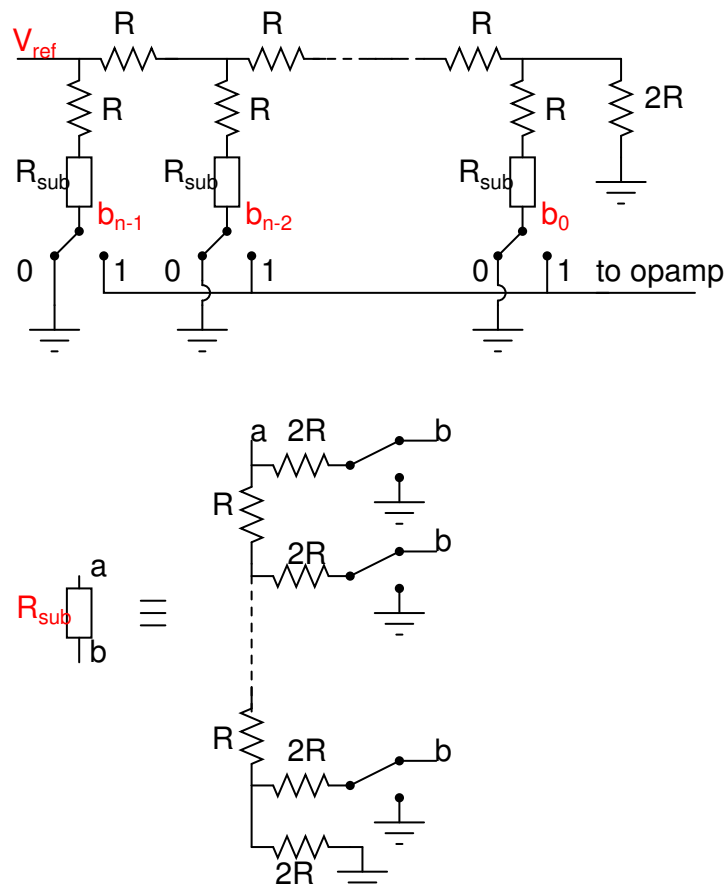


Figure 2.4: Modified DAC structure

The above structure is very similar to the regular R-2R ladder wherein each of the 2R resistors is divided into two parts, a resistor R and an R-2R ladder (R_{sub})

connected in series. The structure of R_{sub} is shown in 2.4. It is an R-2R DAC in itself, and depending on the bits b_i , the branches would be either connected to ground or the opamp. Note that the resistance looking into the vertical branch is still $2R$ and is independent of whether a branch is connected to the ground or to opamp terminal. The advantage of the above structure is that it would help us modifying the amount of current that would flow into the opamp, thereby giving us an opportunity to calibrate the current flowing in a branch. Moreover, the resolution of the subtree can be varied depending upon the accuracy needed, and in this case a resolution of 16 bits was used for R_{sub} .

2.3.2 External Calibration Technique

For the calibration scheme to work, we should have a means of reducing or increasing the current flowing from a branch into the opamp. In order to have such an option, the following technique is used. Consider a particular branch b_i which is being calibrated. Now if we had only this branch being turned on, the current flowing into the opamp would be $b_i \times I_{lsb}$. In the modified scheme of things, the system is initially set up such that if all the resistors used were ideal, then only $31/32$ times the required ideal current would be flowing into the opamp, i.e in this case only $31/32 \times b_i \times I_{lsb}$ would be flowing into the opamp. Therefore, if we had the input digital bits to be ‘X’, then using the above calibration technique, only $31/32 \times XLSB$ current would be flowing into the opamp if all the resistors were ideal. In order to ensure that only $31/32$ times the original current would flow into the opamp, all we need to do is to have the first five bits of the subtree be turned on, i.e. have the first

5 bits of the subtree to be connected to the opamp and the remaining to ground.

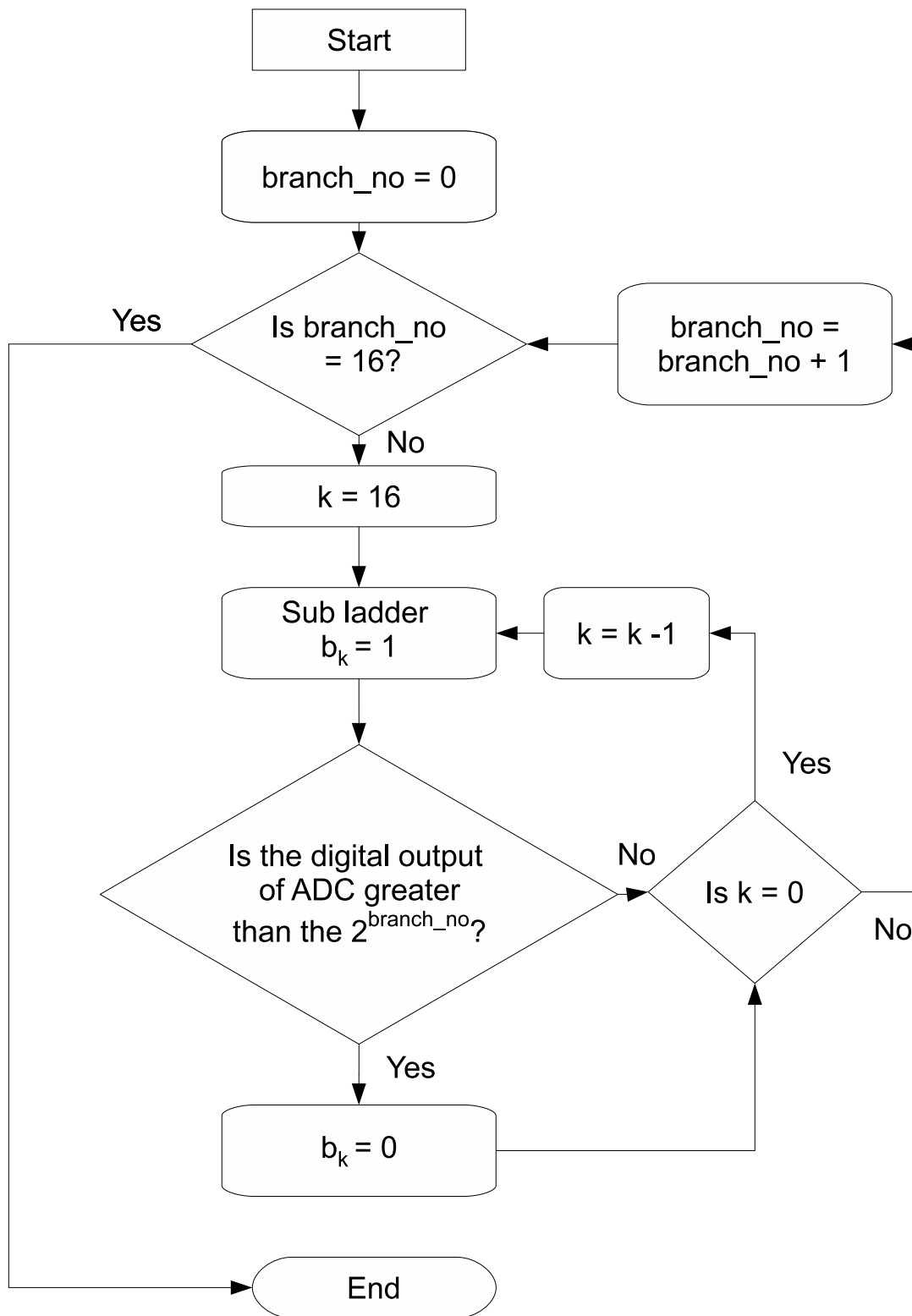
The above step is necessary as that would give us room to both increase and decrease the current flowing through a branch. For example, assume that the above measure was not taken. In some cases, it may turn out that the current flowing into the branch may be lower the ideal value. If this is the case, then even having all the branches of the sub ladder turned on would not help because the current flowing into the ladder is in itself lesser than the required value. Now since the current flowing into the opamp due to a particular branch is lesser than the required value, we would have the INL of the system going for a toss. Therefore, by having the LSB $31/32$ times the original, we in practice have an option which enables us to add current and also decrease it. The number $31/32$ was chosen so that the variations in the MSB bits of the subtree would be minimal and therefore it would lead to more system stability.

Since the resistors used in practice are not ideal, the bits turned on in a subtree would need to be modified for each branch, so that we get the required output current. This is done by using the following calibration algorithm.

- Take the first branch to be calibrated and turn that on while keeping the rest of the bits off i.e. say, b_{N-1} is '1' and the rest of them are equal to '0'.
- Ideally, the current into the opamp due to this branch would be $\frac{31}{32} \times 2^{N-1} \times LSB$.
- In order to get the value close to the ideal value, the algorithm works such that in the first step, only the first bit (i.e. the MSB bit) of the subtree is turned on. Therefore, the total current flowing into the opamp would now be

$I_{b_{(N-1)}} \times 0.5$. This is because, we have only the MSB bit of the subtree being turned on.

- Now the output is passed through an 18 - bit ADC at the output. If this digital output (when accordingly scaled i.e. divided by 4 since an 18-bit ADC is used) is greater than 2^{N-1} then this bit is completely turned off, else it is turned on. This is because the output greater than 2^{N-1} would mean that the current flowing into the opamp is more than the required amount. This bit will now remain on/off, (depending on whether or not it met the requirements), throughout the rest of the calibration for the branch.
- After configuring the first bit of the subtree, we proceed to the next bits in the fashion similar to the one mentioned above. This process is continued till the output of the ADC matches with 2^{N-1} . And once this condition is reached, further restrictions are imposed using the final 2 bits of the 18bit DAC.
- The last 2 bits of the ADC are used to fine tune the value of the current flowing out so that we can be sure that error in the current value is less than 0.25 LSB. The approach used is similar to the one mentioned above, but keeping in mind not to change the distribution required to receive the correct value of the current i.e. $2^{N-1} \times LSB$.
- Once the value of current for the first branch is dealt with, we move on to the subsequent branches and do the matching in the similar way i.e. keep only that particular branch on while keeping the rest off.



2.4 Problem with the above approach

In the above approach, the current from a particular branch was being calibrated by either turning the bits of the subtree on/off. In this case, there was a possibility that the required current could not be attained by a particular subtree. The reasons for this could be attributed to the following

- If the extra current introduced when a switch of a subtree is turned on increases the value of ADC output to more than 2^{k-1} (where k is the subtree number), that would mean that the bit of the subtree would be turned off.
- As a result, we need to switch on the lower switches and see to it that the required current of 2^{k-2} is flowing.
- But in some cases, it turned out that if a switch overshoot the required value marginally, and hence would be turned off. Therefore, ideally we would expect the lower switches to add the required current. But it turns out that in some cases, the lower switches, even with all of the being turned on, could not accumulate the difference required current. Therefore we would have this subtree not working and hence our purpose is defied.
- This particular phenomenon was increasingly observed as the value of σ increased. With $\sigma = 0.05$, the following graph for INL was obtained when averaged out for 50 cases
- Clearly, as seen in figure 2.5, the INL is greater than 50 LSB, which shows that the algorithm is not suitable for large values of σ .

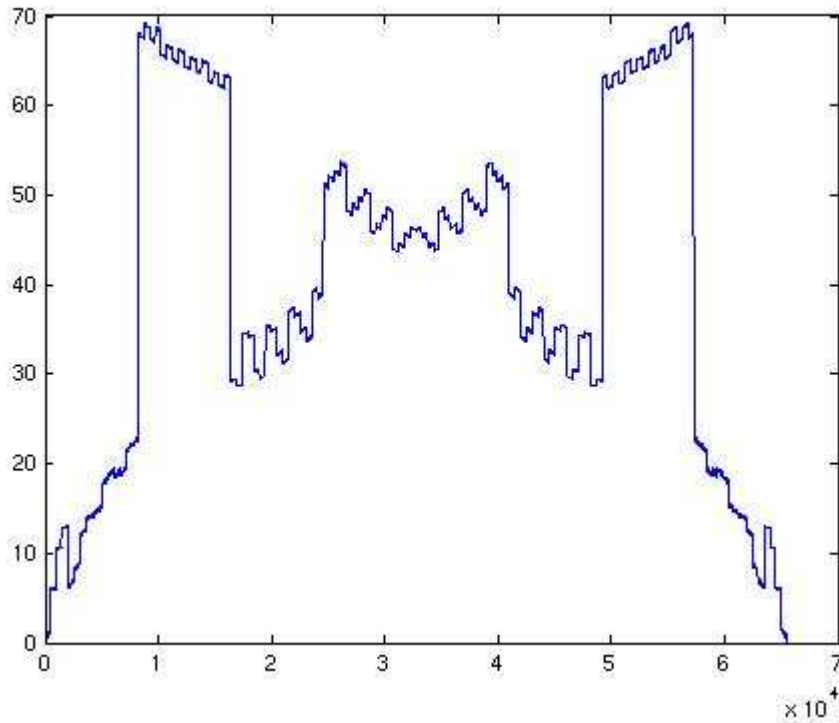


Figure 2.5: INL for 50 cases with $\sigma = 0.05$

2.5 Modified Approach

The above situation could be avoided with the help of a slight modification. This modification, which comes at the cost of few extra resources, is discussed below.

- In the previous case, it is always possible to catch the error i.e. we could precisely know which subtree is causing the error and thereby is not calibrated.
- Now apart from the main ladder, I also use an alternative simple R-2R ladder of 16 bit resolution. Using the above knowledge, whenever a error is caught we could turn on the corresponding switch on the auxiliary R-2R (for this branch alone) and using this extra current the calibration process is repeated once again. If this particular one also fails(which is rare), we move on to the next branch of the simple of the auxiliary R-2R ladder

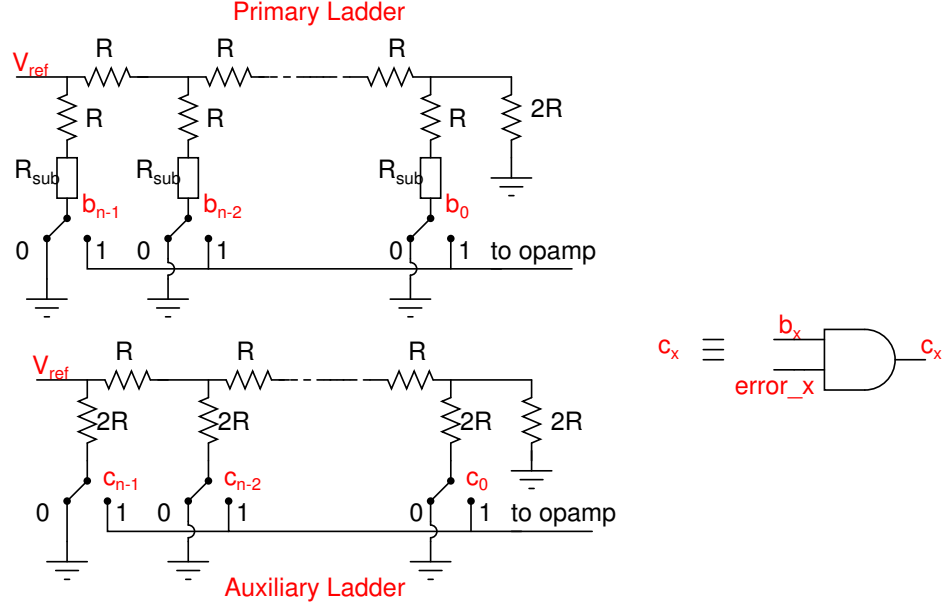


Figure 2.6: Modified ladder

- The results obtained using this algorithm show a great improvement over the previous case and can be seen in figure 2.7

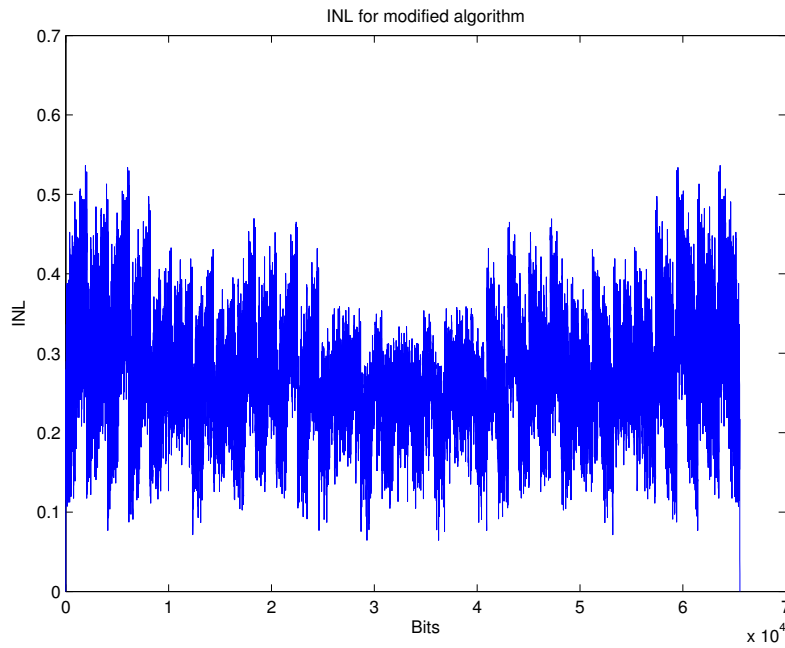


Figure 2.7: INL for 50 cases with $\sigma = 0.05$

The zoomed in version of the above plot is shown in the following figure :

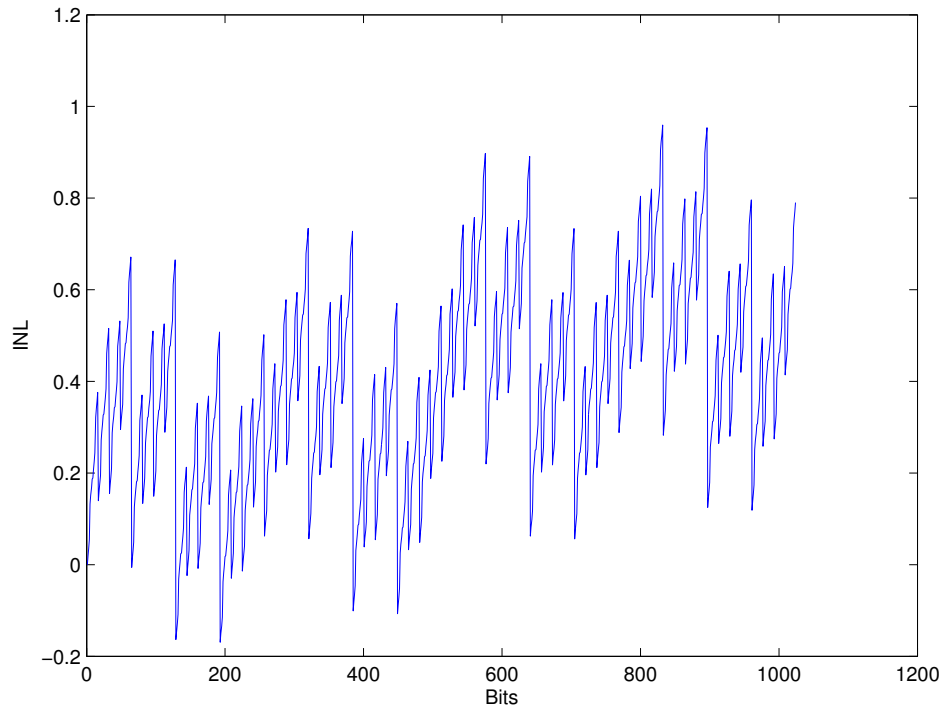


Figure 2.8: Zoomed picture of INL

NOTE : The above plots were obtained using ideal ADC

It is observed that the number of error signals caught is "0" for most cases with $\sigma \leq 0.01$ and less than 3 for $\sigma \leq 0.05$

Building of 18 bit ADC

The 18 bit ADC used for calibration is realized using a $\Delta\Sigma$ modulator which has the following specifications :

- Order = 3
- OSR =64
- Out of band gain = 1.5

- Number of levels of the quantizer = 16

The bit sequence from the modulator was then decimated, (low pass filtered using a 8th order FIR type 1 chebyshev filter and then followed by down sampling), by 64. The SNR obtained using the above modulator for a small frequency sinusoid was close to 120dB.

2.6 Results

2.6.1 Timing Requirements

The number of samples used for $\Delta\Sigma$ modulator to settle to the final value was 4096 points. These points would be feeded at the over sampled rate. In the worst case, we would need each and every branch of every subtree to be calibrated, which would mean that we could possibly need 256 such cycles. Therefore the worst case time required would be $\frac{4096 \times 256}{64 \times 48kHz} \approx 0.4s$.

2.6.2 INL

The following plot shows the INL (taken on an average for 10 cases) using all the above mentioned features. The sigma of the resistors used for the following simulation was equal to 0.05.

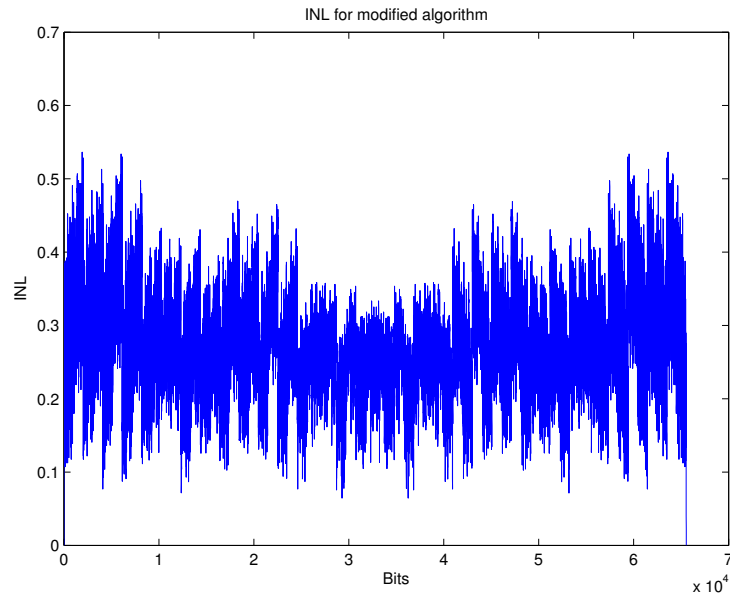


Figure 2.9: INL for $\sigma = 0.05$

2.7 Drawbacks

The above external calibration scheme has a few drawbacks.

- The number of resistors used up in this architecture is huge. This is because each of the sub ladder would consist of 16 resistors. Therefore, the total area used up would be extremely large.
- The number of switches used in the present algorithm is > 250 .
- This number can be reduced to around 200 by assuming that the lower bits would not need detailed calibrations.
- The presence of external device to aid in calibration (in this case, the 18 bit $\Delta\Sigma$ ADC) only complicates things.

The above mentioned drawbacks could be avoided using a self-calibration approach discussed in the next chapter.

CHAPTER 3

Self Calibration Approach

3.1 Differential DAC

In a simple single ended implementation of a DAC (see figure 1.1), if the input common mode voltage is chosen to be V_{cm} , then we could swing the voltage only in one direction. This is because we could either pump in or pump out current into the opamp terminal and could not do both the operations simultaneously. This would limit the voltage swing at the output and hence is a bad implementation of the design. To overcome this problem, the following DAC architecture could be used.

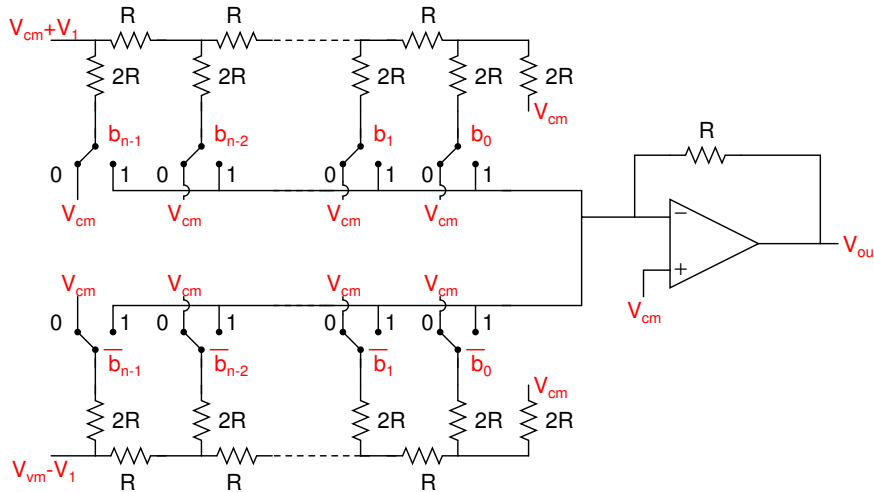


Figure 3.1: Differential like implementation of DAC

The differential ladder overcomes the problem of limited swing direction by having two ladders as shown. The bits fed for the top ladder and the bits fed

for the bottom ladder are complementary. Therefore, the total current flowing into the output terminal would be $D_{in} \times LSB_{top} - (2^N - 1 - D_{in}) \times LSB_{bottom} = D_{in} \times (LSB_{top} + LSB_{bottom}) - (2^N - 1)LSB_{bottom}$

Therefore, in this case, we could swing the voltage on both sides of V_{cm} i.e. for $b_{16} = 0$, we would have the output less than V_{cm} and for $b_{16} = 1$, we would have the output greater than V_{cm} . Note that the LSB of the corresponding differential ladder would be $LSB_{top} + LSB_{bottom}$ and the range of the voltage swing would be from $V_{cm} - V_1$ to $V_{cm} + V_1$

3.2 Self Calibration Approach

3.2.1 Implementation Technique

In this approach, you use the left over current for calibration. The left over current is the current in the last unused branch, and it is shown in the following figure :

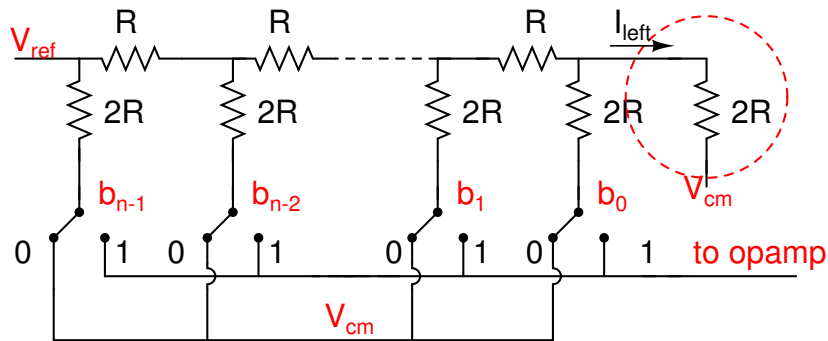


Figure 3.2: I_{left} in an R-2R DAC

For the purpose of calibration, you make sure that the current

$$I_{bn} = \sum_{0 \leq i \leq n-1} I_{bi} + I_{left}$$

where I_{bi} is the current in the branch whose bit value is i and I_{left} is the current in the last unused branch. That is to say, we make sure that the current in a particular branch is equal to the sum of the currents of the previous branches, which would therefore give us the following equations

$$I_0 = I_{left}$$

$$I_1 = I_0 + I_{left}$$

...

$$I_{15} = I_{14} + \dots + I_0 + I_{left}$$

The above current equations are realized by adding appropriate current sources, whose value is equal to the difference between the branch current and the ideal current. The difference current is added using a correction current source for each bit

In order to reduce the number of current sources required for calibration, one can avoid calibrating the lower branches, as the error in the lower bit branches turns out to be very small. This is also supported by the fact that the building of small current sources (of the order of nano amperes) is difficult and cumbersome. Moreover, it can be noted that the calibration need not be done separately the

top and bottom branches separately. This is because, while calibrating one of the branches, say the top, we are also taking into account the inaccuracies of the bottom ladder. Therefore, in effect we need to calibrate very few branches thereby reducing the area requirements. The following graph shows the performance of such a DAC calibrated using the above mentioned logic, wherein the bottom 8 branches are left uncalibrated and only the top ladder is calibrated:

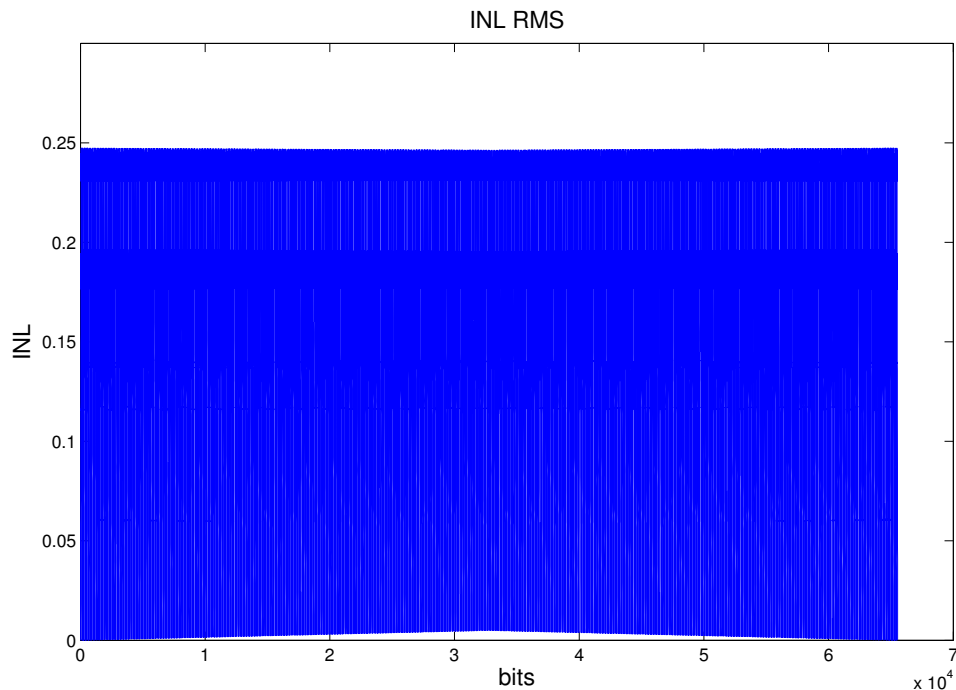


Figure 3.3: differential like implementation of DAC

The realization of the current comparison and the implementation issues are dealt with in Chapter 5.

3.3 Modification to the above algorithm

3.3.1 Sub-Nano Ampere Current Sources

The performance of the above circuit depends very much on how small a current source can be built. This is because the above technique works on the principle of adding the difference current. Therefore, the smaller the current sources available, the higher would be the performance of the circuit as it would enable us to get difference between the current values to as low as possible. For example: if we are able to build current sources of the order of 0.25 LSB, then that would mean we cannot achieve an accuracy below 0.25 LSB. Similarly if we only had current sources of the order of 1 LSB, then that would mean the accuracy achieved could not be better than 1 LSB.

In the R-2R ladder built, to meet the noise and the distortion specifications on the opamp, the value of the resistors used were $20k\Omega$. And the output voltage swing limit available is 1.4 V. Therefore, that would mean that the LSB current would be :

$$I_{lsb} = \frac{1.4}{2^{16} \times 20k\Omega} \approx 1nA$$

The above value of I_{lsb} means that to have current sources of accuracy 0.25 LSB, one would need to build current sources of the order of 0.25 nA. This order of accuracy is possible to achieve (6), but it comes at the cost of large area and is difficult to implement, thus making it impractical for this algorithm.

3.3.2 R-2R Sub Ladder

As discussed above, the problem with this architecture is limited by how low and accurate a current source one can build. Moreover, in the above ladder, to calibrate a particular branch, we need to supply all the error current. The worst case deviation of current in a particular branch could be as high as

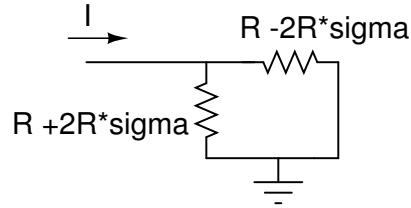


Figure 3.4: differential like implementation of DAC

This implies we not only need to build current sources of small values, but we also need to build current sources of large values to take into account the errors in the branch current. It is important to note that the current sources need to be accurate, otherwise they themselves would cause non-linearity and thereby increase INL. Therefore, to avoid the above methodology, a new architecture is discussed.

In this architecture, we calibrate the main ladder using another R-2R ladder. The logic for this calibration goes in a similar fashion as discussed in 2.3.2. The steps of working of the algorithm are mentioned below:

- For the first step, consider only the branch being calibrated. Let the branch being calibrated be 'i'. Therefore as discussed in the above algorithm, we need to compare the currents I_i & $\sum_{0 \leq i \leq n-1} I_{bi} + I_{left}$.
- For calibrating this current, we need to add some current to the current of the branch 'i'. For this, the algorithm works such that in the first step,

only the first bit of the subtree is turned on. Now the the currents $I_i + I_{subtree}$ & $\sum_{0 \leq i \leq n-1} I_{bi} + I_{left}$ are compared.

- If the current added by the subtree makes the current of the branch more than the latter, this branch of the subtree is turned off and we move on to the next branch of the subtree and so on...
- These steps are done till all the branches of the subtree are checked for, and in the end we would find the bits of the subtree that need to be turned on for each particular branch.
- The above series of steps is repeated for all the branches and for each and every branch being calibrated, the amount of current added by the subladder is stored in memory.
- Therefore, when the input data comes in, the current supplied by the subladder would be equal to the sum of the currents needed by all the branches which would be turned on.
- For example : If a current of $10I_{lsb}$ was needed by branch b_5 and a current of $15 I_{lsb}$ was needed by the branch b_6 , then when the input binary data is 110000, a total current of $25 I_{lsb}$ will be added by the sub ladder.

The above algorithm is shown in the form of a flow chart in figure [3.5](#)

In the flow chart shown, the variable ‘branch_no stands’ for the branch which is being calibrated. ‘k’ stands for the resolution of the sub-ladder.

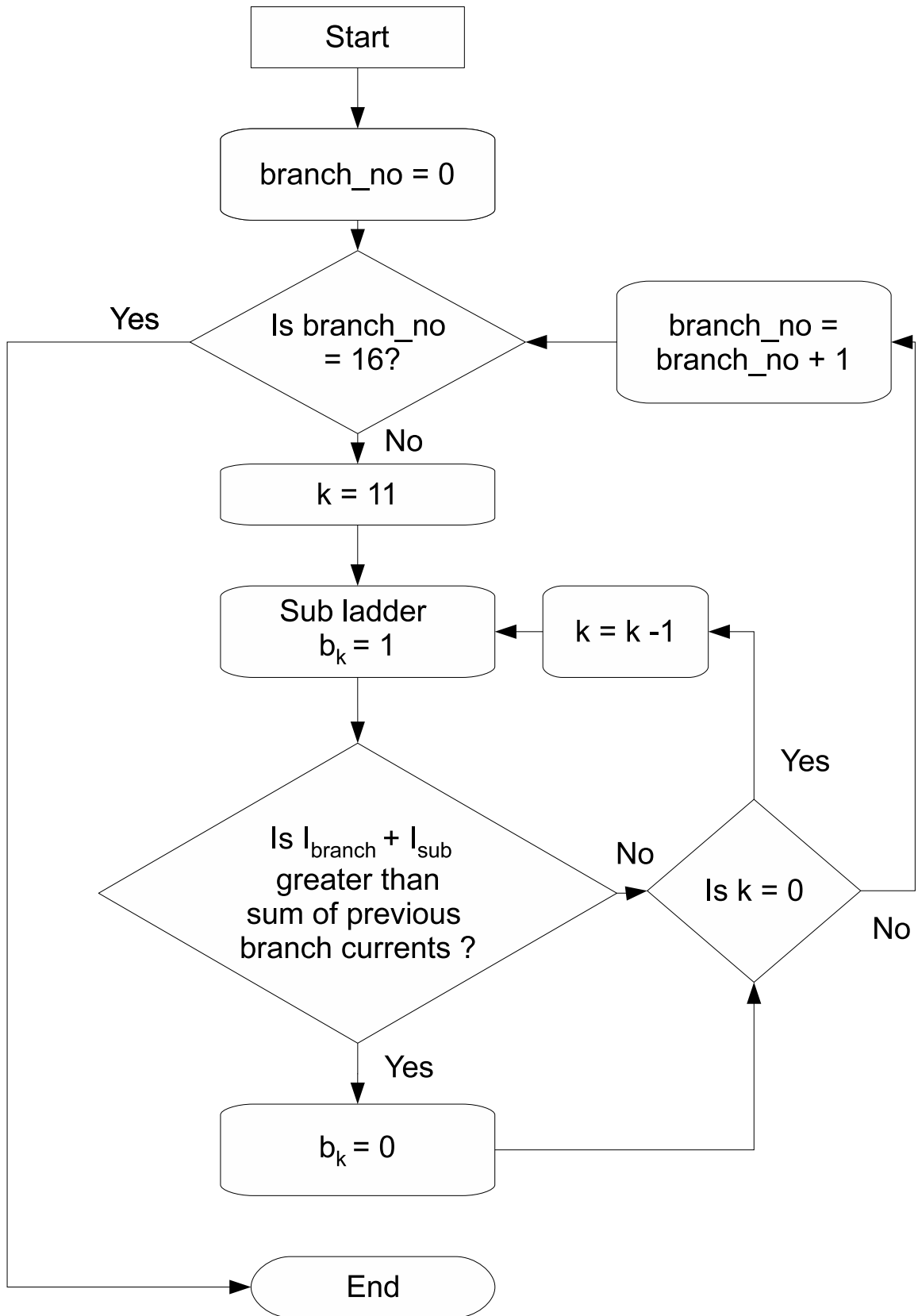


Figure 3.5: Flow chart of algorithm used

3.3.3 Non Linearity of the Sub Ladder

Since the sub ladder being used is also an R-2R ladder, and since the resistors used are not ideal, the sub ladder used would also be non linear. This has a very big influence on the calibration scheme because when an input bit pattern arrives the current added by the sub ladder is equal to the sum of the needed by all the branches that would be turned on. Therefore, if the calibrating DAC is non-linear, then the current being added would not be linear, thereby defeating the whole purpose. Consider the example discussed above where in $10I_{lsb}$ was needed by branch b_5 and a current of $15 I_{lsb}$ was needed by the branch b_6 . When both these branches are turned on, if the calibrating DAC was linear, we would have a total current of $25 I_{lsb}$ added by the sub ladder. But since it is not, we would have some other current, thereby having an effect on the INL.

In order to solve the above problem, we can use different ladders for different bits, thereby reducing the effect of non-linearity in the sub ladder. Since it was noted that the error current in lower branches, we would not be needing 16 sub ladders for calibration. Instead, we could group in different branches together, so that the number of sub ladders needed in the end would be reduced.

Since the sub-ladder used is of 11-bit resolution, an alternative technique would be to calibrate the 11-bit ladder using a 7-bit ladder.

3.4 Results

For the final calibration algorithm, 3 sub ladders of 11 bit resolution were used. The branches 11,10 and 9 were calibrated using one ladder, branches 15 and 11 with another and finally, the branches 13 and 12 with the third sub ladder. The supply voltage of 11-bit sub ladder was $V_{dd}/16$ and the following INL was observed when averaged over 50 cases.

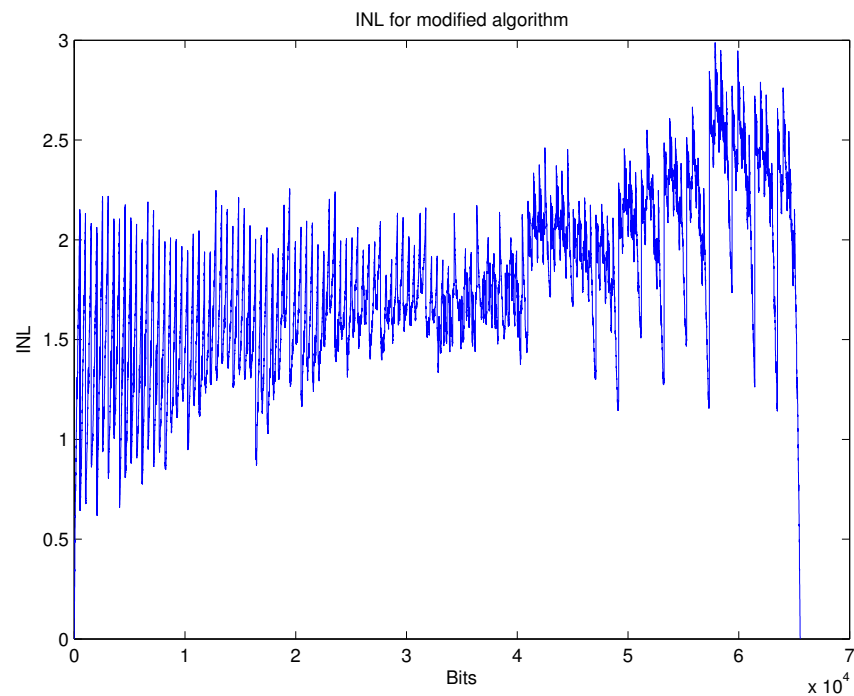


Figure 3.6: INL for the final algorithm used

CHAPTER 4

Comparator

4.1 Comparator Specifications

The comparator plays an very important part of the circuit, as it enables us to compare two different voltages, thereby enabling us to calibrate accurately. Since the value of LSB voltage is equal to $1.4V/2^{16} = 21\mu V$, the comparator should be able to detect such low voltages as only then can we expect the expect the error in the currents to be less than 1LSB. Different comparator architectures are discussed in detail (7).

A comparator consisting of a simple positive feedback latch would fail to operate as it would have an in built offset in it. The offset voltage of a simple latch, consisting of two inverters connected back to back, was calculated to be around 5mV, thereby making it impossible to use it for calibration as it would fail to detect voltages below 5mV. In order to overcome this problem, one needs to use an pre-amplifier. Therefore, the comparator design can be broadly classified into two parts :

1. Latch
2. Pre-Amplifier

4.1.1 Pre-Amplifier

A pre-amplifier is used to amplify the difference voltages to a level such that the latch would be able to regenerate it the full voltage levels. The worst case error in the currents in any branch of the R-2R ladder would be in the order of 100LSB. So that would mean that the maximum voltage swing required would be in the order of $100 \times 21\mu V = 2.1mV$. Since the swing limits placed are not very stringent and we need to reduce power to as much as possible, a telescopic cascode opamp was used as a pre-amplifier. Note that the gain of the telescopic cascode opamp should atleast be $500(= 10m/21\mu)$,

The telescopic opamp built has the following structure:

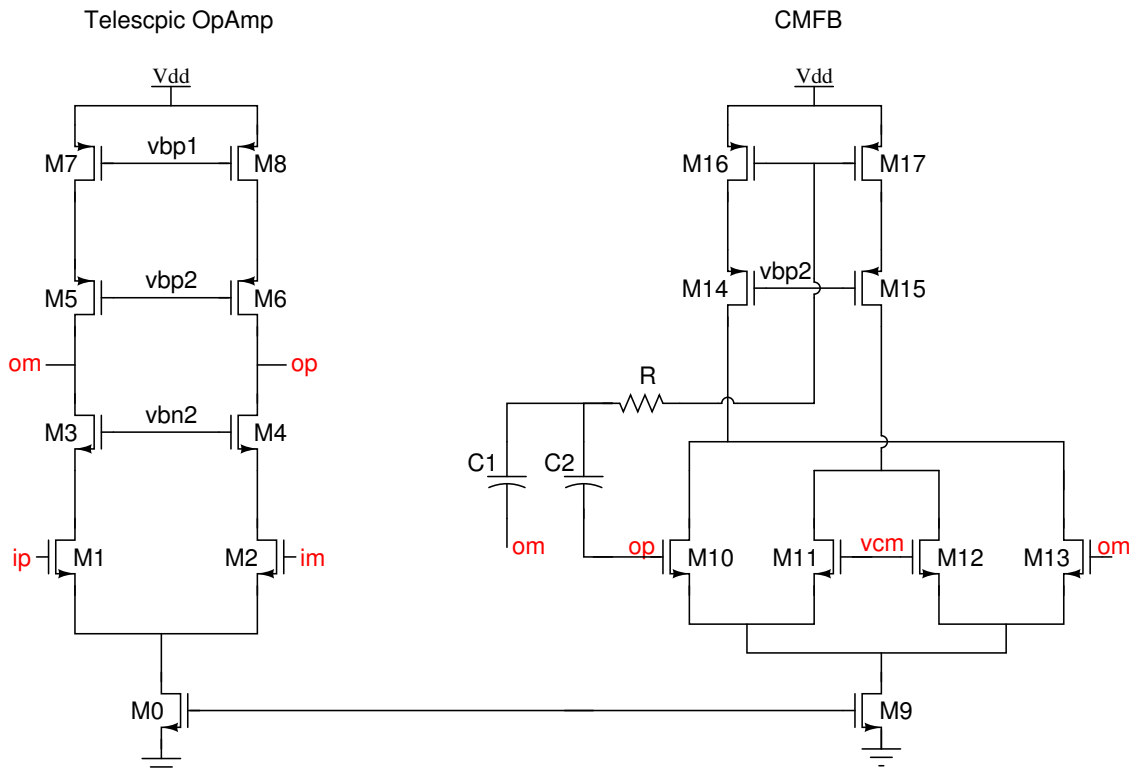


Figure 4.1: Telescopic Pre-Amplifier

Transistor	Size (W/L)
M0	8(0.75 μ /1 μ)
M1,M2,M3,M4	4(0.75 μ /1 μ)
M5,M6,M7,M8	16(0.75 μ /1 μ)
M9,M10,M11,M12,M13	4(0.75 μ /1 μ)
M14,M15,M16,M17	8(0.75 μ /1 μ)

The above table gives the dimensions of the MOSFET's used in the telescopic opamp. In the above circuit, both the capacitors are 1pf each.

The telescopic opamp built, has a gain of 60dB and the total current consumed was 137 μ A. The output from the telescopic opamp could not be directly connected to the inputs of the positive feedback latch. This is because of the low on resistance during the evaluation period. Hence I used a voltage buffer in the form of voltage follower before connecting it to the positive feedback latch.

The final block diagram of the circuit looks as follows :

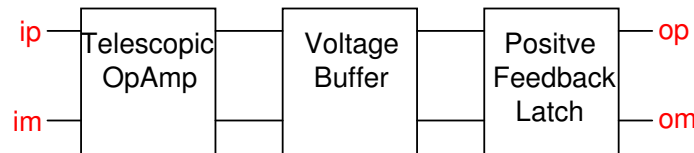


Figure 4.2: Block Diagram

The input given to the opamp was a square wave of time period =40 μ s and 12 μ V_{pp} differential. The output observed is shown in the following plot.

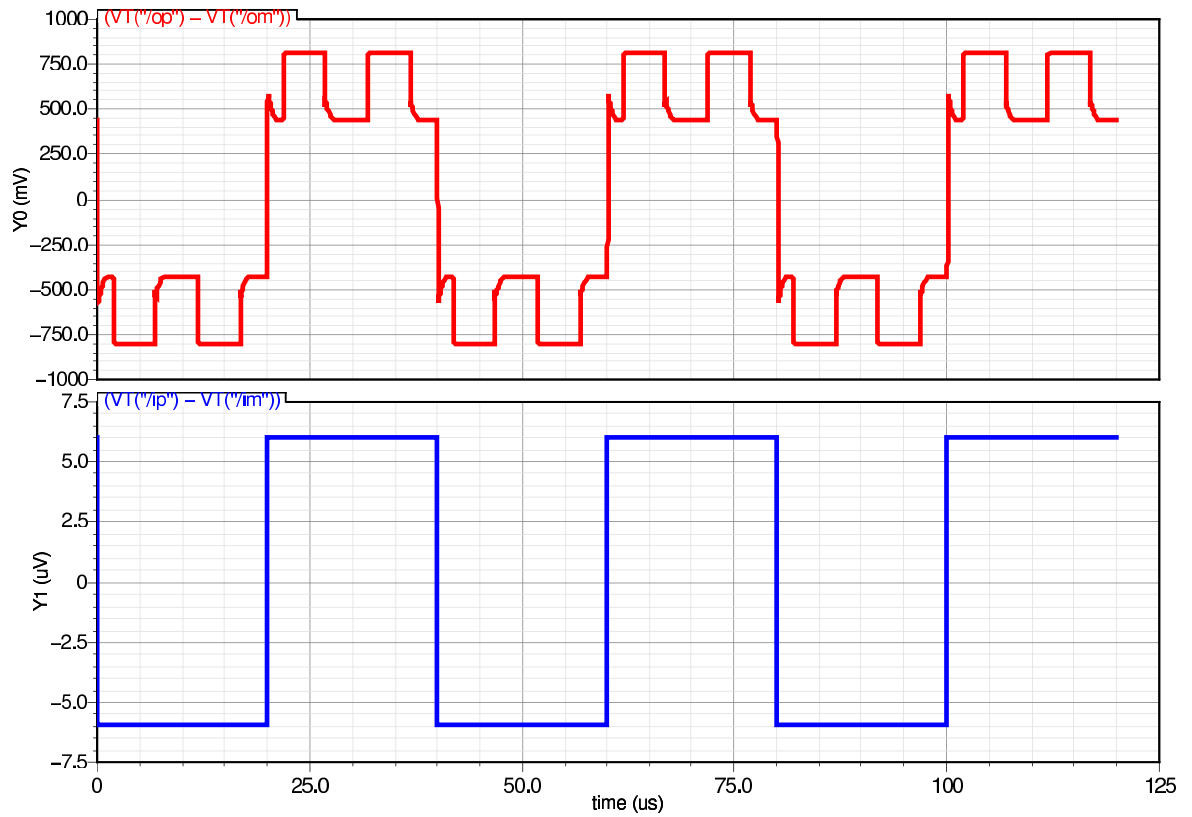


Figure 4.3: Comparator Output

In the above plot, the frequency of the input was taken to 25kHz. The frequency of operation can be improved further until 0.1MHz and has been checked for it.

4.2 Latch

The latch works on the principle of positive feedback, wherein it takes the output from the pre-amplifier in one cycle and regenerates in the other to give an output of V_{dd} or 0 accordingly. The latch consists of two inverters connected back-to-back

as shown in figure B.1 :

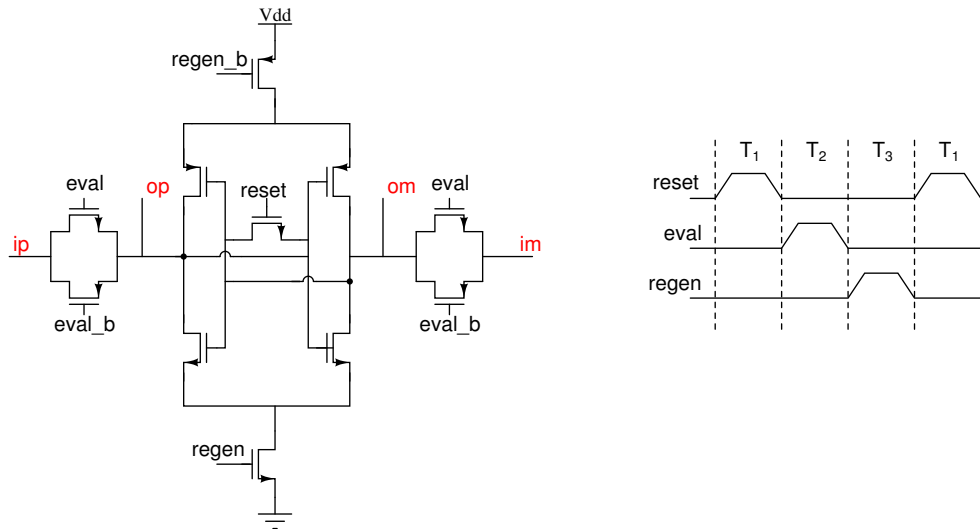


Figure 4.4: Regenerative Latch

In the figure B.1, the three phases of operation of a latch are shown.

1. Reset
2. Evaluate
3. Regenerate

4.2.1 Reset

During the reset phase, the outputs of the latch are both re-initialized to the common mode voltage of the latch. This is to make sure that no memory is transferred from one decision cycle to the next, i.e. in other words to avoid hysteresis. The simplified version of the latch reset phase is shown in figure 4.5

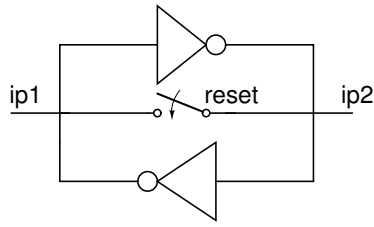


Figure 4.5: Simplified model of the latch

4.2.2 Evaluate

During this phase, the inputs are evaluated and stored on the parasitic capacitance of the latch. For the input to be evaluated properly, one needs to make sure that the input signal is greater than the offset of the latch. For if this condition is not met, then the output would be erroneous. Therefore, to make sure that the output is correct, the offset voltage effect must be taken care off. The offset voltage of the latch was evaluated to be

$$\sigma_{offset} = \frac{\sqrt{g_{mp}^2 \sigma_{v_{tp}}^2 + g_{mn}^2 \sigma_{v_{tn}}^2}}{g_{mp} + g_{mn}}$$

Therefore, for the latch to operate as expected, the input voltage needs to be greater than the offset value. The above offset value was calculated to be 3mV, thereby putting a restriction on the minimum input voltage to be more than 3mV.

4.2.3 Regenerate

In the regenerate phase, we have both the inverters connected back to back as shown in [4.5](#)

During the reset phase, both the inverters are shorted. Therefore, the settling point of the system would be the common mode voltage. But once the reset signal is removed, and a small difference voltage is applied to the input, due to positive feedback of the circuit, we would see the output voltage settle at V_{dd} and the other settling at 0 depending on which of the inputs, ip1 or ip2, was greater. The modeling of the positive feedback circuit is dealt with in the appendix.

4.2.4 Offset Cancellation

Consider an amplifier. Ideally, with a zero input, the output of the amplifier should also be equal to zero. Due to random mismatches present in the IC, we have an offset voltage present in the amplifier, therefore, even for a zero input, we get a non-zero output.

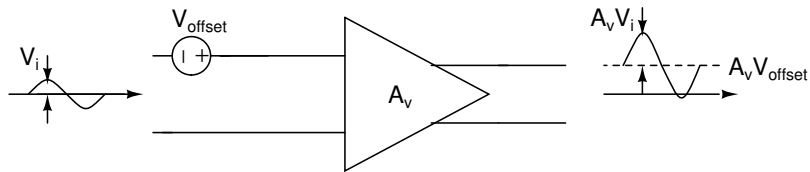


Figure 4.6: Need for offset cancellation

As it is seen in the above figure that the offset voltage is also amplified, one needs to develop a technique to remove the offset from the pre-amplifier so that it does not affect the actual input. To do this, the following offset cancellation technique was used :

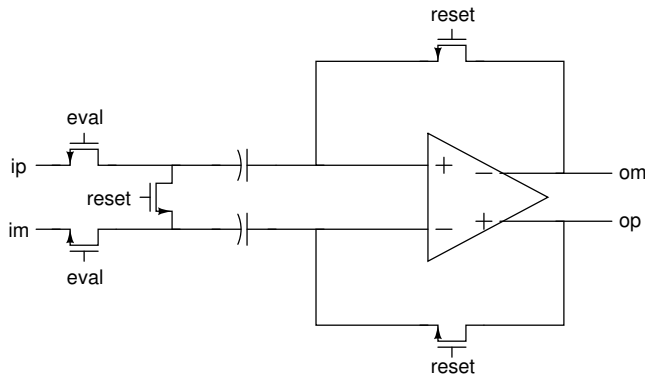


Figure 4.7: Offset cancelation

4.3 Comparator

The latch and the pre-amplifier discussed in the previous are combined together to form the comparator. Along with it, the pre-amplifier was offset corrected. The complete comparator circuit is shown in figure 4.8

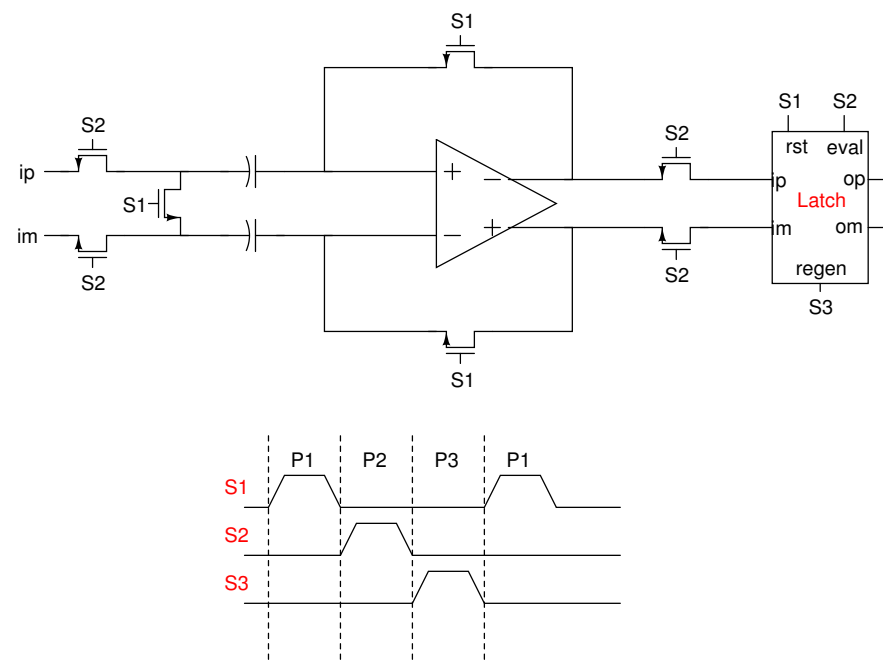


Figure 4.8: Final comparator circuit

4.4 Simulation Results

In the above circuit, for the sake of testing purposes the offset present in the input amplifier was implemented by putting a dc voltage source appropriately. The following results were observed for an offset of 15mV in the opamp and 3mV offset in the Latch.

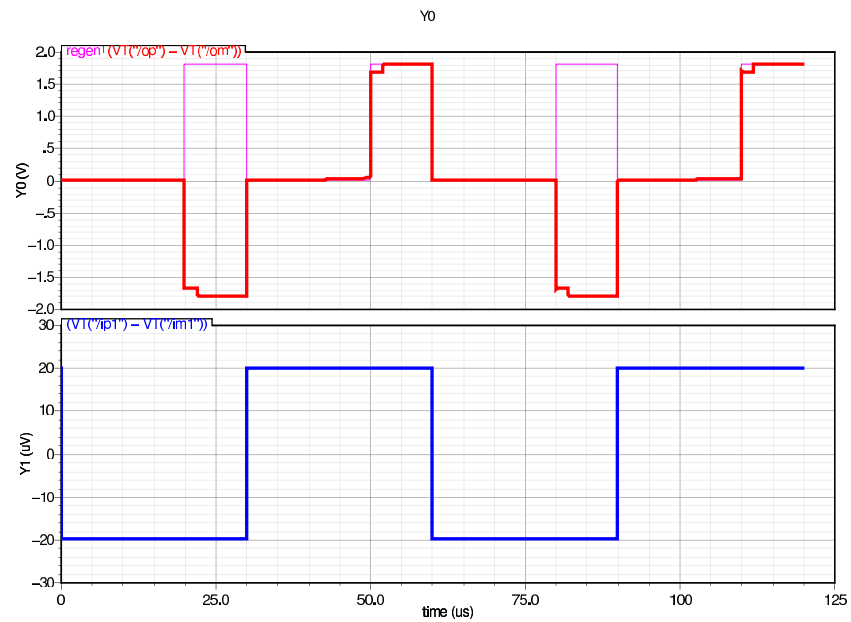


Figure 4.9: Output

The blue square shows the input signal, the pink square wave shows the regenerate signal and the red square wave is the output.

CHAPTER 5

Results

5.1 Results

With the above calibration scheme discussed above, the INL measured was a maximum of 3 LSB. In order to measure the distortion performance, a sinusoidal wave with frequency close to $f_s/2$ was given and whose magnitude was 1db less than the max. allowed value i.e. input taken was

$$x = 1 + 0.89 \cdot \sin(2 \cdot \pi \cdot n / N \cdot 501) ; , N=1024$$

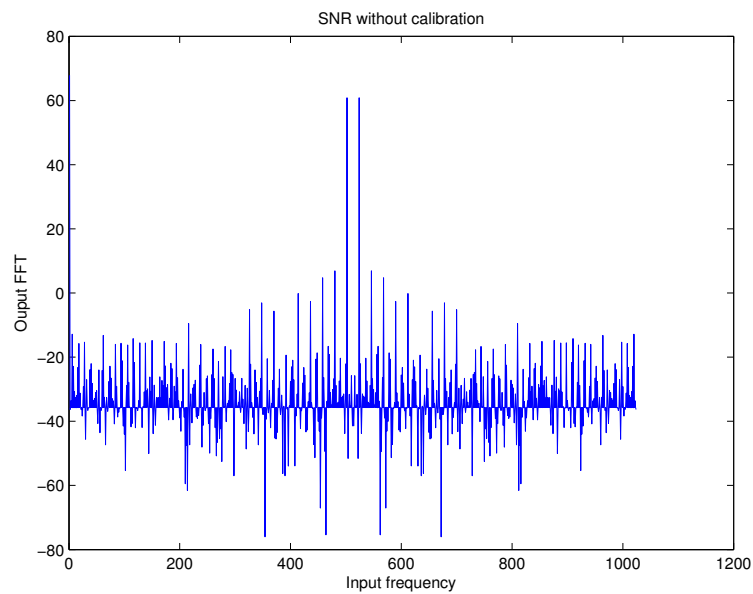


Figure 5.1: FFT without calibration

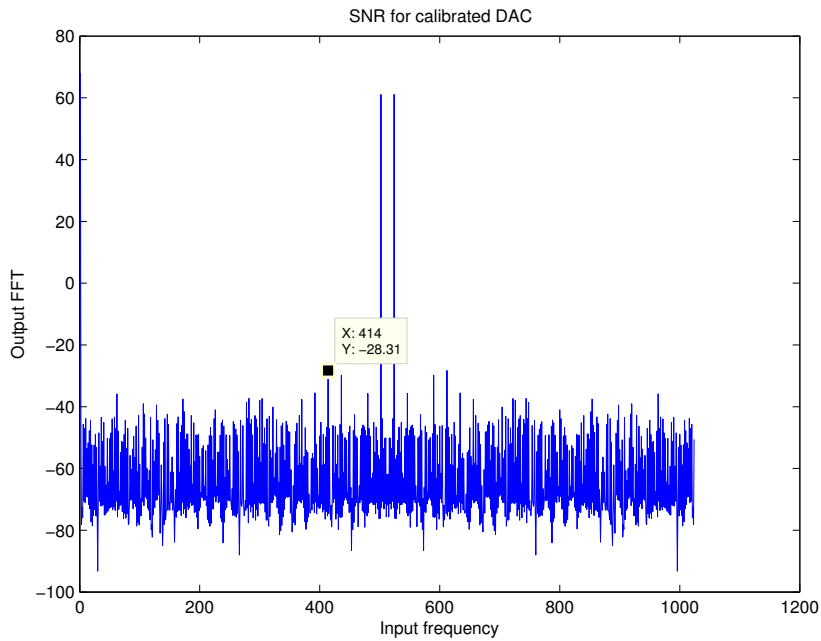


Figure 5.2: FFT with calibration

The SNDR observed was equal to 91db with calibration and and 51db without calibration.

The final calibration algorithm used for the design consists of one main ladder and the other a normal 16-bit R-2R ladder. The algorithm used for calibration is self calibration algorithm discussed earlier.

5.2 Layout

The layout of the R-2R ladder is completed, and was tested with an ideal opamp for its performance. The SNDR obtained was 97 db. The layout of the ladder is shown in the following figure :

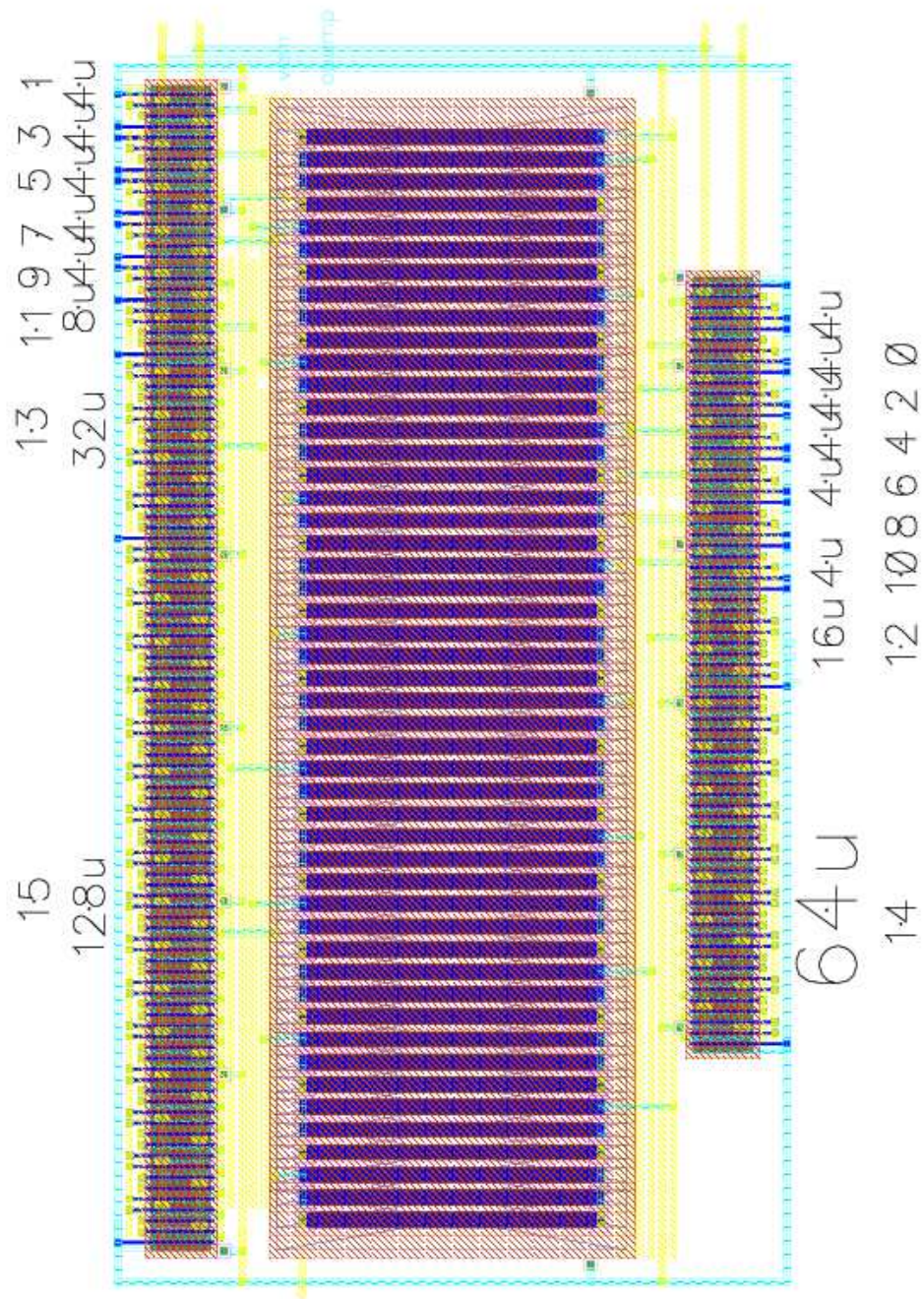


Figure 5.3: Layout of the R-2R Ladder

CHAPTER 6

Conclusion & Future Work

6.1 Conclusion

Different digital calibration schemes have been proposed in this particular architecture along with the drawbacks of each of them. The calibration algorithms developed are not in particular with a 16-bit DAC, and could be used on a wider scale, i.e. to say that the same algorithms could be used to calibrate a 18-bit or an 11-bit DAC with slight modifications.

6.2 Future Work

In the self calibration approach discussed, the accuracy of the algorithm depends very much on the accuracy of the sub-ladder available. Therefore, instead of using an inaccurate R-2R sub ladder, we could make an accurate 11-bit DAC, say a current steering DAC, which could be used for calibration. This will surely improve the performance of the main DAC because of the very fact that it would be a linear system.

APPENDIX A

DNL & INL

DNL stands for Differential Non Linearity. It shows how much two adjacent code analog values deviate from the ideal 1LSB step. INL, Integral Non-Linearity, gives a measure of performance of the DAC. It shows how much the DAC transfer characteristic deviates from an ideal one. That is, the ideal DAC characteristic is a straight line; INL shows how much the actual voltage at a given code value differs from that line, in LSBs (1LSB steps). Therefore, we would have

$$INL(n) = \sum_{i=0}^n DNL_i \quad (\text{A.1})$$

The calculation of INL and DNL for a 3-bit DAC is shown in the following table

Binary Value	Current Sources Turned On	Output	DNL	INL
0	-	0 LSB	-	-
1	I_0	1.3 LSB	0.3 LSB	0.3 LSB
2	I_1	2.3 LSB	0 LSB	0.3 LSB
3	$I_0 + I_1$	3.6 LSB	0.3 LSB	0.6 LSB
4	I_2	3.4 LSB	-1.2 LSB	-0.6 LSB
5	$I_0 + I_2$	4.7 LSB	0.3 LSB	-0.3 LSB
6	$I_1 + I_2$	5.7 LSB	0 LSB	-0.3 LSB
7	$I_0 + I_1 + I_2$	7 LSB	-0.2 LSB	0 LSB

From the above table, we can clearly see that the DAC fails to operate normally, and can come to the conclusion that for a DAC to function normally, one would need the $|INL|$ to be less than 0.5 LSB. This condition can also be arrived from the condition that $|DNL| \leq 1$.

APPENDIX B

Regeneration in a Positive Feedback Latch

The three phases of the regenerative latch is once again shown here :

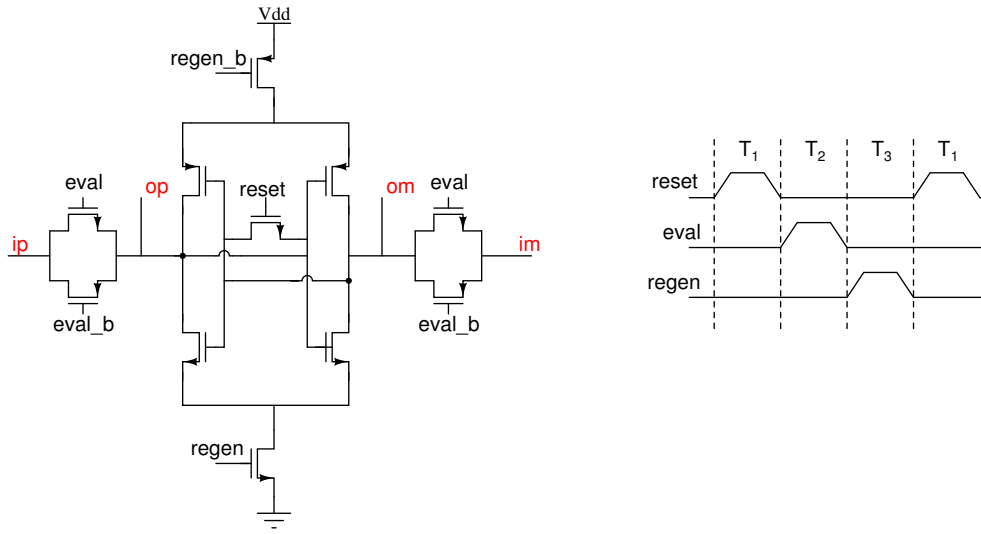


Figure B.1: Regenerative Latch

In the regeneration phase of the latch, , the latch can be represented by a simplified circuit consisting of two back-to-back inverters, as shown in the following figure

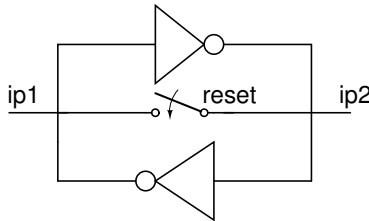


Figure B.2: Simplified model of a latch in regeneration phase

Since the output voltages of the two inverters at the end of the evaluate phase

are close to each other, the inverters can be modeled as a VCVS driving RC loads as shown in the following figure :

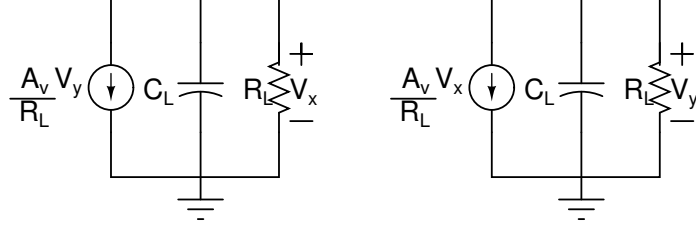


Figure B.3: Simplified model of a latch in regeneration phase

The above circuit can be solved for the the difference voltage ($V_x - V_y$) (8). Upon solving the above circuit, we get

$$\Delta V = \Delta V_o e^{(A_v - 1)t/\tau} \quad (\text{B.1})$$

where $\Delta V = V_x - V_y$ is the difference voltage, $\tau = R_L C_L$ is the time constant and gain A_v is the low-frequency gain of each inverter and is equal to $g_m R_L$, where g_m is the inverter's transconductance. The above equation can be approximated to give a time constant τ_{latch} , which is given by

$$\tau_{latch} = \frac{C_L}{g_m} \quad (\text{B.2})$$

Therefore, if ΔV_o is the initial differential voltage level applied to the latch before regeneration, and ΔV_{logic} is the voltage necessary for the succeeding stages to recognize the correct output value, then the total time required for this operation is

given by

$$T_{latch} = \frac{C_L}{g_m} \ln \left(\frac{\Delta V_{logic}}{\Delta V_o} \right) \quad (\text{B.3})$$

Therefore, from the above equation, we can conclude that if ΔV_o is small, then the amount of time needed for the latch to regenerate to ΔV_{logic} will be larger and viceversa.

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