Design of a 32kb SRAM and a 16 byte register in a 0.18μm CMOS process

A Project Report

submitted by

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under the guidance of

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MAY 2007

THESIS CERTIFICATE

This is to certify that the thesis titled **Design of a 32kb SRAM and a 16 byte register in a 0.18μm CMOS process**, submitted by **Tanuj Goyal**, to the Indian Institute of Technology Madras, for the award of the degree of **Bachelor of Technology**, is a bona fide record of the B.Tech work done by him under my supervision. The contents of this thesis, in full or in part, have not been submitted to any other Institute or University for the award of any degree or diploma.

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I would like to cherish the unforgettable moments spent in IIT and all my friends in VLSI laboratory. I would also like to thank all my friends for the discussion and encouragement provided throughout the project and my life at IITM.

Finally, I thank all those who have shown their cooperation in my work directly or indirectly. I convey my sincere thanks to all of them.

ABSTRACT

This thesis discusses two topics:

32kb SRAM : Design of SRAM, decoders, sense amplifier and multiplexer has been discussed. The overall goal is to provide a memory circuitry which can operate at low power and high speed in 0.18μm CMOS technology. The designed memory cell uses 6T architecture with 2 PMOS and 4 NMOS. The differential Sense amplifier has been used which amplifies the difference of 20mV to 1.7V in 200ps. Buffers have been used to maintain the signal swing. Multiplexer also works on differential logic. This designed memory runs at 2.5GHz with a total average power consumption of 550mW on simulating with Cadence. This is likely to operate at lower speeds after completing its layout.

16 byte register file : Design of static memory which consists of sixteen 8bit registers has been discussed. This design uses D flipflops with feed back logic as its basic cell. This memory has been designed using 0.18μm CMOS technology. This register file uses an area of .22x.25mm^2 with an average power consumption of 56μW @ 5Hz.

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CHAPTER 1

Introduction

Static random access memory (SRAM) is a type of semiconductor memory. The word static indicates that the memory retains its contents as long as power remains applied, unlike dynamic RAM (DRAM) that needs to be periodically refreshed.

A high speed and low power SRAM is a key device for many VLSI chips. This is true especially for embedded memories like on-chips caches. The key to the low power operation in the SRAM is to reduce the signal swing on the high capacitance bit lines. This minimum required signal swing is limited by the sensitivity of the sense amplifier, the better the sensitivity, the lower the power consumption as it can detect even a low differential voltages of bit and $\overline{\text{bit}}$ lines. This brings us a need to build a good sense amplifier and a low capacitive bit lines of SRAM. Another way to reduce the power consumption is not to precharge the bit and $\overline{\text{bit}}$ lines to Vdd but, reset them to a common potential through a NMOS reset switch. There is a need for highly capable sense amplifier which will not only detect the low difference between bit and $\overline{\text{bit}}$ lines but will also able to amplify the low magnitude signal . This report deals with such a design of sense amplifier which is able to perform both the operations.

To achieve high speed in SRAMs, there is a need to design a good architecture which can reduce the capacitance of bit and $\overline{\text{bit}}$ lines. There are some applications which require only small SRAMs and these can be run at high speed as the capacitive load as well as area is reduced.
This report discuss the complete design and architecture of 32kb SRAM and 16 byte register file.

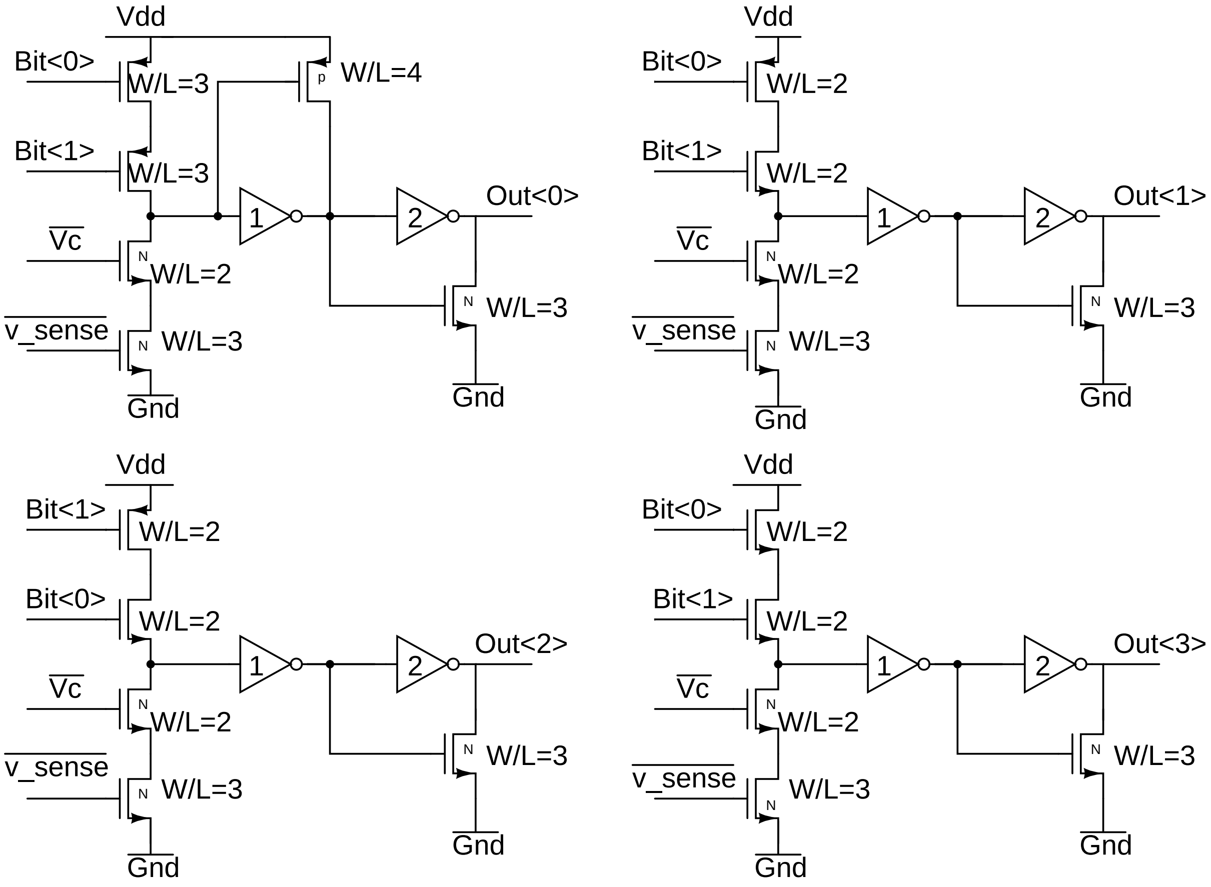
To measure the on-chip performance of DAC or ADC such SRAMs can be used. There are high speed DACs or ADCs which have low speed external interfaces. Such DACs or ADCs can work based on the speed of external interfaces. These SRAMs can be accessed at low speed for writing and at high speed for reading purposes.

There are applications which require even a smaller memory at very low speed. Such memory can be used to control various parameters in RF transceiver. Such parameters can be SET, START, STOP, RESET etc. 16 byte register file can be used to give sixteen such signals.

CHAPTER 2

Decoders

2.1 2 Bit decoder



Inverter 1 : (P_INV W/L=2) and (N_INV W/L=4)
Inverter 2: (P_INV W/L=3} and (N_INV W/L=2)

Figure 2.1: 2 Bit decoder

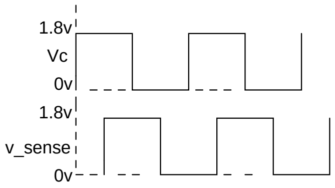


Figure 2.2: Two clocks (Vc and v_sense)

2 Bit decoder:

This has been designed using MOSFETs and buffers. The sizes above are chosen to satisfy the swing limits. v_sense is 90 ° ahead of Vc in phase, when both $\overline{\text{Vc}}$ and $\overline{\text{v\_sense}}$ become high then we reset the output node .

2.2 4 Bit decoder

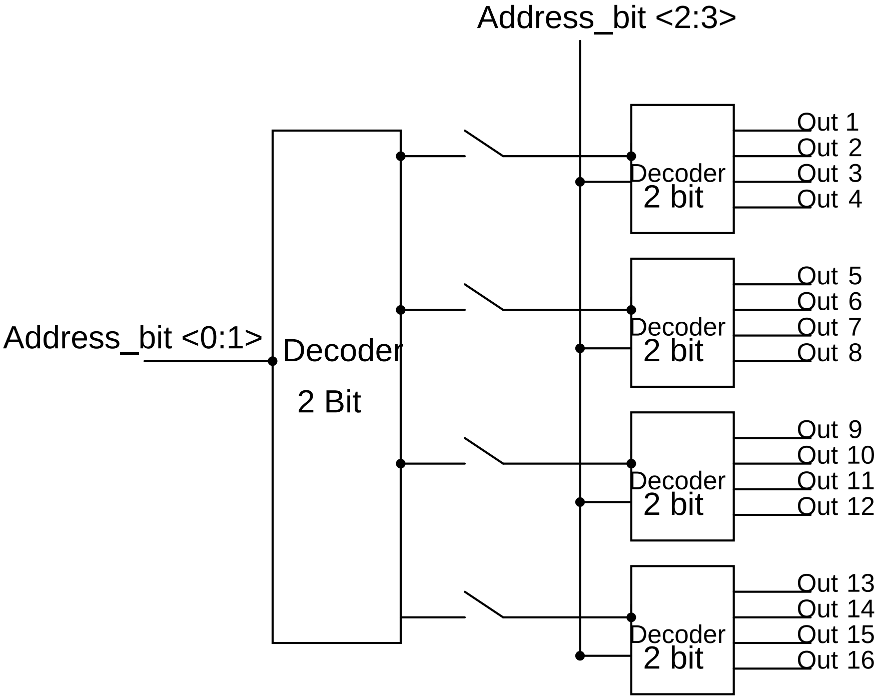


Figure 2.3: 4 Bit Decoder

4 Bit decoder:

This has been made using 2 bit decoders. Some additional buffers have been put inside the cascading decoder block to maintain the signal swing and delay. Address_bit 0 form the MSB and Address_bit 3 form the LSB of this 4 bit decoder block. In Fig. 2.3, when the input appears at the Address_bit bus of the left most decoder, it generates an output to select one of the four column decoders.

2.3 8 Bit decoder

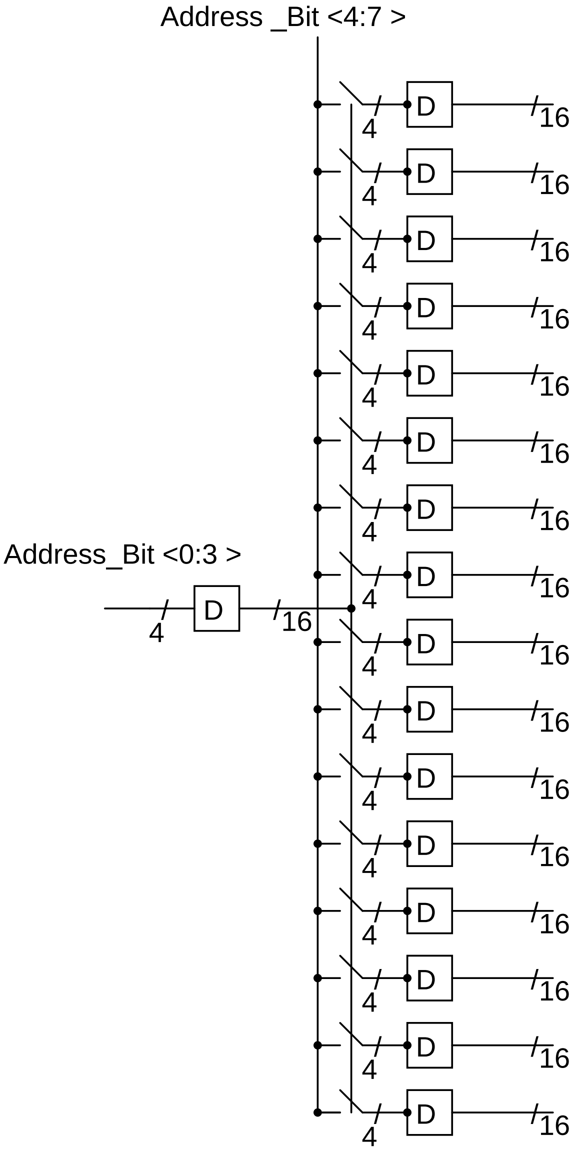


Figure 2.4: 8 Bit Decoder

8 Bit decoder:

This is made using 4 bit decoders. The 4 bit decoder used here is described in Fig. 2.3.The left most 4 bit decoder as shown in Fig. 2.4 generates 16 outputs.These 16 outputs act as control signals to access 16 different NMOS switches, to select only one column decoder. Also, some additional buffers have been used inside the cascading decoder block to maintain the signal swing. Address_bit 0 form the MSB and Address_bit 7 form the LSB of this 8 bit decoder block.

CHAPTER 3

Design of SRAM

3.1 6T SRAM cell

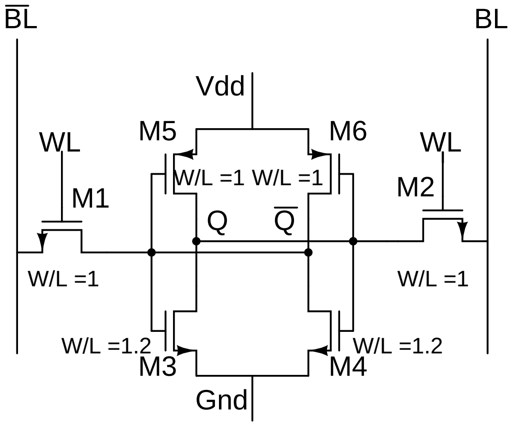


Figure 3.1: 6T SRAM Cell

6T SRAM Cell

Reference [1] discusses low power SRAM circuit design.
Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. Thus it takes six MOSFETs to store one memory bit.

Access to the cell is enabled by the word line (WL in Fig. 3.1) which controls the two access transistors M1 and M2 which, in turn, control whether the cell should be connected to the bit lines: BL and $\overline{\text{BL}}$. They are used to transfer data for both read and write operations.

$$\mathrm{I} = \mu\mathrm{Cox}\frac{W}{2L}(Vgs - Vt)^2$$

3.2 SRAM Operation

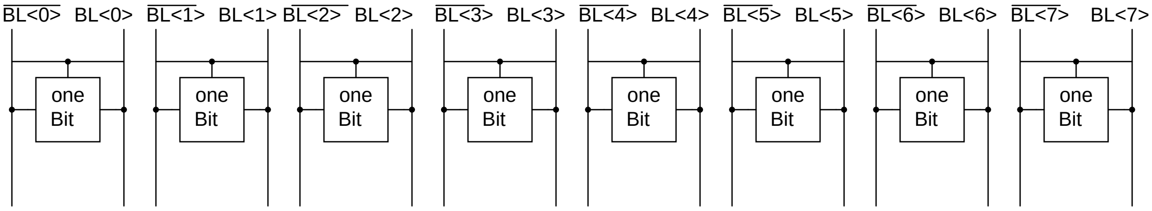


Figure 3.2: Byte wide memory

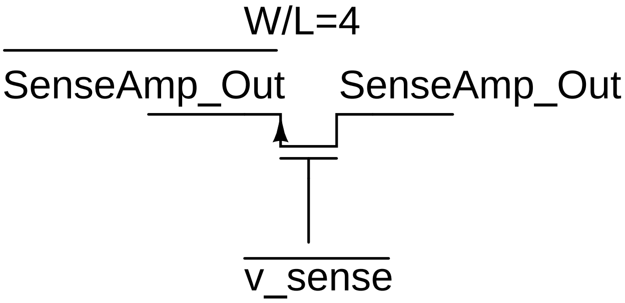

W/L=4
$\overline{\text{SenseAmp\_Out}}$
SenseAmp_Out
$\overline{\text{v\_sense}}$

Figure 3.3: Reset Switch

Byte wide memory

8 SRAM cells are combined to give one byte. WL is the control address to select these SRAMs cells for read or write operation. Before read or write operation we need to reset the bit and $\overline{\text{bit}}$ lines by simply making the two voltages common through reset NMOS switch.

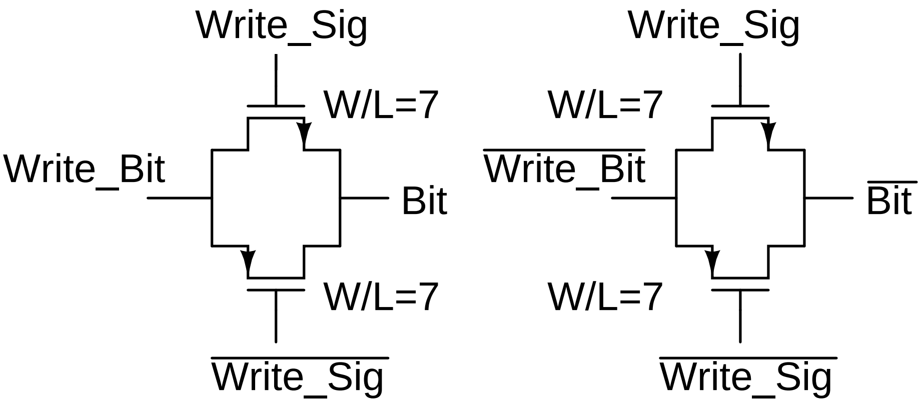

Write_Sig
W/L=7
Write_Bit
Bit
W/L=7
$\overline{\text{Write\_Sig}}$
Write_Sig
W/L=7
$\overline{\text{Write\_Bit}}$
$\overline{\text{Bit}}$
W/L=7
$\overline{\text{Write\_Sig}}$

Figure 3.4: Write logic

During write operation, the 8 bit write data is placed on the bit and $\overline{\text{bit}}$ lines by making the Write_sig high and $\overline{\text{Write\_sig}}$ low, which then gets written at the nodes of two cross-coupled transistors. If we wish to write a 0, we would apply 0 Volts to the bit lines, i.e. setting Write_bit to 0 and $\overline{\text{Write\_bit}}$ to 1.8V. This 0V will cause the voltage of the corresponding node to fall from common point to 0, which in turn makes the other end rise upto 1.8V. The voltages are applied the other way round to write a 1.

During Read operation, first we have to reset the bit and $\overline{\text{bit}}$ lines, then assert the word line WL, which will enable both the access transistors M1 and M2 causing a change between bit and $\overline{\text{bit}}$ line voltage that can be sensed using a Sense amplifier and multiplexer to compute the data bit.

CHAPTER 4

Sense Amplifier

4.1 Sense Amplifier

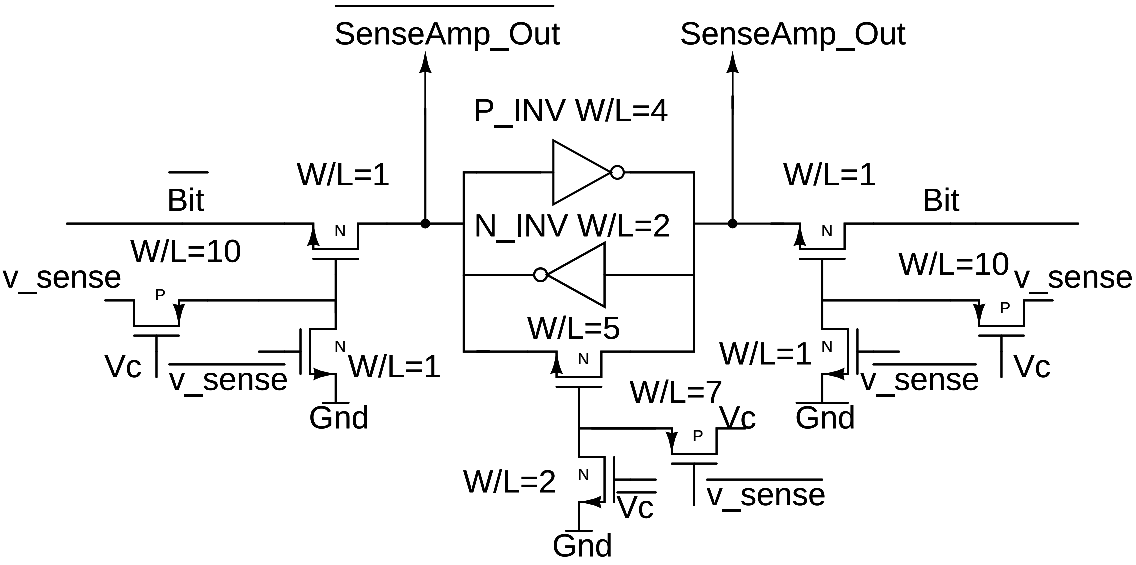


Figure 4.1: Sense Amplifier

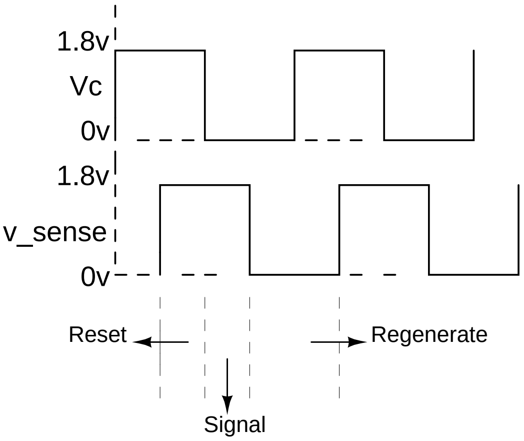


Figure 4.2: Different phases of clock for sense amplifier

Sense amplifier

References [2] and [3] discuss the design of high performance and low voltage sense amplifiers.

The sense amplifier which is shown in Fig. 4.1 works differentially. Once bit and $\overline{\text{bit}}$ voltages are sufficiently different, which is typically few mV. The difference voltage is then applied to the two cross-coupled inverters of the sense amplifier through the use of 2 NMOS switches. In this case the difference is 20mV. The input is applied only for the quarter clock cycle that is when Vc is low and v_sense is high as shown in Fig. 4.2. After the signal is applied the cross-coupled inverters will regenerate the differential signal voltage to approximately full rail to rail swing in about half the clock cycle which is when v_sense is low. The amplifier is then reset to the common value in the last quarter cycle which is when Vc is high and v_sense is also high.

CHAPTER 5

Multiplexer

5.1 4:1 Multiplexer

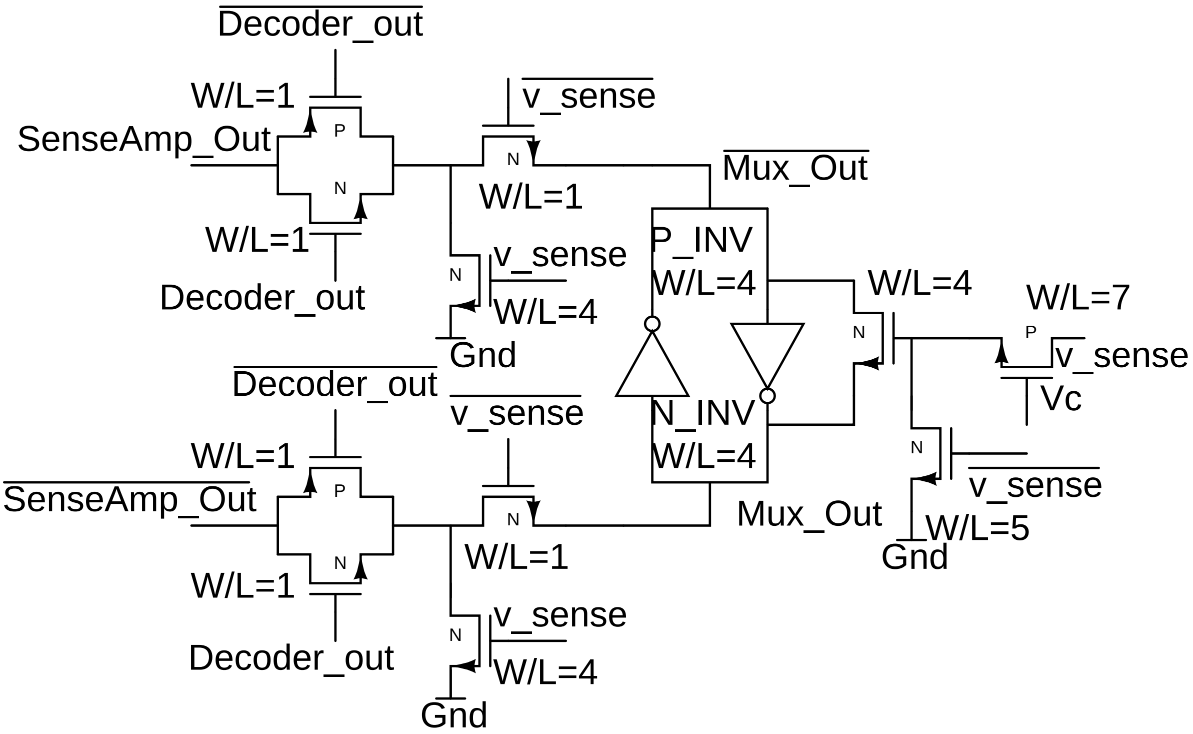


Figure 5.1: Multiplexer

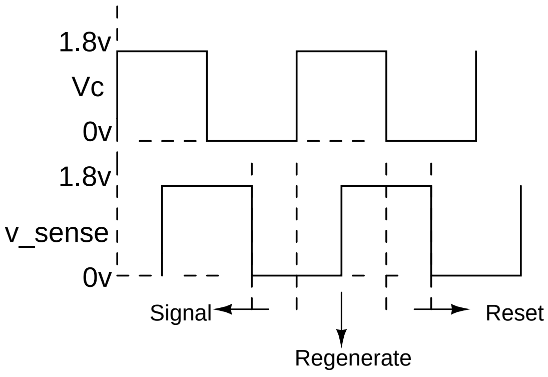


Figure 5.2: Different phases of clock for multiplexer

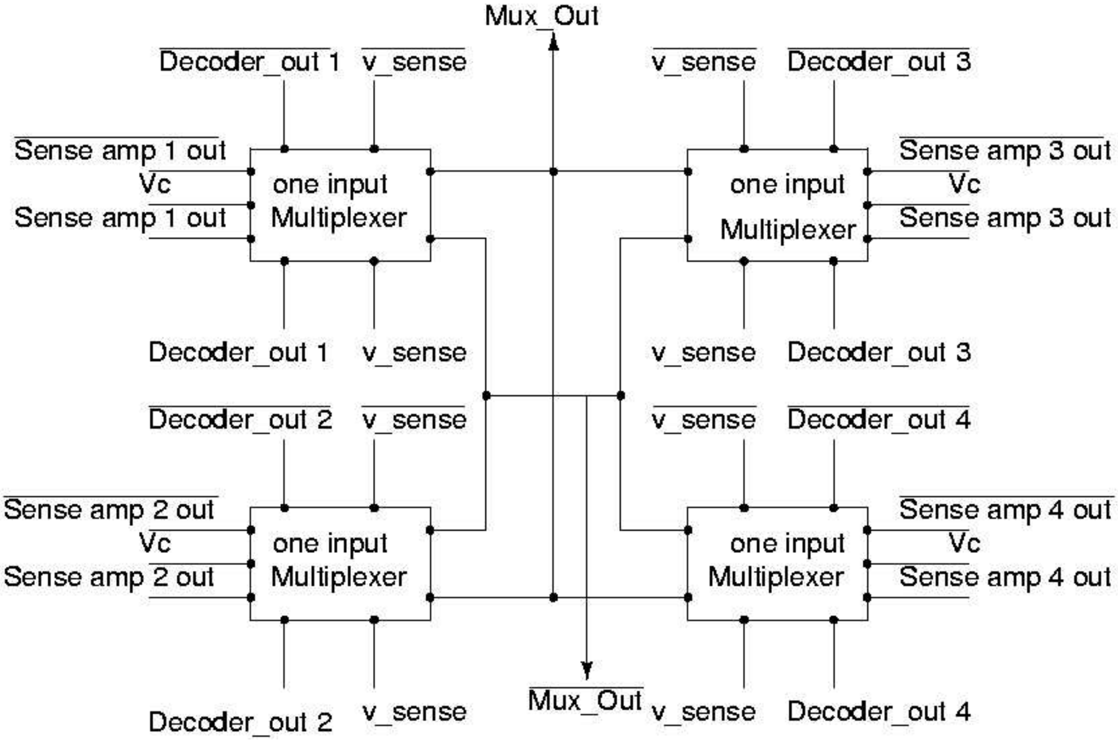


Figure 5.3: Connections of all four inputs to multiplexer

4:1 Multiplexer

Fig. 5.1 indicates only one input part of the multiplexer. The output of the sense amplifier is applied as the input to the multiplexer through the transmission gates which are controlled by the output of the 2 bit decoder. The input to this decoder is the upper most 2 MSBs of 12 Bit address bus. The signal to this multiplexer will be regenerated when Vc is high and reset to the common voltage in the next quarter cycle when v_sense is high and Vc is low.In the final design four such circuits will be connected together which is shown in Fig. 5.3.

See Fig. 6.3 to know how SRAM, decoders, sense amplifier and multiplexer are connected.

CHAPTER 6

Integration of memory circuitry

6.1 2kb SRAM

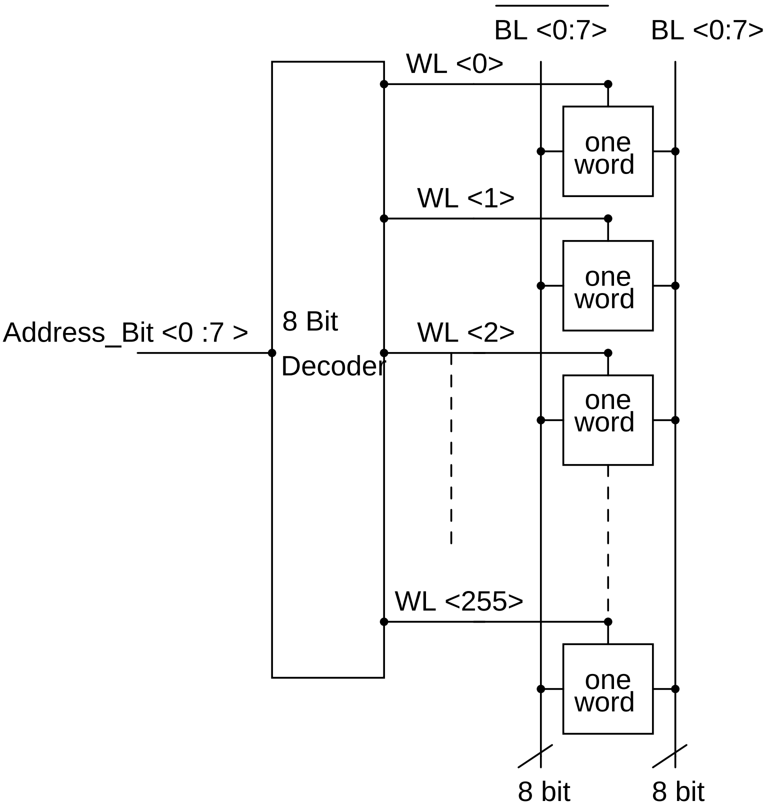


Figure 6.1: 2kb SRAM

2kb SRAM

8 bit decoder is generates 256 addresses which access 256 bytes of memory or 2kb. The data byte appears at bit and $\overline{\text{bit}}$ lines.

6.2 8kb SRAM

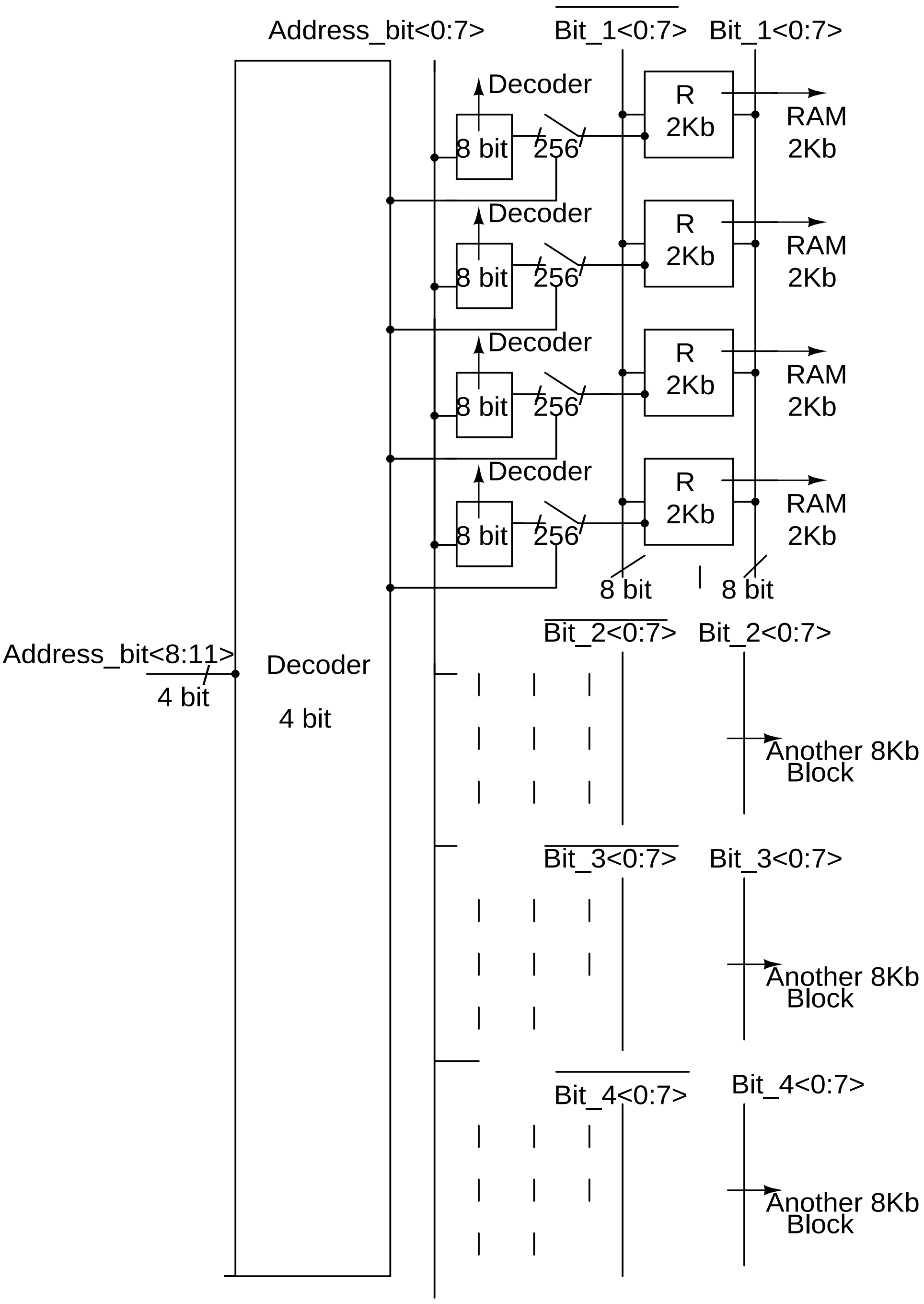


Figure 6.2: 8kb SRAM

8kb SRAM

We have used 4 bit decoders to select (one out of sixteen) 2kb SRAM. This decoder generates outputs as well as their complements so that at any point of time we can select only one block. The address to this 4 bit decoder is the top most 4 MSBs of address_bit bus. We have put separate 8 bit decoders for each of the 2kb SRAM blocks as shown in Fig 6.2.

6.3 32kb SRAM

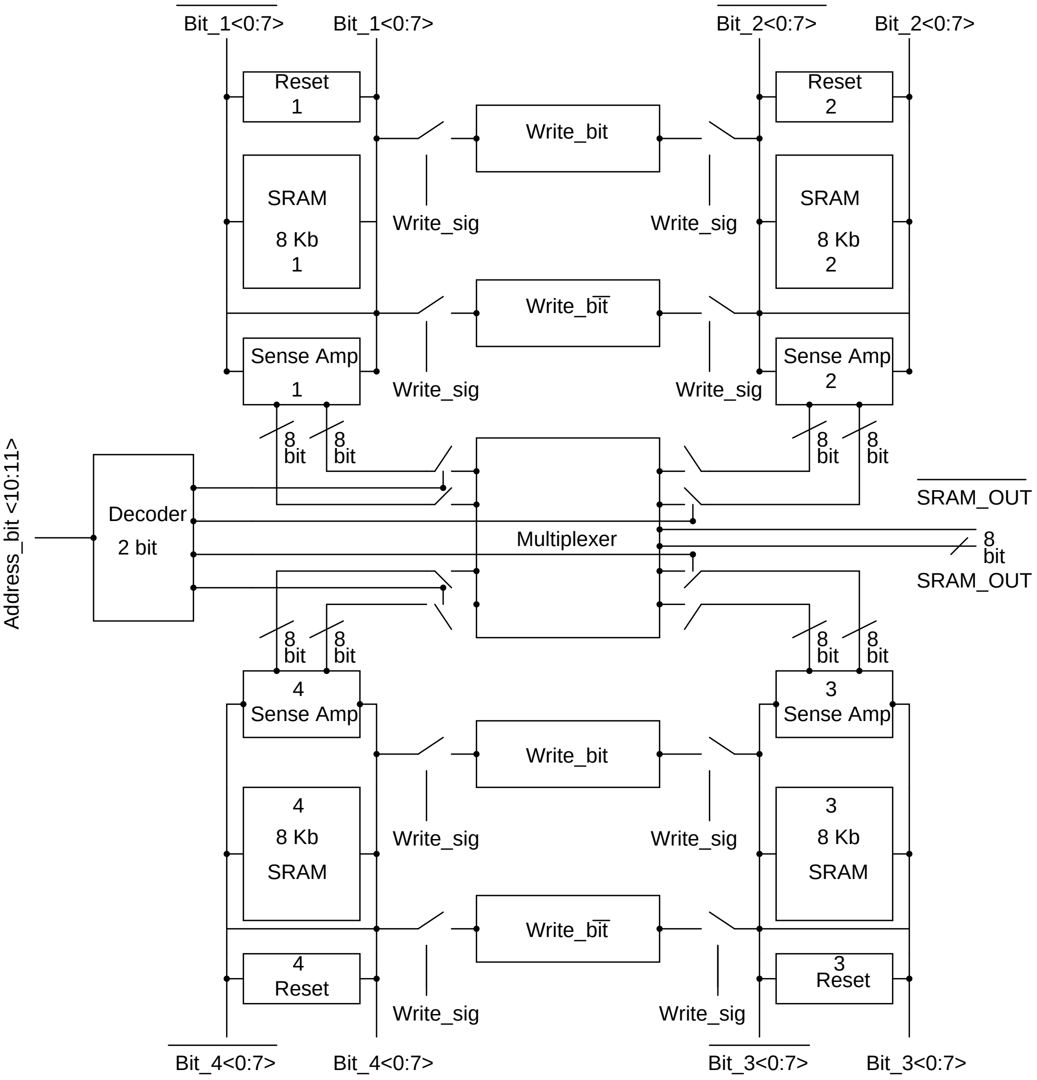


Figure 6.3: 32kb SRAM

32kb SRAM

The Fig. 6.3 is the final design of the integrated SRAM, decoders, sense amplifiers and multiplexer. There are 4 separate 8kb memory blocks which are provided with 4 sense amplifiers and 1 multiplexer . To select the output from one of these four sense amplifiers, a 2 bit decoder with some buffers is used which decodes the top most 2 MSBs of address bus. The output of one of these sense amplifiers is given as the input signal to differential multiplexer to generate the data read from the SRAM cell. The buffers in the decoder in Fig. 6.3 have been used to compensate the delay of half clock cycle between the row address of SRAM and output of the sense amplifier.

There is also a latency of half clock cycle between the sense amplifier output and multiplexer output, which makes the overall latency of one clock cycle between row address of SRAM and multiplexer output.

For write operation, the data should be placed to the bit lines of each 8kb block and it gets written to the cell based on the address generated by the decoders which is shown in Fig. **??**. First, 2kb SRAM is selected based on the address generated by the outer 4 bit decoder and then one row is selected based on the address generated by the inner 8 bit decoder.

The Overall Latency of this design from Address_bits to the multiplexer output is 2 clock cycles. 8 bit decoder in Fig. 6.1 generates the row address after a delay or latency of one clock cycle, so the data which we wish to write should be provided with a delay element of one clock cycle. Another latency is between the row address of SRAM and multiplexer output.

For eg, if we give an Address_bit 110000000001 to 8 bit decoder, it will generate the corresponding row address after a delay of one clock cycle. The data from this location is generated at the output terminal of multiplexer after another delay of one clock cycle .

Method to reduce the simulation time while designing the memory circuitry

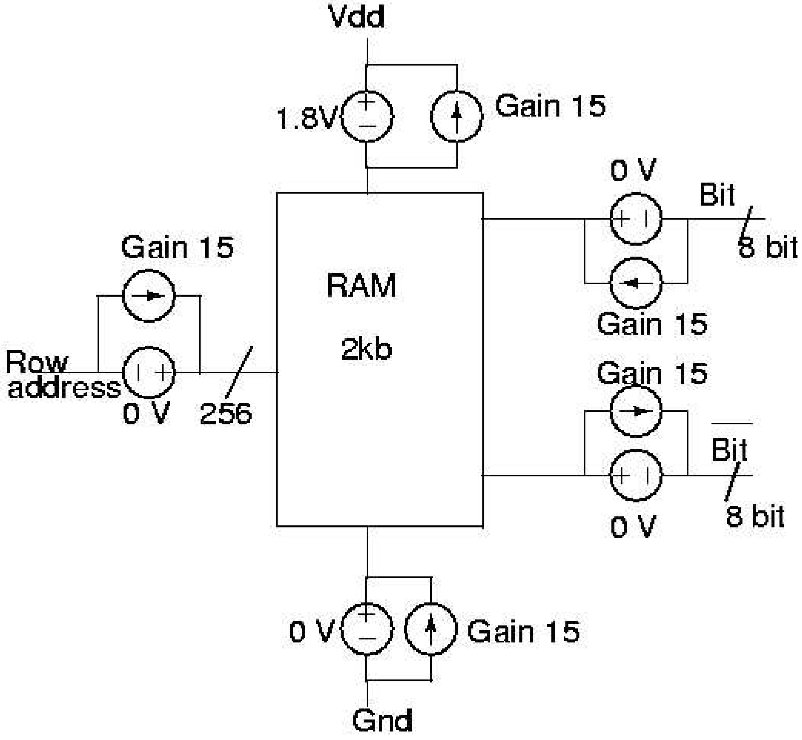


Figure 6.4: RAM of 2kb block giving a loading effect of fifteen 2kb blocks.

A 32kb SRAM is designed with sixteen, 2kb blocks. During integration of all the 16 SRAM blocks, if proper functioning of a block has to be seen then other 15 blocks should not get selected in any of the clock cycles. The loading effect of these fifteen 2kb SRAM blocks must be there otherwise, our results will be biased. If we run the simulation with proper select address then it takes a long time as the circuitry is increased. To reduce the simulation time we can introduce only two 2kb blocks instead of sixteen 2kb blocks. One block should always be selected as we want to see its functionality and the other block should give us the required loading effect . To get this, current controlled current source with a gain of 15 can be used. First calculate the current required in a 2kb block which is not accessed at any point of time, then make the current source equal to that value with a gain of 15, this can give us a capacitive loading effect of fifteen 2kb blocks with a reduced simulation time as shown in Fig. 6.4.

CHAPTER 7

Simulation Results of 32kb SRAM

7.1 Row address generated by decoders

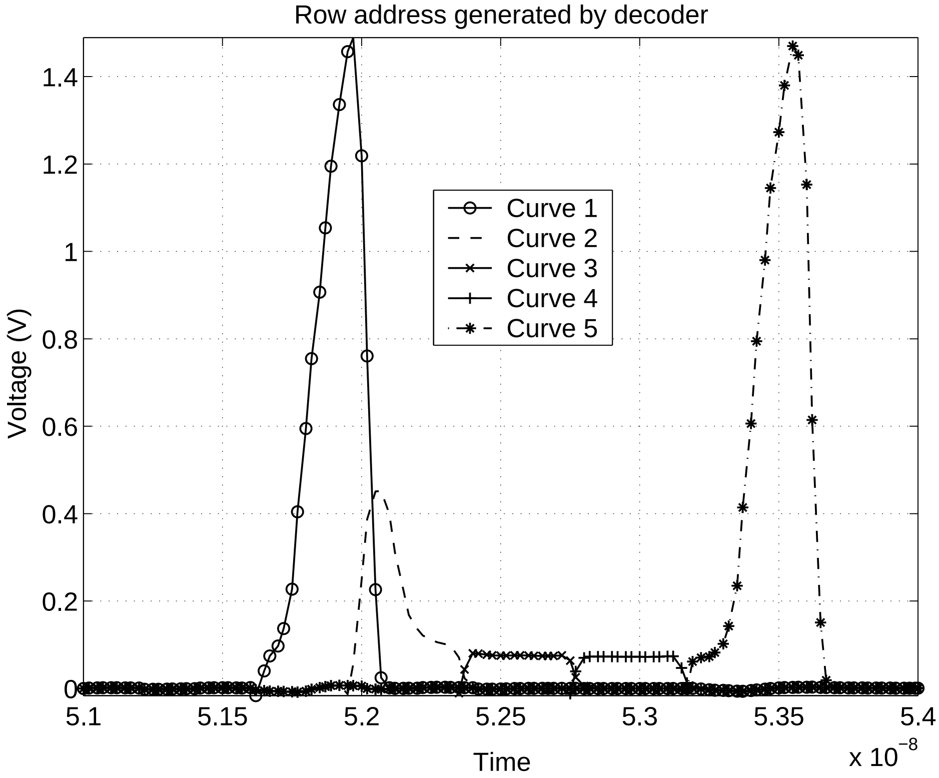


Figure 7.1: Row address generated to select one 8kb SRAM block

The simulation results are shown for a particular input pattern (Fig. 6.3), there are four 8kb RAM blocks, which are selected one by one in every 4 clock cycles. The above Fig. 7.1 represents the row address that is generated once in every 4 clock cycles to select that particular (8kb RAM) block 1 .

Curve 1 and 5 show the row addresses of about 1.5 V swing generated between 51.6ns to 52ns and 53.2ns to 53.6ns once in every 4 clock cycles.

Curve 2, 3 and 4 show the row addresses generated for three consecutive clock cycles i.e between 52ns and 53.2ns, which do not have enough swing to access the cell.

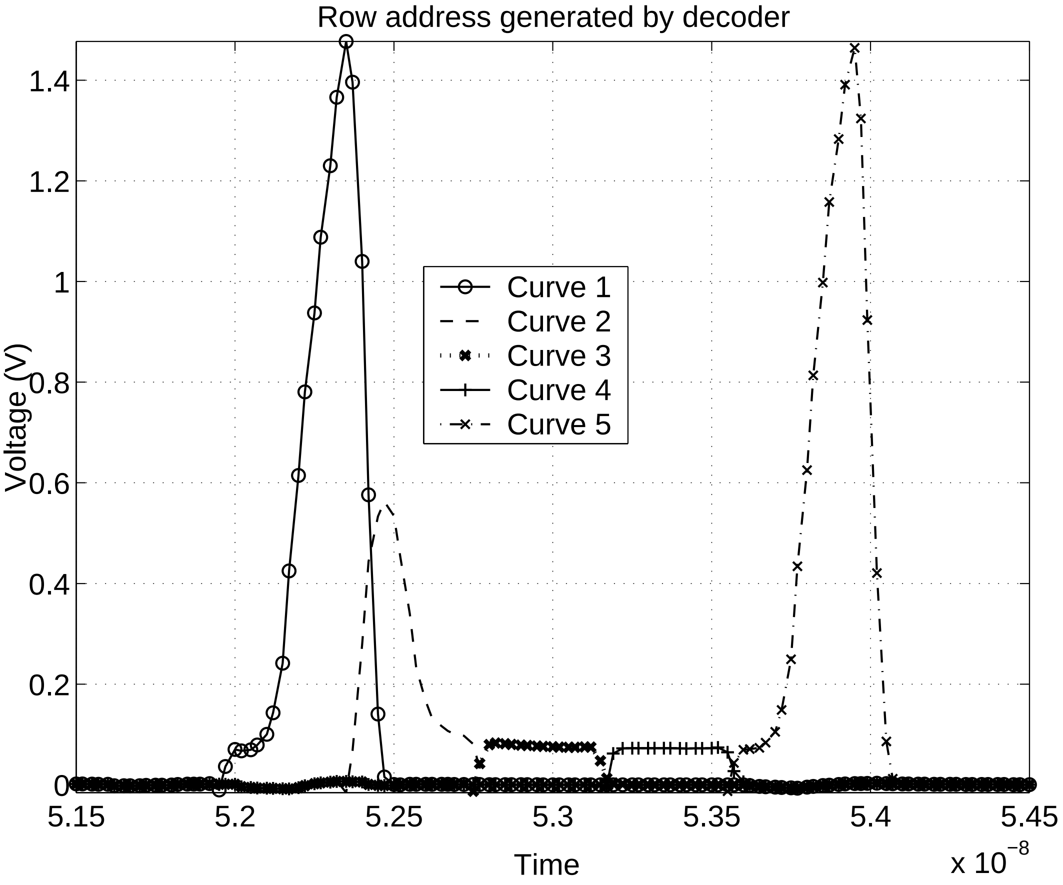


Figure 7.2: Row address generated to select second 8kb SRAM block

The Fig. 7.2 represents the row address that is generated to select other (8Kb RAM) block2 .

Curve 1 and 5 show the row addresses of about 1.5 V swing generated between 52ns to 52.4ns and 53.6ns to 54ns. Note :- here second RAM block is getting selected after first RAM block (which was between 51.6ns to 52ns)
Curve 2, 3 and 4 show the row addresses generated between 52.4ns and 53.6ns, which are not enough to access the cell.
Similarly, third and fourth RAM block is being selected between 52.4ns to 52.8ns and 52.8ns to 53.2ns respectively, then again first block gets selected as can be seen in previous Fig. 7.1 .

7.2 Writing pattern to the 6T cell

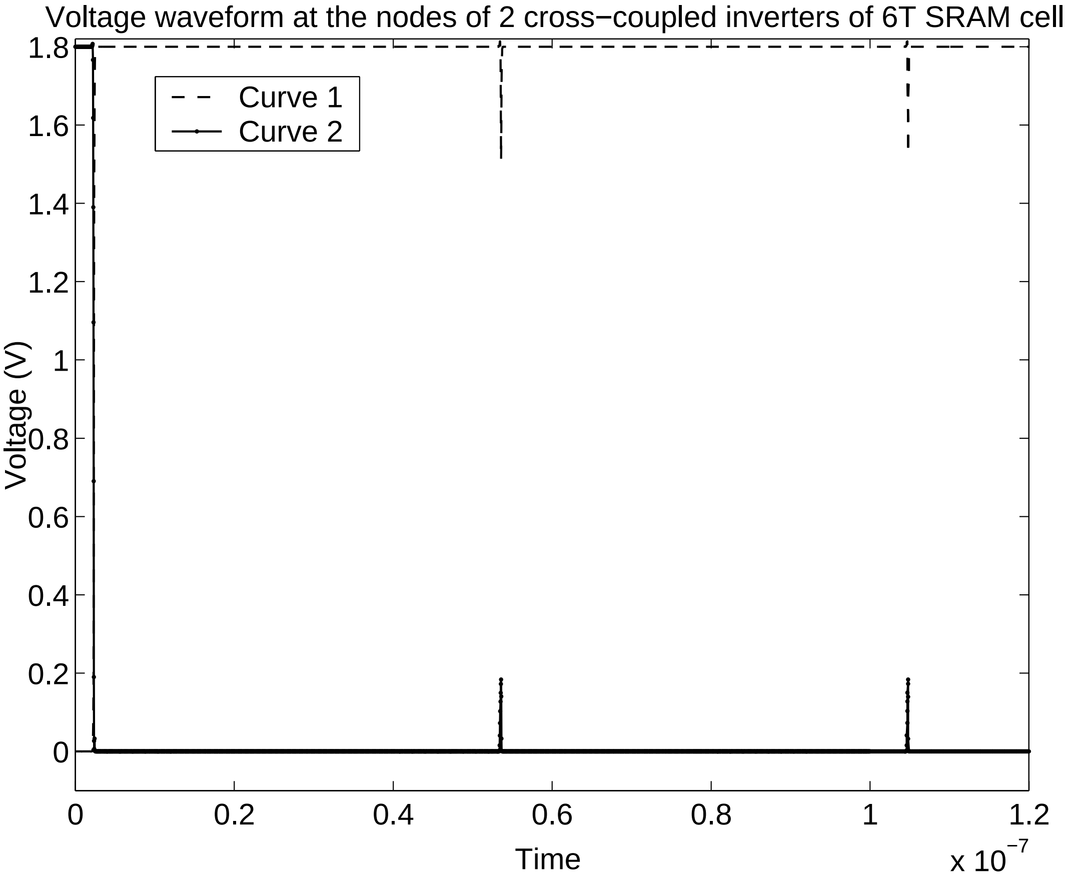


Figure 7.3: Voltages from the internal nodes of 6T SRAM cell.

Curve 1 shows the bit line voltage, around 2ns its voltage is driving to 0V showing writing bit 0 to the cell, it also shows the voltage fluctuations at 2 instances which is an attempt to read the cell .

Curve 2 shows the $\overline{\text{bit}}$ line voltage, around 2ns its voltage is driving to 1.8V showing writing bit 1 to the cell, it also shows the voltage fluctuations at 2 instances which is an attempt to read the cell .

7.3 Writing and reading 100100..pattern

Suppose we want to write a particular input pattern 100100100100100100100100. It means when block 1 of (8kb) is selected then 1 should be there for 4 clock cycles as next address will appear after 4 clock cycles, (see Fig. 7.1) and 00 should be there for 8 clock cycles. Output of first sense amplifier should show 1111000000001111... during read cycles, similarly output of second, third and fourth sense amplifier should show 00000000011110000... , 0000000011110000... , 1111000000001111... respectively but the multiplexer output should show the read pattern as 100100100100100100100100....

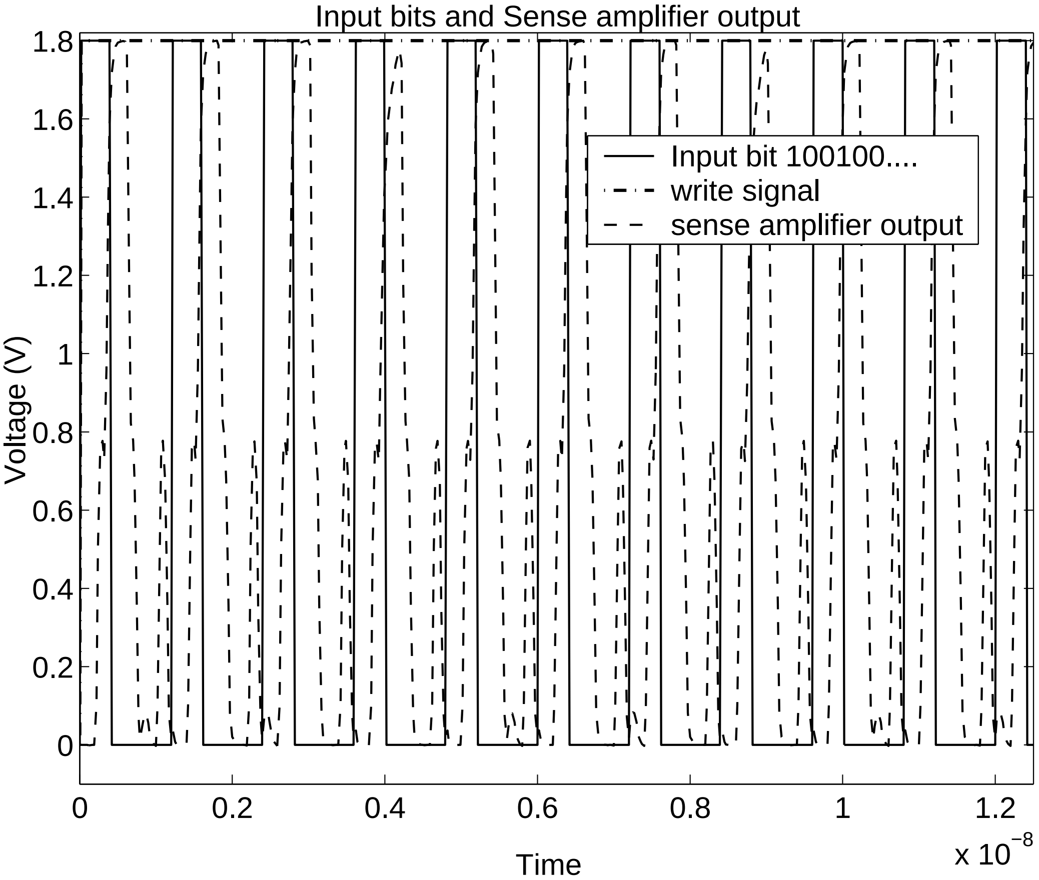


Figure 7.4: Write pattern (100100...) to the SRAM cell

Curve 1 shows the input bits 100100100100 which is to be written.

Curve 2 shows that write signal is high during this part of the curve.

Curve 3 shows the actual waveform of write bits 100100100100 and so on.

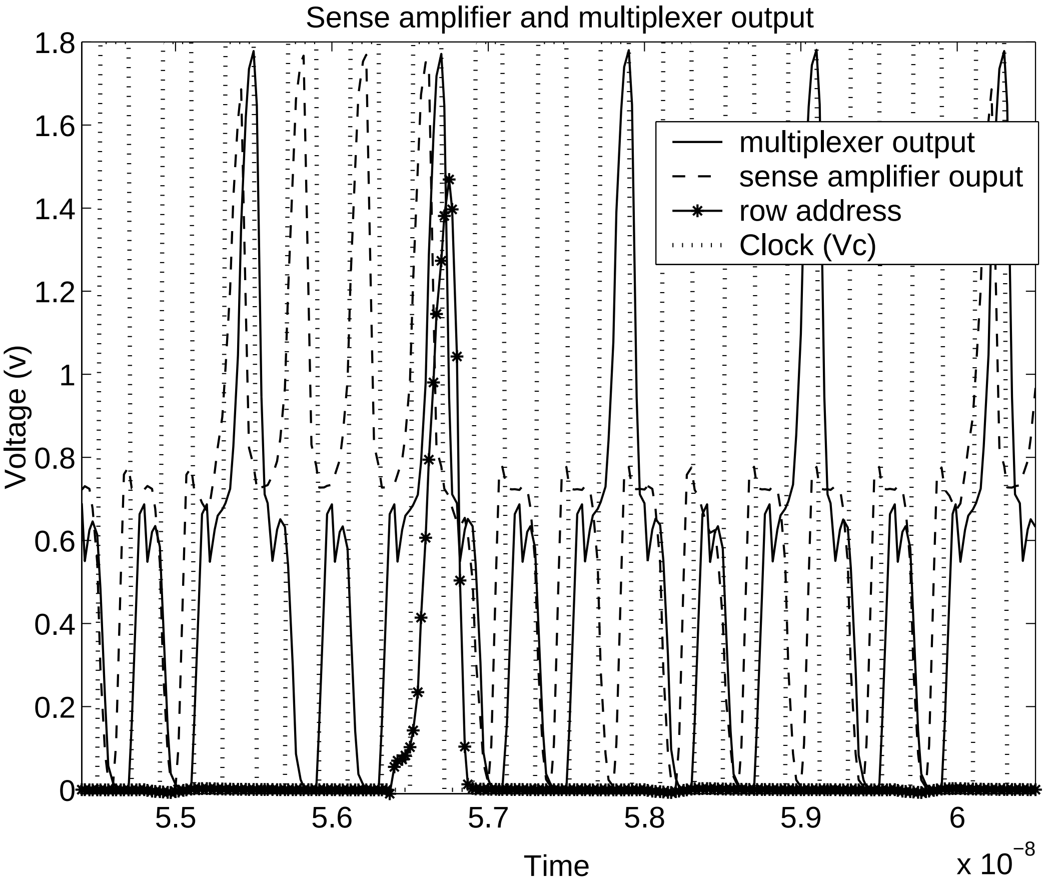


Figure 7.5: Sense amplifier and multiplexer output

Curve 1 shows the final data across the output terminal of multiplexer which is 100100100100.

Curve 2 shows the zoomed-in version of senseamplifier output showing value to be 111100000000 and so on.

Curve 3 shows the row address and the transition between sense amplifier and the multiplexer output.

Curve 4 shows the clock of frequency 2.5GHz. .

Fig. 7.5 shows that the output of multiplexer is achieving full rail to rail swing at the speed of **2.5GHz** during cadence simulation.

7.4 Writing and reading 101010..pattern

To check the proper functioning of the SRAM, worstcase input pattern should be applied. Give input data as 1010101...., here also argument is the same as we discussed in the previous example.In cycle 1 input is 1 goes to 8kb block1. In cycle 2 input is 0 goes to 8kb block 2. In cycle 3 input is 1 goes to 8kb block3. In cycle 4 input is 0 goes to 8kb block 4. In cycle 5 input is 1 goes to 8kb block1 this procedure gets repeated as long as write signal is high. First block should always show 1111111...as whenever this block gets selected only bit 1 is to be written, similarly second, third and fourth SRAM block should show 0000000...., 1111111..., 0000000..respectively during read cycle.

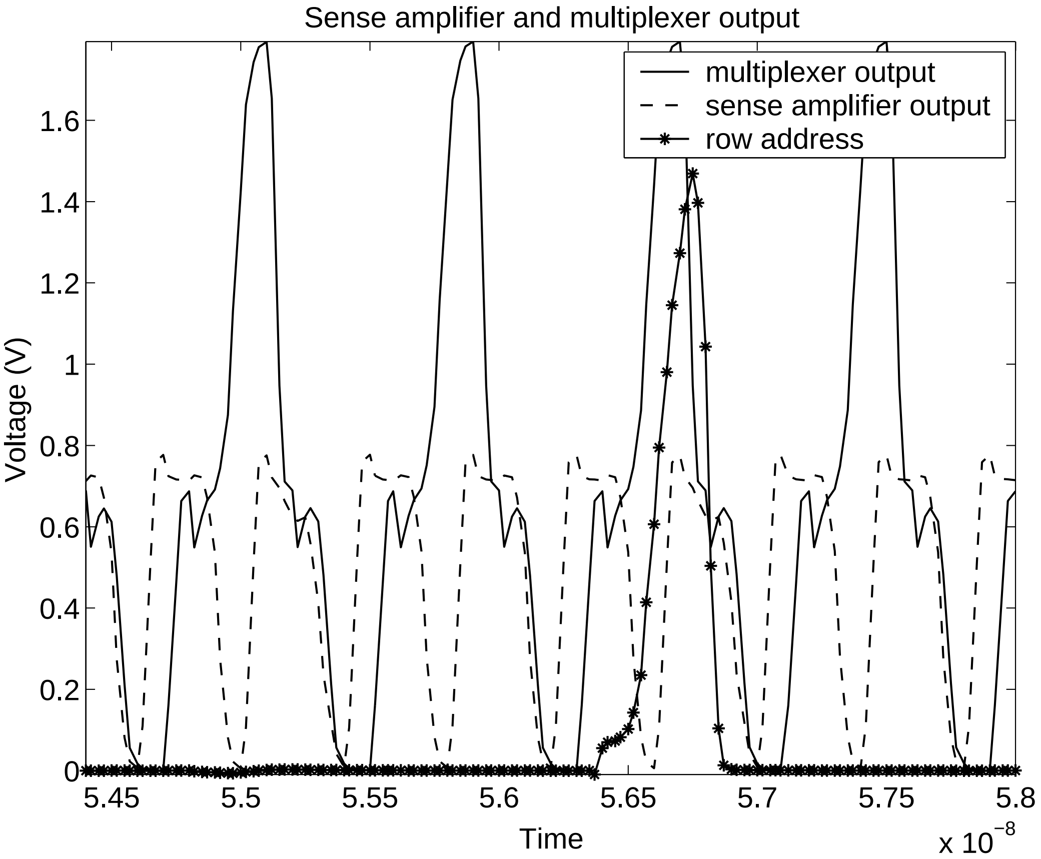


Figure 7.6: Sense amplifier and multiplexer output for the 1010... input pattern

Curve 1 shows the correct data 1010.. at the output terminal of multiplexer with a swing of 1.8V.

Curve 2 shows the output of sense amplifier having a pattern of 00000...

Curve 3 shows the row address and the transition of output voltage from 1 to 0 .

7.5 Overall latency of SRAM

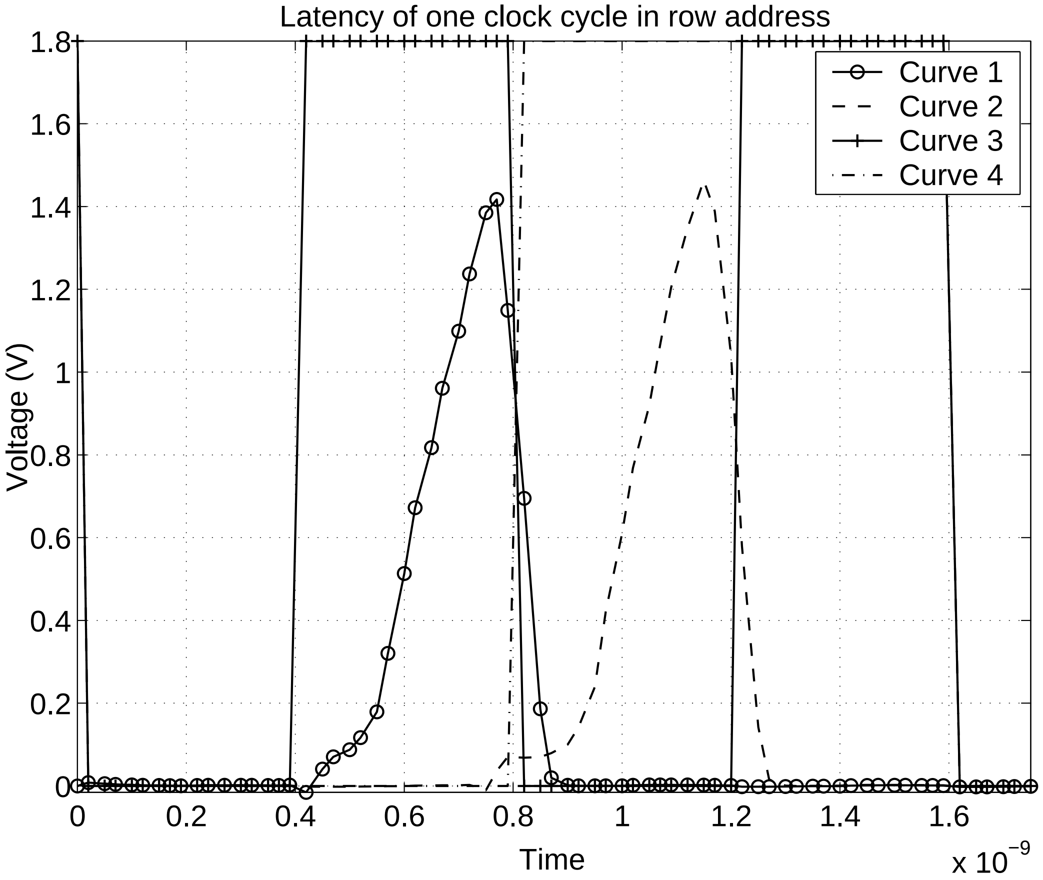


Figure 7.7: Latency of one clock cycle between Address_bits given to decoder and row address generated by it

Curve 1 shows the row address corresponding to the Address 0.

Curve 2 shows the row address corresponding to the Address 1.

Curve 3 shows the address_bits corresponding to the Address 0.

Curve 4 shows the address_bits corresponding to the Address 1.

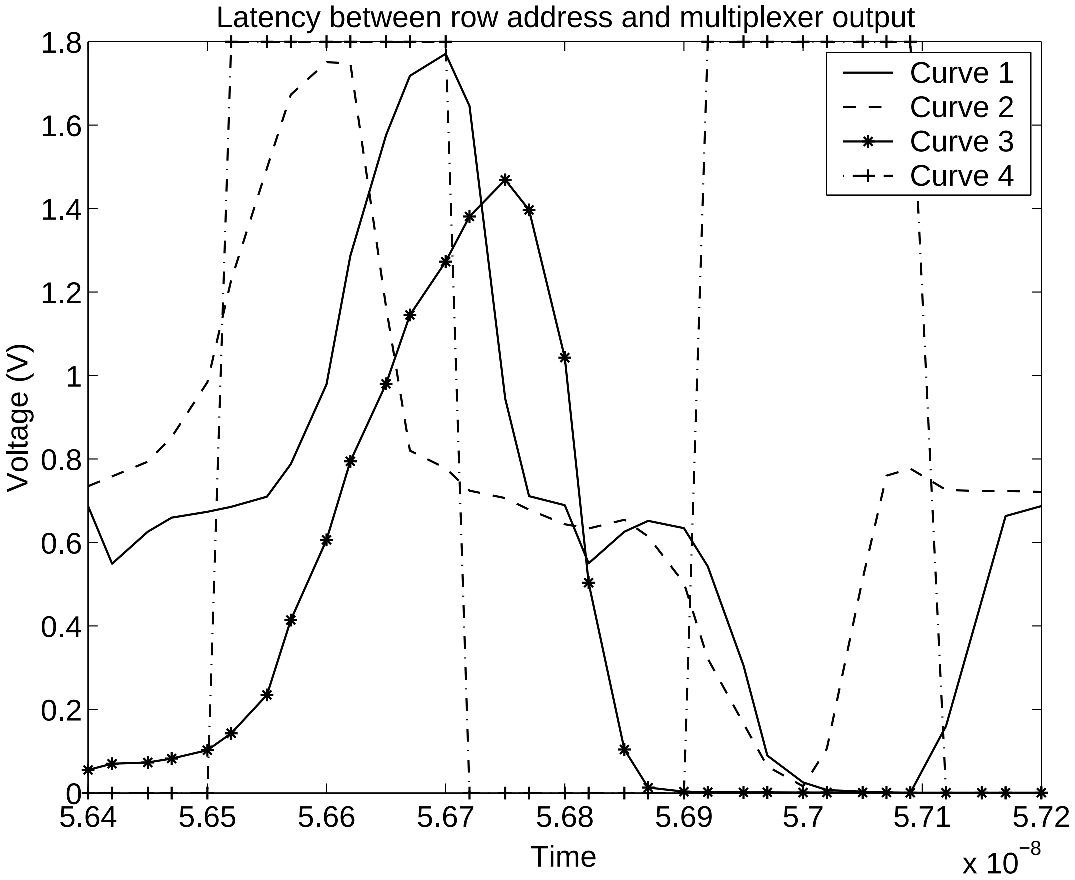


Figure 7.8: Latency of one clock cycle between row address generated by decoder and the output of multiplexer.

Curve 1 shows the output of the multiplexer.

Curve 2 shows the output of the sense amplifier.

Curve 3 shows the row address generated by the decoder.

Curve 4 shows the clock of 2.5GHz.

Fig. 7.7 and Fig. 7.8 shows that there is a latency of one clock cycle between the output and the row address and another latency between the row address and the output of multiplexer, therefore **the overall latency comes out to be 2 clock cycle**.

7.6 Amplification stage of sense amplifier

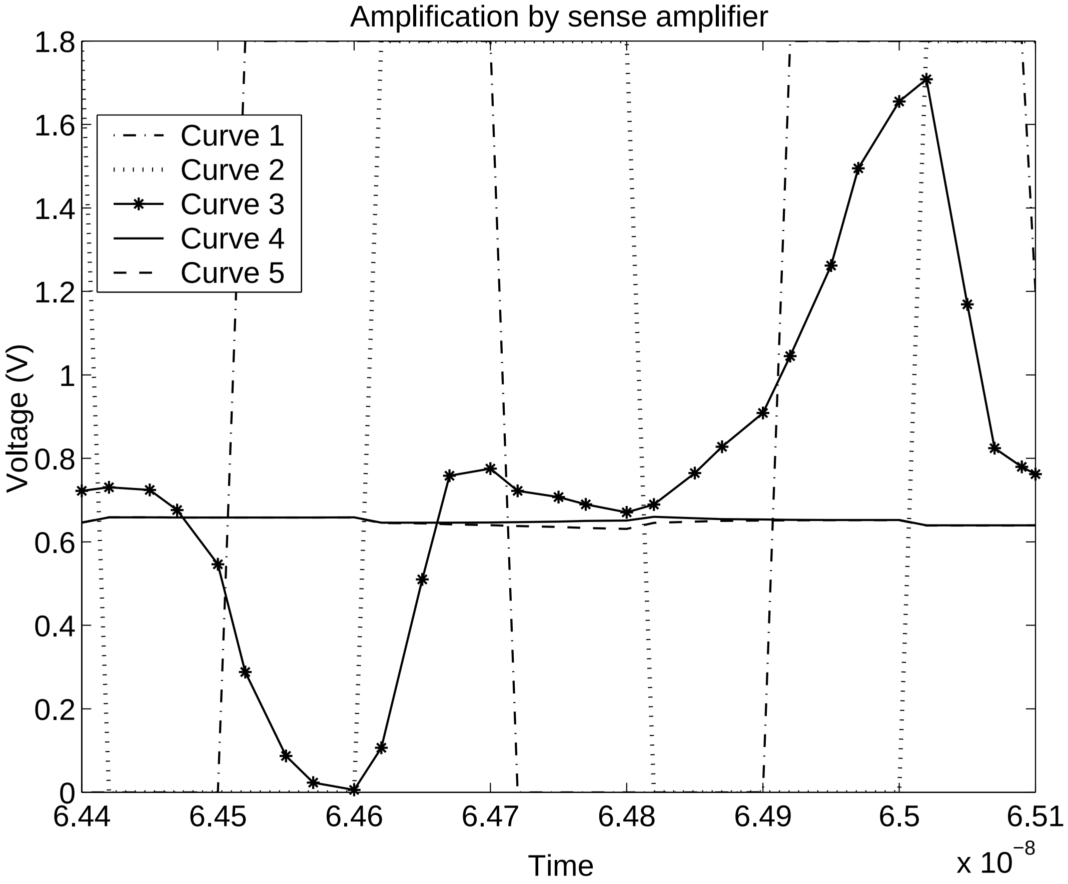


Figure 7.9: Amplification of bit line voltage by sense amplifier

Curve 1 shows when Vc(clock) is low and v_sense is high the signal is applied to the sense amplifier.

Curve 2 shows the regeneration period of sense amplifier, here v_sense is low.

Curve 3 shows the sense amplifier output, which is changing from 0 to 1.8V.

Curve 4 shows the bit line voltage .

Curve 5 shows the $\overline{\text{bit}}$ line voltage.

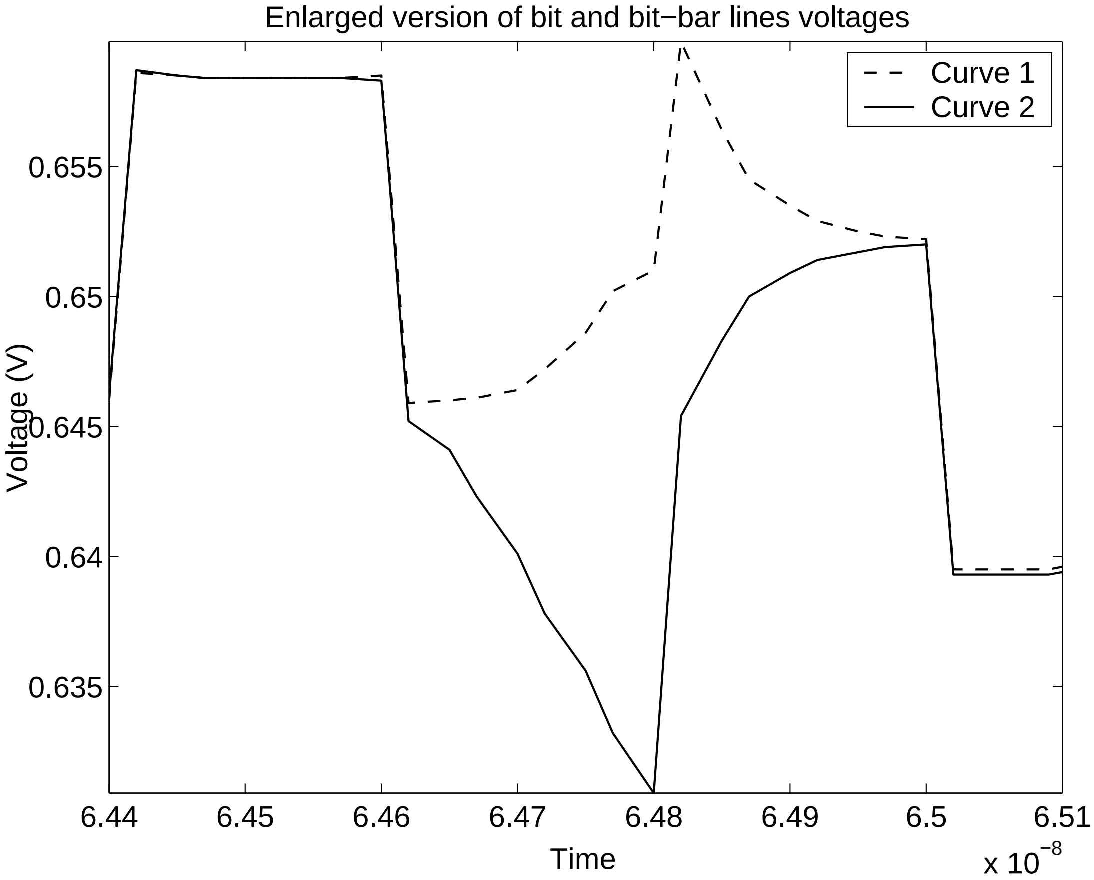


Figure 7.10: Enlarged version of differential input to the sense amplifier

Curve 1 shows the enlarged version of the bit line voltage .

Curve 2 shows the enlarged version of the $\overline{\text{bit}}$ line voltage.

Thus,**the sense amplifier which is designed in Fig. 4.1 is amplifying approximately (20mV to 1.7V) in a period of half a clock cycle or in other words in 200ps.**

CHAPTER 8

Registers

8.1 Register using D flipflop

D Flipflop

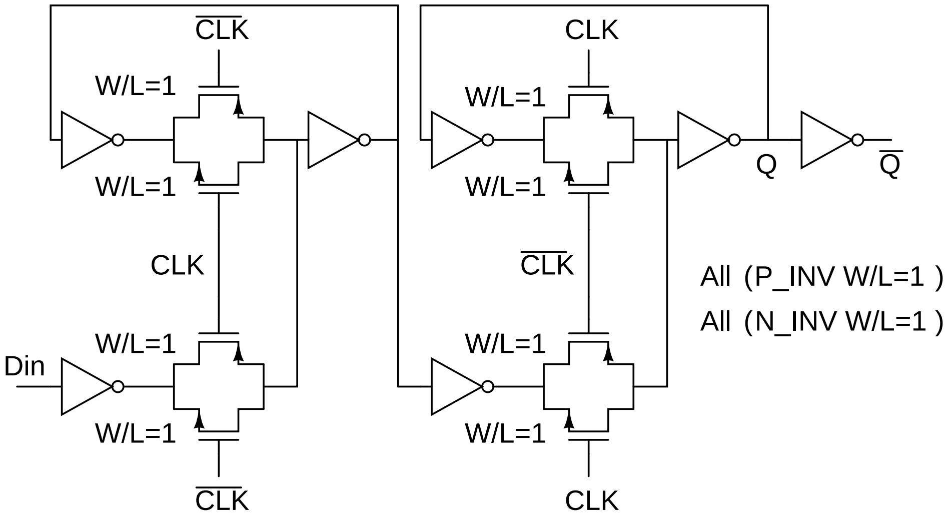


Figure 8.1: D flipflop used to design register

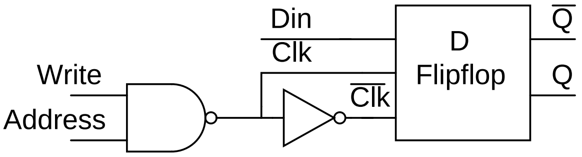


Figure 8.2: One bit register

D flipflop

The above flipflop shown in Fig. 8.1is based on feedback logic, it is designed using (W/L = 1) for NMOS and PMOS transistors. Here input can be latched to the output when $\overline{\text{CLK}}$ becomes high. As there is positive feedback during CLk, it doesn't lose its data and hence it can be used at very low speeds.

single bit Register

The register shown in Fig. 8.2 is designed using inverters, transmission gates and D flipflop.

During write operation, first Data-in should be present at the input bus, then control address should produce through the use of decoders, after that make write signal high so that new data can be written to the D flipflop.

During read operation, make sure that write signal is low so that the output cannot be changed even if there is a change in input data .

8.2 8 bit Register

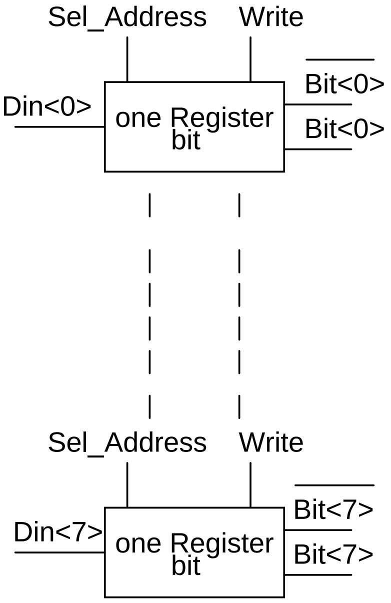


Figure 8.3: One byte register

8 bit Register

The above 8 bit register shown in Fig. 8.3 is designed using 8 single bit register, here the input and output bus are of 8 bit. The control signals and working procedure are similar to that of the single bit register.

8.3 16 byte register file

RAM of 16 x 8 Bits

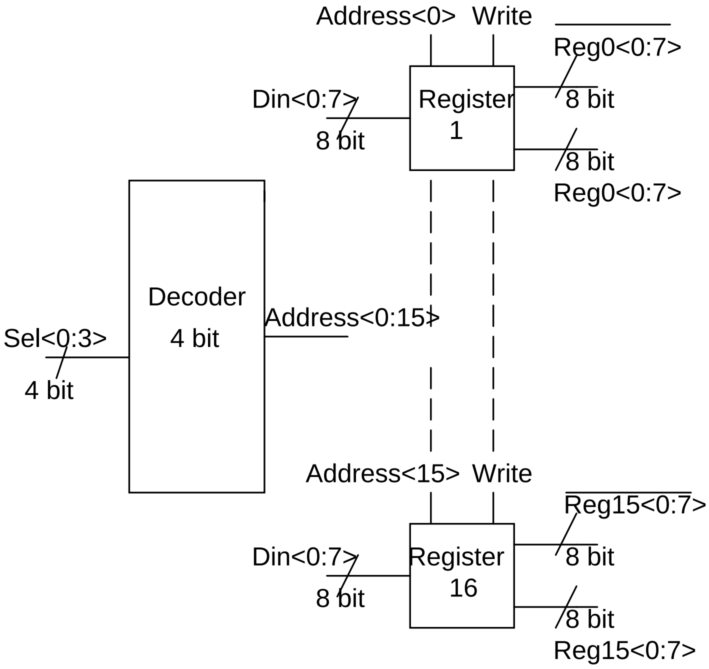


Figure 8.4: Memory consisting of 16 registers

RAM of 16 registers

The above Fig. 8.4 is the design of RAM using 16 registers. One 4 bit decoder is used here to access 16 different locations or, in other words, 16 registers. At any time all the registers outputs are available at 16 different output buses. if, we wish to write a particular register then 8 bit data should be present at the input bus. Generate the select address from the 4 bit decoder, followed by write signal. This will rewrite that particular register whose address is generated by the decoder, all other registers will remain unchanged.

CHAPTER 9

Layout of 16 byte register file

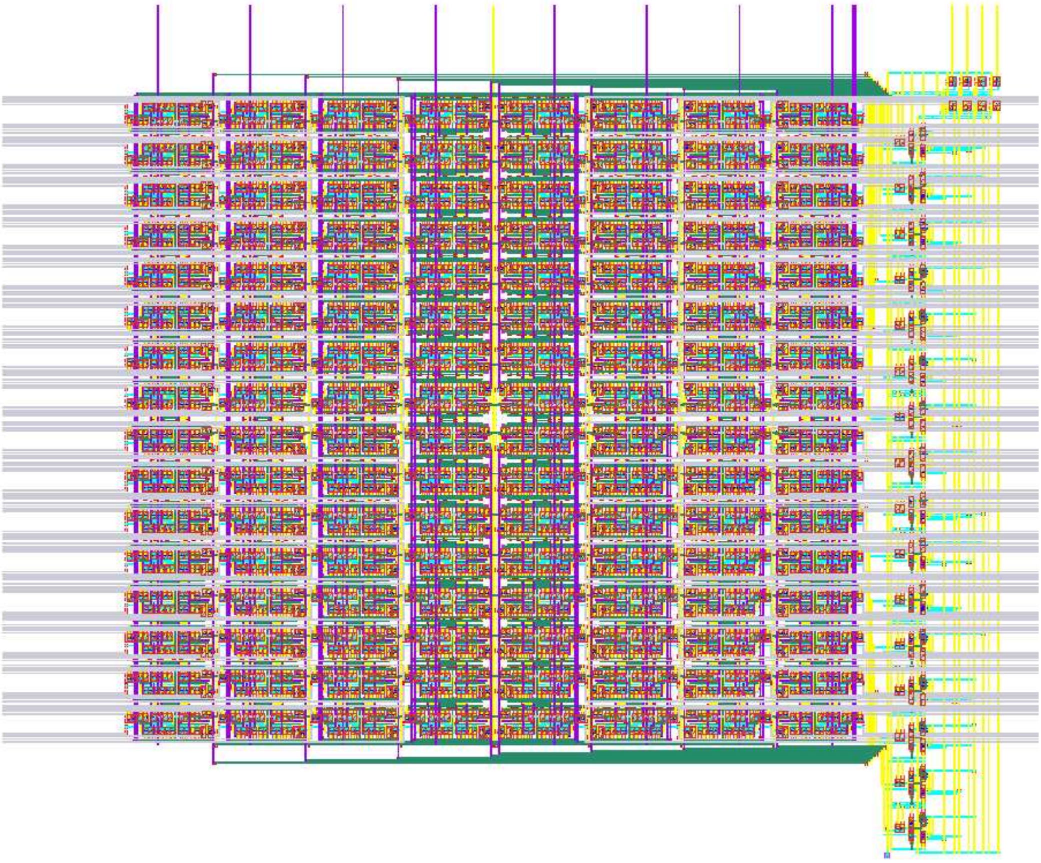


Figure 9.1: Layout of RAM consisting of 16 registers

CHAPTER 10

Experimental results of 16 byte register file

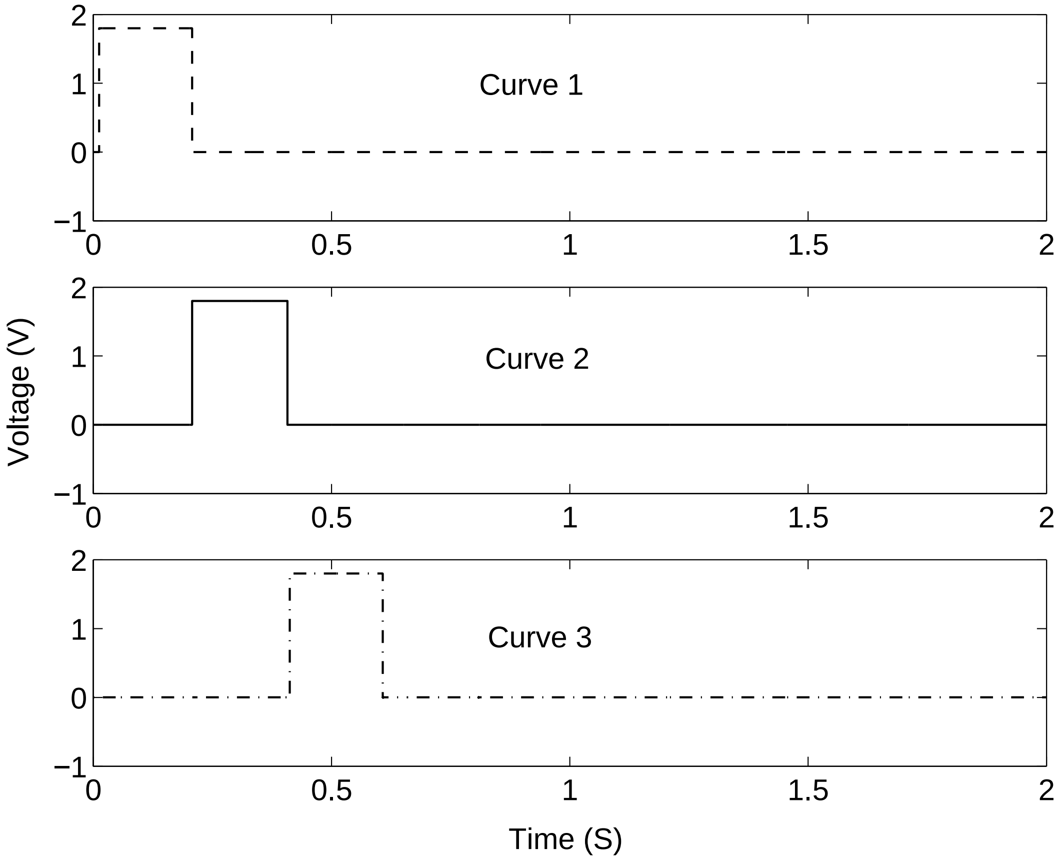


Figure 10.1: Row address for registers 1,2 and 3 .

Curve 1 shows the row address for register1.

Curve 2 shows the row address for register2.

Curve 3 shows the row address for register3.

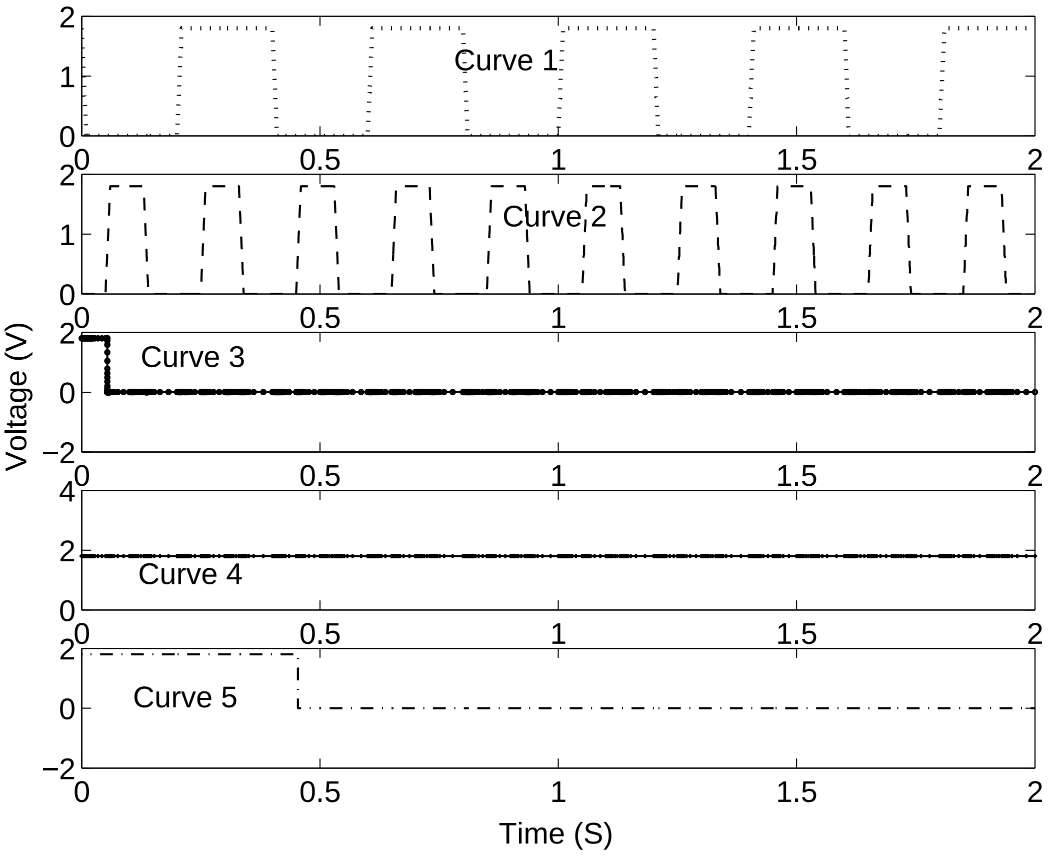


Figure 10.2: Output of 16 byte register file when input and write signal are changed

Curve 1 shows the data input given to the registers.

Curve 2 shows the Write input given to the registers.

Curve 3 shows the content of register1, which is changing from 1 to 0 as Data input is 0 when write and sel_ address pulse appears refer Fig. 10.1.

Curve 4 shows the content of register2, which is remains at 1 , as Data input is 1 when write and sel_ address for this register appears refer Fig. 10.1.

Curve 5 shows the content of register3, which is also changing from 1 to 0 as Data input here is 0 when write and sel_ address for this register appears refer Fig. 10.1.

Note: The contents of register are static and remains unchanged unless write signal and row address appears.

CHAPTER 11

Conclusions

The 32Kb SRAM which is discussed in this report is running at 2.5GHz on cadence simulation' but its layout is not done so it is likely to run at lower speed. [4] discusses 16kb memory at 1.1GHz using 0.18um CMOS technology. The total power dissipation in the designed SRAM is 550mW after simulation but, after doing layout this is likely to change.

The RAM of 16 registers which is discussed can work at speed as low as few Hz.

Table 11.1: Key results of 32kb SRAM and 16 byte register memory.

$Parameter$	$32kbSRAM$	$16byteregister$
CMOS Technology	0.18μm	0.18μm
Memory Size	To be determine after layout	0.22x0.25mm^2
Power supply	1.8V	1.8V
Total average Power dissipation	550mW @ 2.5GHz	56μW @ 5Hz

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