Design of a Thermocouple Signal Conditioner

A THESIS

submitted by

DEEPA DEVENDRAN

for the award of the degree

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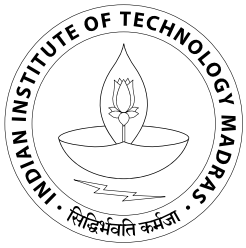
MASTER OF SCIENCE

(by Research)



Department Of Electrical Engineering
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March 2010

CERTIFICATE

This is to certify that the thesis titled **Design of a Thermocouple Signal Conditioner** , submitted by **Deepa Devendran**, to the Indian Institute of Technology Madras, for the award of the degree of **Master of Science**, is a bona fide record of the work done by her under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Date: 30 March 2010

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ABSTRACT

This thesis describes the design of a low noise, low offset amplifier using chopper stabilization. Low-offset amplifiers are widely used in measurement systems. Typical applications include strain gauges, thermocouples, photodiodes etc. In CMOS process, offset and 1/f noise are primary bottlenecks that severely limit the accuracy and dynamic range of such amplifiers. Chopping is used to modulate the offset and 1/f noise to higher frequencies after which it can be easily filtered out, providing continuous offset reduction.

An illustrative CMOS prototype of a chopper stabilized amplifier in a 0.18 μm process is presented which achieves an input referred noise of 1 μV in 1 Hz to 1 kHz bandwidth. It consumes 0.65 mW of power and occupies 0.215 mm^2 of area.

The offset after chopping is not zero since the mismatch between the cascode devices in the first stage opamp is not chopped. Also the residual offset drifts with time and temperature. This is corrected using nested chopping which employs two levels of chopping wherein lower and more stable residual offsets can be attained.

Finally a full system design required to measure signal from a K type thermocouple is illustrated. This involves the design of a chopper amplifier, a cold junction compensation buffer, an oscillator and finally an output differential to single ended converter. The integrated circuit designed in 0.35 μm CMOS process has an output sensitivity of 2 mV/^{o}C. The chopper amplifier, CJC buffer and output differential to single ended converter consumes 1.98 mW, 2 mW and 1.935 mW of power respectively. The thermocouple signal conditioning block consumes around 6 mW occupying 1 mm^2 of area.

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ABBREVIATIONS

RTD	Resistance Temperature Detectors
DAB	Digital Audio Broadcasting
CJC	Cold Junction Compensation
ADC	Analog to Digital Converter
IC	Integrated Circuit
SPICE	Simulation Program with Integrated Circuit Emphasis
PSS	Periodic Steady State
PAC	Periodic AC Analysis
IDFT	Inverse Discrete Fourier Transform
i.i.d	Independent Identically Distributed
NMC	Nested Miller Compensation
RHP	Right Half Plane
CMRR	Common Mode Rejection Ratio
PSRR	Power Supply Rejection Ratio
UMC	United Microelectronics Corporation
MPW	Multi Project Wafer
PCB	Printed Circuit Board
JLCC	J- Leaded Chip Carrier
DSM	Delta Sigma Modulator
OA	Opamp
DE-SE	Differential to Single Ended converter

CHAPTER 1

Introduction

A sensor is a device that receives a signal or stimulus and responds with an electrical signal. Sensors and their associated circuits are used to measure various physical properties such as temperature, force, pressure, flow, position, light intensity etc. These properties act as the stimulus to the sensor, and the sensor output is conditioned and processed to provide the corresponding measurement of the physical property. Sensors may be classified in a number of ways. From a signal conditioning viewpoint it is useful to classify sensors as either active or passive. An active sensor requires an external source of excitation. Resistor-based sensors such as thermistors, resistance temperature detectors (RTDs), and strain gauges are examples of active sensors, because a current must be passed through them and the corresponding voltage measured in order to determine the resistance value. An alternative would be to place these devices in a bridge circuit. In either case, an external current or voltage is required. On the other hand, passive (or self-generating) sensors generate their own electrical output signal without requiring external voltages or currents. Examples of passive sensors are thermocouples and photodiodes which generate thermoelectric voltages and photocurrents. The outputs of most sensors (passive or active) are small voltages, currents, or resistance changes, and therefore their outputs must be properly conditioned before further analog or digital processing can occur. Because of this, an entire class of circuits has evolved, generally referred to as signal conditioning circuits. Amplification, level translation, galvanic isolation, impedance transformation, linearization, and filtering are fundamental signal conditioning functions that may be required. Whatever form the conditioning takes, the circuitry and performance will be governed by the electrical characteristics of the sensor output. Accurate characterization of the sensor in terms of parameters appropriate to the

application like sensitivity, voltage and current levels, linearity, impedances, gain, offset, drift, time constants, maximum electrical rating must be done.

A quite common application of sensors is within process control systems. One example would be the control of a physical property, such as temperature. In such a system the output from a temperature sensor will be conditioned, transmitted over some distance, received, and then used appropriately.

1.1 Thermocouple Principle

Thermocouples are widely used in many applications from simple stand alone temperature measurements to data acquisition systems present in industrial process control (many data acquisition modules accept thermocouple inputs directly apart from voltage and current inputs, eg: RS-485 DAB). They are the most popular type of temperature sensor because they are cheap, have interchangeable connectors, and they can measure a wide range of temperatures. Using different thermocouples, it is possible to measure temperatures over a very wide range of temperatures, from below -250 ^{o}C to above 2500 ^{o}C. The levels of accuracy that can be achieved are also high, typically between 0.5 ^{o}C and 2 ^{o}C.

In operation, thermocouples rely on the fact that two dissimilar metals joined together produce a voltage output roughly proportional to temperature. They are more linear than many other sensors, and their non-linearity has been well characterized. The most common metals used for thermocouples are iron, platinum, rhodium, rhenium, tungsten, copper, alumel (composed of nickel and aluminium), chromel (composed of nickel and chromium) and constantan (composed of copper and nickel). A variety of thermocouples are available suitable for different applications. They are selected based on temperature range and sensitivity needed. Type J thermocouples are the most sensitive, producing the highest output voltage for a given temperature change, but over a relatively narrow temperature span. On the

other hand, Type S thermocouples are the least sensitive, but can operate over a much wider range. Type K - Chromel/Alumel, is the most commonly used general purpose thermocouple since it is relatively linear compared to the other type of thermocouples. A Type K thermocouple exhibits a sensitivity of approximately $40\,\mu\mathrm{V}/^{o}\mathrm{C}$. Hence thermocouples produce only millivolts of output, and thus they typically require precision amplification for further processing.

1.1.1 Cold Junction compensation

Thermocouples measure the temperature difference between two junctions and not absolute temperature of the source. Hence one of the junctions the cold junction is maintained at a known (reference) temperature, while the other junction is at the temperature to be sensed. Having available a known temperature cold junction is possible for laboratory calibrations but it is simply not convenient for most directly connected indicating and control instruments. Instead, they incorporate into their circuits an artificial cold junction using some other thermally sensitive device (such as a thermistor or diode) to measure the ambient temperature of the instrument. This signal from the temperature sensor of another sort that measures the cold

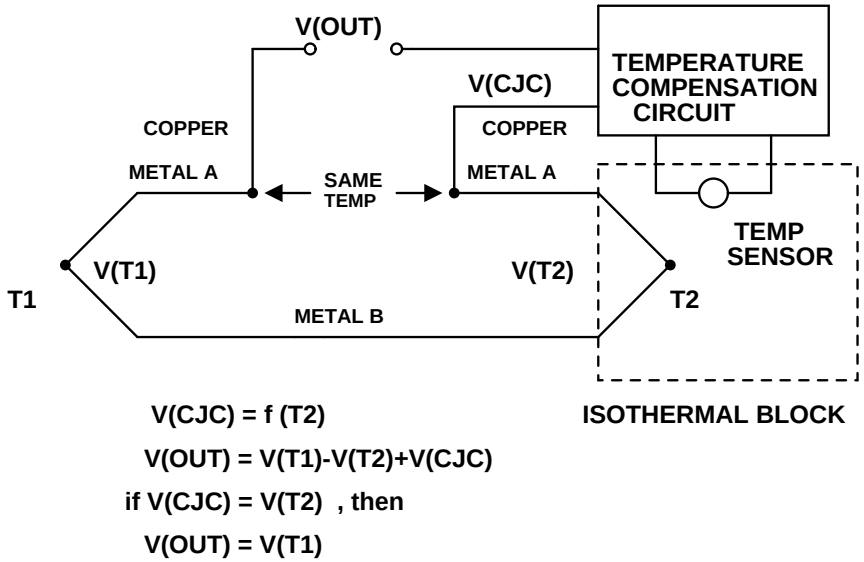


Figure 1.1: A semiconductor sensor can be used to provide cold junction compensation

junction is added with thermocouple signal from which the actual temperature

of the source can be determined as shown in Fig. 1.1 [1]. This is known as Cold Junction Compensation (CJC).

Signal conditioning blocks are primarily needed to manipulate an analog signal in such a way that it meets the requirements of the next stage for further processing. In performing this conversion a number of functions may take place [2]. They include:

Amplification Amplification increases the resolution of the input signal. Thermocouple sensors generate very low output voltage signals (in the range of few millivolts) which is too low for an Analog-to-digital converter (ADC) to process directly. In this case it is necessary to bring the voltage level up to that required by the ADC.

Electrical Isolation Electrical isolation breaks the electrical path i.e., there is no physical wiring between the input and the instrumention block. The input is normally transferred by converting it to an optical or magnetic signal then it is reconstructed before being processed by the measuring block. By such isolation, unwanted signals on the input line are prevented from passing through to the output. Isolation is required when a measurement must be made on a surface with a voltage potential far above ground. Isolation is also used to prevent ground loops which can introduce relatively large errors in the readings.

Linearization Converting a non-linear input signal to a linear output signal. This is common for thermocouple signals.

Filtering A thermocouple can act very much like an antenna, making it very susceptible to noise from nearby 50 Hz power sources. Therefore, it is recommended to apply a low-pass filter to the thermocouple signal to remove this noise.

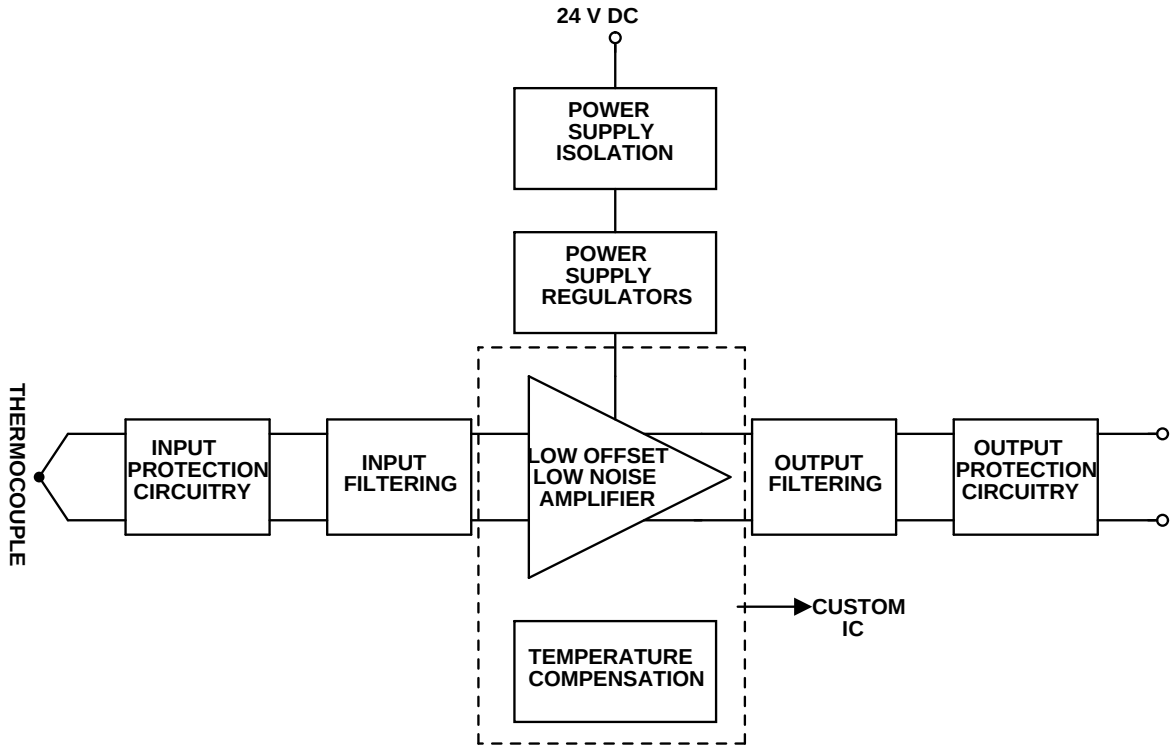


Figure 1.2: Thermocouple measurement system

A thermocouple measurement system shown in Fig. 1.2 requires amplification with low noise and offset for accurate temperature measurements, cold junction compensation circuitry for measurement of absolute temperature, and high isolation between thermocouple, power supply, and output sections to be able to be used effectively in harsh environments. Realization of the amplifier on an integrated circuit provides for scalability to a large number of sensors and an indigenous design of a suitably accurate amplifier. The goal of this work is to understand different methods of realizing a low noise, low offset amplifier and to design one such integrated circuit amplifier with a provision for cold junction compensation. The gain and noise requirements are calculated suited to a K-type thermocouple. Such a design can also be ported to other types of thermocouples with suitable adjustment of parameters. The design can also be useful for other sensors which require sensitivities in the microvolt range.

1.2 Organization

In this work we concentrate our efforts in building an IC that incorporates the low offset, low noise amplifier and a room temperature compensation block as shown within the dotted box in Fig. 1.2. This thesis is organised as follows - Chapter 2 describes various techniques to eliminate offset and 1/f noise. Chapter 3 deals with the design of a three-stage high gain opamp which is used to build an amplifier that amplifies the thermocouple signal. In Chapter 4, test results of the fabricated design are given. Chapter 5 discusses in detail the design of a complete thermocouple signal conditioning block with simulated results of the same. Chapter 6 gives the conclusions.

CHAPTER 2

Circuit Imperfections & Cancellation Techniques

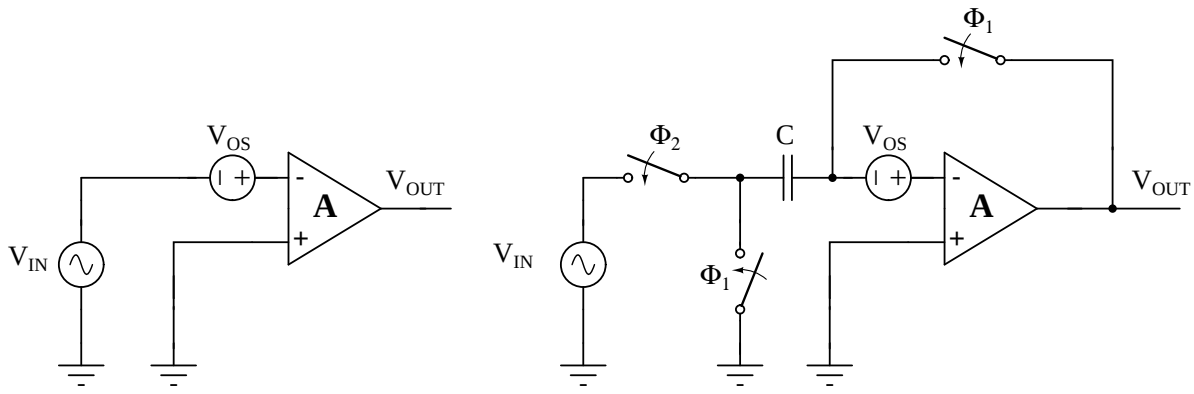
Thermocouple signal conditioners can be constructed with opamps and other passive circuit elements. Most of the limitations of analog circuits are due to the fact that they operate with electrical variables and not simply with numbers. Therefore, their accuracy is fundamentally limited by unavoidable mismatches between components, and their dynamic range is limited by noise, offset, and distortions. Among the non-idealities, the 1/f noise and offset are narrowband low frequency signals whereas the thermal noise occupies a wide frequency band. Since thermocouple signals are also narrowband low frequency signals, the narrowband noise sources of an opamp must be reduced in order to achieve good accuracy and dynamic range with the circuit. The following sections discuss the two basic techniques used to reduce the offset and the low frequency noise of an opamp.

2.1 Autozeroing

The basic idea of autozeroing is to sample the unwanted quantity (noise and offset) and then subtract it from the instantaneous value of the signal either at the input or the output of the opamp. Fig. 2.1(a) depicts an amplifier with offset.

$$V_{OUT} = -A(V_{IN} + V_{OS}) \tag{2.1}$$

Input referred offset voltage is amplified along with the input signal. Fig. 2.1(b) represents an autozeroed circuit wherein the offset is stored at the input terminal. Here Φ_1 is the autozeroing phase and Φ_2 is the amplification phase.



(a) Amplifier with offset (b) Autozeroing principle

Figure 2.1

During Φ_1 as shown in Fig. 2.2(a),

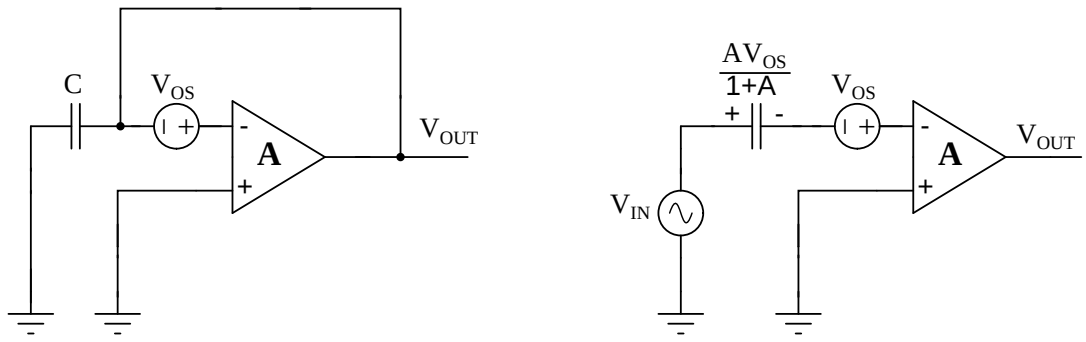
$$V_{OUT} = -A(V_{OUT} + V_{OS}) \tag{2.2}$$

$$V_{OUT} = \frac{-A}{1+A} V_{OS} \tag{2.3}$$

During Φ_2 as shown in Fig. 2.2(b),

$$V_{OUT} = -A(V_{IN} + \frac{V_{OS}}{1+A}) \tag{2.4}$$

Hence the resulting input referred offset is reduced to $\frac{V_{OS}}{1+A}$ from V_{OS}.



(a) Autozeroing phase Φ_1 (b) Amplifying phase Φ_2

Figure 2.2

Besides offset reduction, autozeroing also provides another means for performance improvement. Observe the differentiation process happening inherently during autozeroing. This is due to the sampling occurring in one clock phase, followed

by the subtraction in the next phase. As a result, this technique high pass filters the low frequency 1/f noise of the opamp, thus strongly reducing its contribution at the output of the amplifier. To remove all the 1/f noise of an amplifier the autozeroing frequency f_{AZ} must be higher than the 1/f corner frequency f_c of the amplifier. Since autozeroing involves sampling operation, there will be folding of the wideband thermal noise in the signal band which can potentially raise the noise floor [3]. Higher the bandwidth of the amplifier more is the noise that is folded and sampled back on the capacitor. The detailed analysis of the increase in noise floor due to autozeroing is shown in Appendix A.

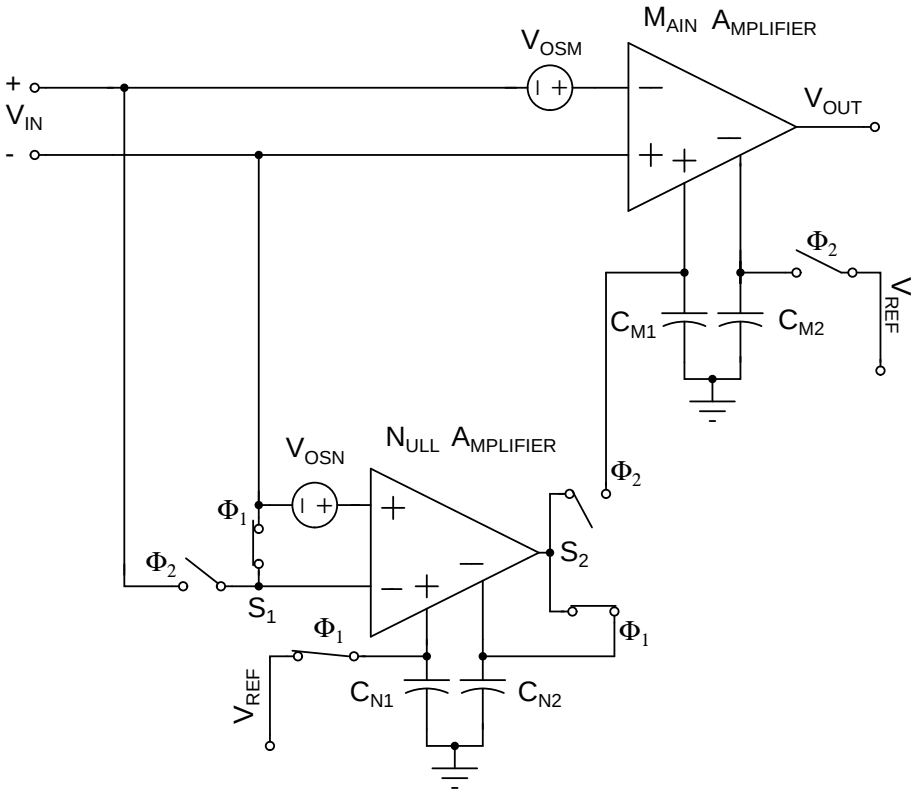


Figure 2.3: Continuous time autozeroing

Continuous time autozeroing can also be performed wherein the main amplifier remains unswitched. Such amplifiers will have two input paths, one primary input path and an auxiliary input. Two amplifiers will be required to implement the continuous time autozeroing technique as shown in Fig. 2.3. The main amplifier is unswitched and continuously amplifies the input signal. In Φ_1, the nulling amplifier

disconnects from the signal path and nulls its own offset. In Φ_2 it reconnects to the signal path to null the main amplifier's offset [4] [5].

Charge injection from the switching action cause transients that depends on the input signal, causing intermodulation distortion. Distortion is an important issue associated with autozeroed amplifiers. Any distortion component aliased down to DC will change the amplifier's apparent offset voltage. Another problem is that the signal independent charge injected by the switches will not be cancelled by the autozero mechanism further adding to the offset. To overcome the problem of charge injection the capacitor size can be made typically large. But the presence of large capacitors in the signal path will slow down the settling time of the autozeroing amplifier.

In conclusion, though autozeroing process reduces the offset, it also increases the white noise foldover component due to aliasing of the amplifier's thermal as well 1/f noise. The speed of the amplifier is also severely limited by the parasitics and the capacitors in the signal path.

2.2 Chopper Stabilization

Unlike the autozeroing technique chopper stabilization technique does not use sampling. It involves modulation of the signal to a higher frequency where there is no 1/f noise and then demodulation back to the baseband [3]. The principle is illustrated in the Fig. 2.4. As illustrated, the input signal $v_{in}(t)$ is multiplied by a square wave carrier signal $v_{clk}(t)$ with unity amplitude and 50 % duty cycle of frequency f_{CHOP}. The input signal thus gets translated to odd harmonics of the carrier frequency. In the ideal chopping case the amplifier bandwidth is assumed to be infinity. Hence multiplying the signal twice with $v_{clk}(t)$ will reconstruct the input signal ideally. Since the noise and offset introduced by the amplifier go through the modulation process only once, they remain translated to

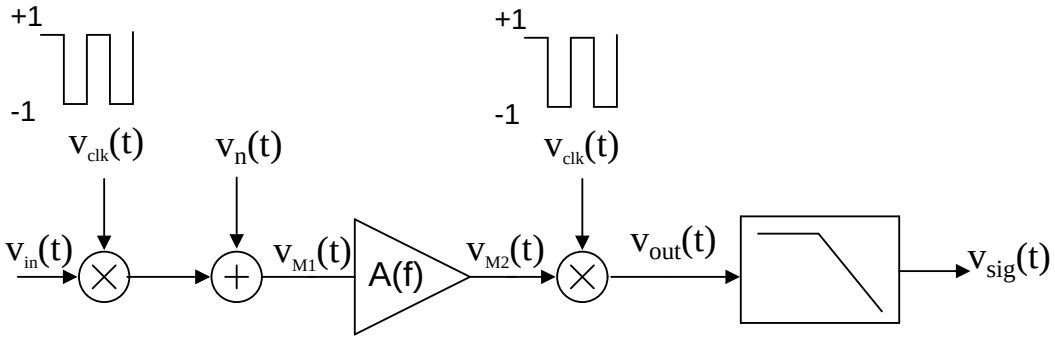
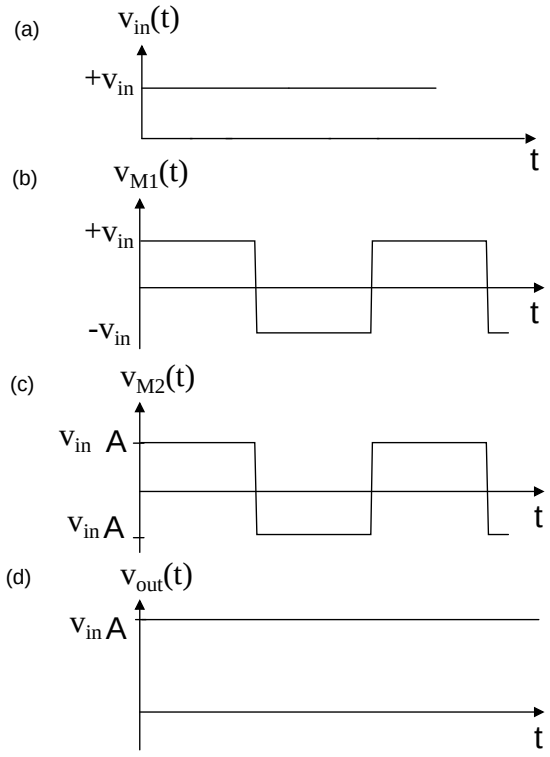
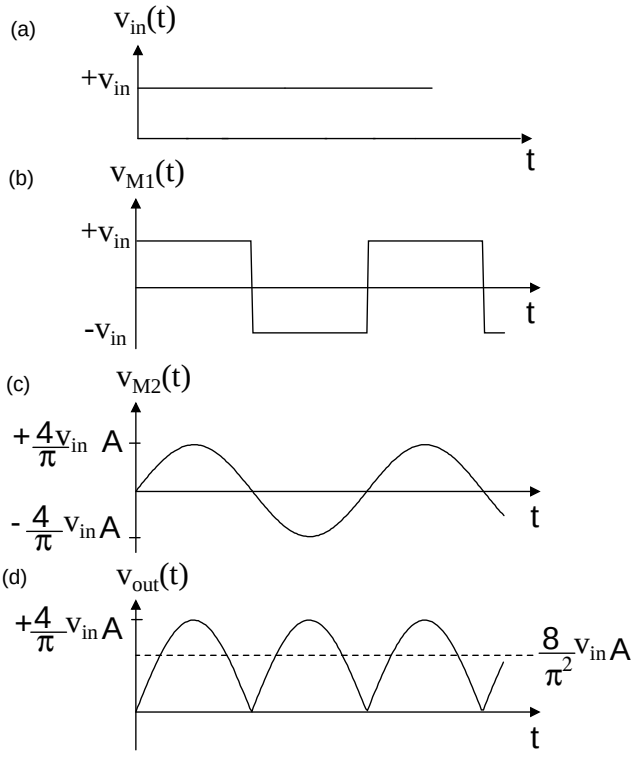


Figure 2.4: Chopper stabilization principle

the odd harmonics of the chopping frequency at the output. But when the amplifier bandwidth is limited, the input signal is demodulated back to the original baseband along with some spectral contributions at even harmonics of the chopper frequency. Low pass filtering this output removes the offset and the low frequency noise of the amplifier when we obtain a clean signal $v_{sig}(t)$. Fig. 2.5(b) shows the



(a) Amplifier has infinite bandwidth



(b) Amplifier is band limited

Figure 2.5: Waveforms appearing across the chopper amplifier for a DC input

waveforms that appears across a chopper amplifier for a DC input when the amplifier's bandwidth is limited to twice the chopping frequency. The output of the

amplifier is now a sine wave which after passing through the second modulator will become a rectified sine wave having even order harmonic components of the chopping frequency. This when compared with Fig. 2.5(a) has an effective gain of 0.8A whereas in the ideal case the gain is A.

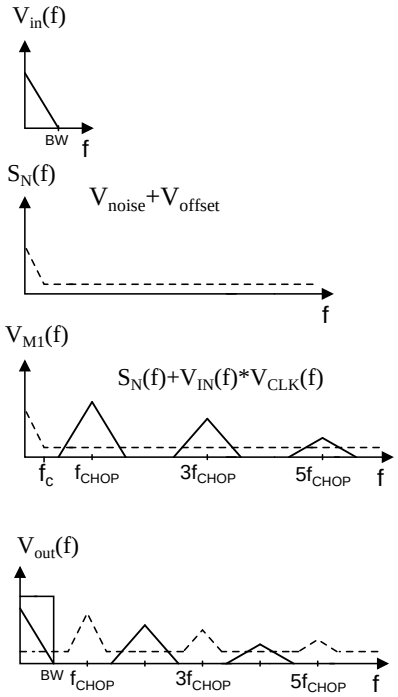


Figure 2.6: Chopper stabilization principle in frequency domain

Fig. 2.6 clarifies the process of noise reduction by demonstrating the chopping principle in frequency domain. The output power spectral density $V_{out}(f)$ is a replica of the noise power spectral density $S_N(f)$ at the odd multiples of the chopper frequency along with the input power spectral density $V_{in}(f)$ which is demodulated back to the baseband and also present at the even harmonics of f_{CHOP} since the amplifier is band limited. $S_N(f)$ will rapidly decrease in magnitude with the order of the harmonic. The noise power spectral density at low frequencies is now equal to the down-converted noise from frequencies around the harmonics of the clock frequency.

The chopping frequency is chosen to be higher than the 1/f corner frequency (f_c) of the amplifier so that the baseband noise after chopping is almost equal

to the wideband thermal noise of the amplifier. The chopping frequency must also be higher than the bandwidth of the input signal to avoid aliasing. Hence the relation, $f_{CHOP} > 2\ BW + f_C$. The low noise of the chopper stabilization technique is the main reason to use it condition weak thermocouple signals.

2.2.1 Chopping Architecture

As discussed before, chopper stabilization applies modulation to reduce the low frequency noise. The carrier signal can be any high frequency signal. The simplest form of a chopper modulator is shown in the Fig. 2.7. It is implemented with four MOSFET switches which will alternately open and close to chop the signal.

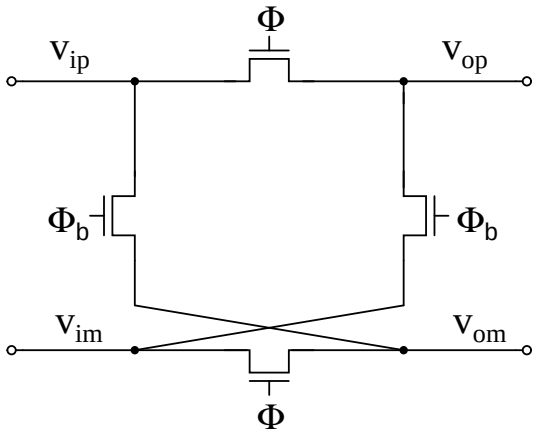
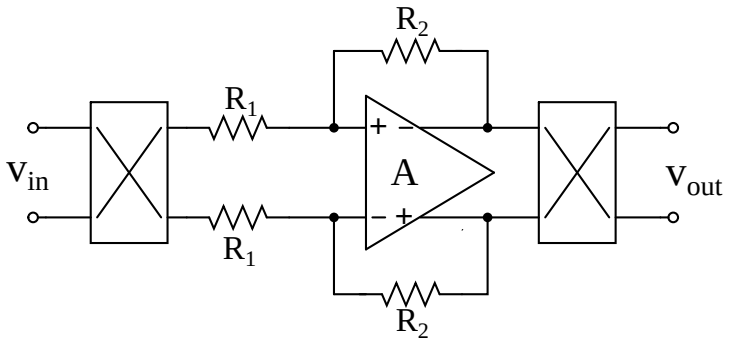


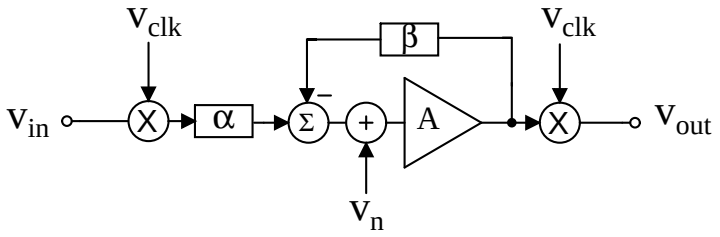
Figure 2.7: Chopper modulator

In the ideal chopping case, the bandwidth of the amplifier is assumed to be infinity. As long as this is true, multiplying the signal twice with $v_{clk}(t)$ will reconstruct the input signal. In conventional implementations, the signal is chopped at the input, amplified and demodulated at the output nodes as shown in Fig. 2.8. The equivalent block level model is shown in the Fig. 2.8(b) to analyse the effect of chopping on the signal and noise individually.

β is the feedback factor $\frac{R_1}{R_1 + R_2}$ and α is the attenuation factor $\frac{R_2}{R_1 + R_2}$. The signal transfer function and the noise transfer function are calculated using super-



(a) Schematic Representation



(b) Block Representation

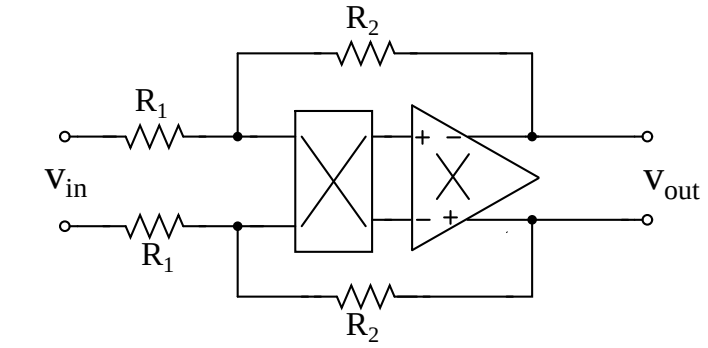
Figure 2.8: Chopper stabilized amplifier : Configuration 1

position principle. The relationship is as follows

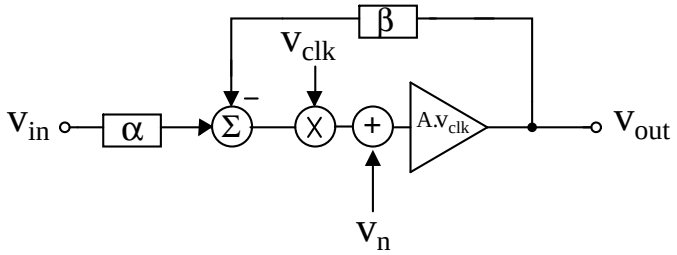
$$v_{out} = \alpha \frac{A}{1 + A\beta} v_{clk}^2 v_{in} + \frac{A}{1 + A\beta} v_{clk} v_n \tag{2.5}$$

From equation 2.5 it is evident that the noise signal is multiplied by the clock signal only once whereas the input signal is multiplied twice effectively separating the signal and noise in frequency domain which can be later filtered off.

The disadvantage with this configuration is that the output of the amplifier where the switches are placed will swing rail to rail. The resistance of the switches will vary with the signal strength leading to distortions at the output. The limited bandwidth of the amplifier also will lead to the presence of undesirable high frequency spectral components at the output due to switching. Hence high frequency chopping cannot be performed. Besides the switch's thermal noise is directly coupled to the output. Because we have switches in the middle of the supply, for low voltage applications a charge pump is needed to ensure smaller ON-resistance of the switches. To overcome these disadvantages, the signals can be chopped at the low impedance, smaller swing nodes. The choppers can be moved around the



(a) Schematic Representation



(b) Block Representation

Figure 2.9: Chopper stabilized amplifier : Configuration 2

amplifier block as long as the signal and noise transfer functions follow the chopping principle. One possible implementation is shown in Fig. 2.9. The relationship between the input and output in this configuration is represented below.

$$v_{out} = \alpha \frac{A}{1 + Av_{clk}^2 \beta} v_{clk}^2 v_{in} + \frac{A}{1 + Av_{clk}^2 \beta} v_{clk} v_n \tag{2.6}$$

Equation 2.6 is similar to equation 2.5, hence by placing the chopper within the amplifier the chopping operation is not being affected. Fig. 2.10 illustrates the placement of chopper inside an opamp. V_{imchop} and V_{ipchop} are input signals after chopping. The final outputs V_{om} and V_{op} are obtained by placing the chopper at the output nodes (V_{omchop}, V_{opchop}) of the telescopic cascode opamp as shown in Fig. 2.10(a). The same output can be obtained by absorbing the choppers within the opamp, at the cascode nodes between the transistors M1-M2 and M3-M4 and as well between M5-M6 and M7-M8 as shown in Fig. 2.10(b). By absorbing the chopper within the amplifier, the problem arising because of switching at the high swing nodes is reduced. Hence high frequency chopping can be performed. There

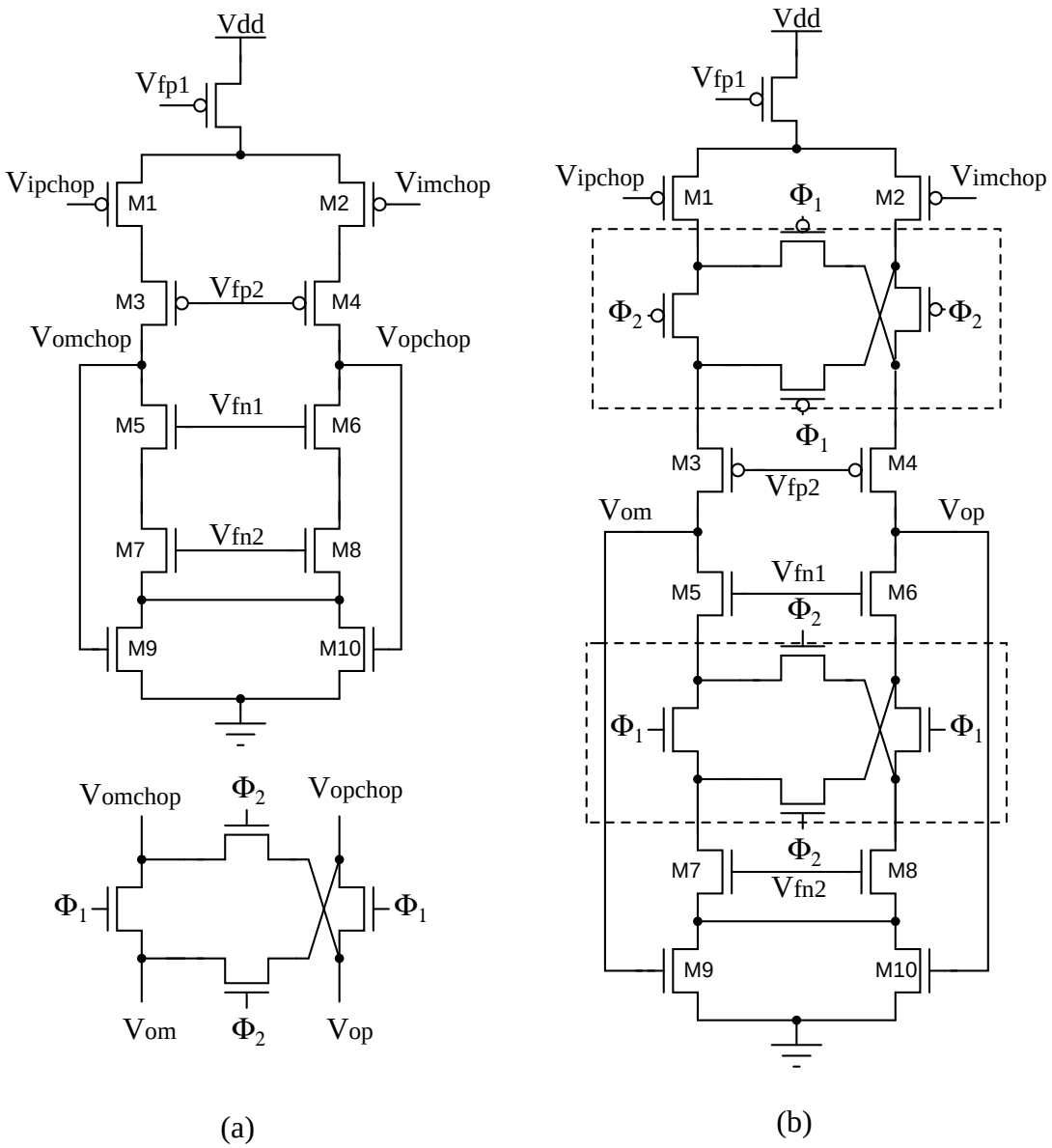


Figure 2.10: Schematic showing the placement of choppers within an opamp

will also be a reduction in the non-linearities caused due to the switches since they are placed at smaller swing nodes. The disadvantage in this technique is that the switches are placed in the bias current path. In the previous configuration one end of the switches will be connected to the input terminal of the opamp, hence no current will flow through them. If the resistance of the switches is considerable enough for the bias currents flowing through them, then the voltage drop across the switches will alter the DC operating point of the amplifier. In order to achieve small resistance values the transistor sizes can be chosen large enough but then the capacitance offered by them would cause glitches due to charge injection and

clock feedthrough which would degrade the linearity and stability of the amplifier. Despite these disadvantages, configuration 2 is a better choice owing to its superior linearity.

2.3 Simulation of Time Varying Circuits

By their very nature, choppers are time varying circuits. To obtain the frequency response of such a circuit would require the help of a transient analysis tool like SPICE. In addition some post processing will be required on the output data of the transient analysis to extract the gain and phase information. This method of analysis is time consuming and places a high demand on the computer resources. Cadence Design Systems has developed a tool, SpectreRF, a simulator that performs time and frequency domain analysis of such periodic time varying circuits [6]. For time invariant circuits, the frequency response can be calculated using the linearized circuit model around the DC operating point. Similarly for periodically switching circuits, the frequency response can be calculated by linearizing the circuit around the periodic operating point. After PSS analysis, a Periodic AC analysis (PAC) is run to compute the frequency response of the circuit. Noise behaviour of the circuit can be simulated with Periodic Noise analysis(Pnoise). The PSS analysis should be run with the clock alone driving the circuit. For illustration, the simulation result of an amplifier's noise with and without chopping is shown in the Fig. 2.11. The same amplifier is then autozeroed and the noise reduction that is achieved is also plotted in the Fig. 2.11. The higher noise floor due to the sampling process is evidently seen in the autozeroed noise curve.

2.3.1 Noise Analysis

To quantify the reduction in noise due to chopping, 1/f noise is generated in Matlab and it is chopped. White noise samples are taken and multiplied by an appropriate filter sequence, to get the desired 1/f spectrum [7]. It is then transformed to time domain with an IDFT operation. Now we have samples which are correlated with

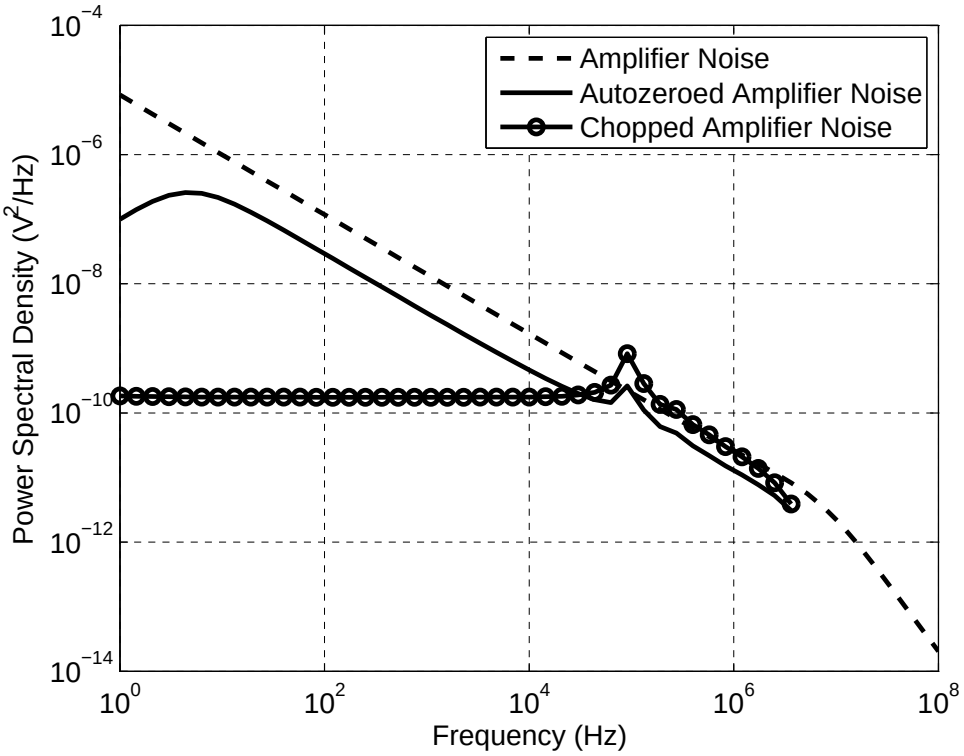


Figure 2.11: Comparison of noise in chopper stabilization and autozeroing

the desired autocorrelation properties of flicker (1/f) noise. The filter transfer function H(f) in this case is $\frac{1}{\sqrt{f}}$. Fig. 2.12 shows the generation of 1/f noise samples after which it is chopped with a carrier signal v_{clk}.

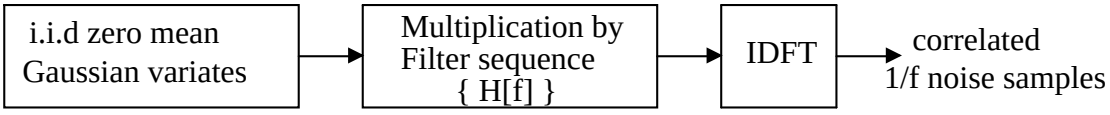


Figure 2.12: Generation of 1/f noise for chopping

This generalized model of a chopping system is simulated and the maximum reduction in noise achievable for a particular chopping frequency can be calculated. PSS analysis has the disadvantage that it is computationally expensive. To overcome this issue, noise analysis of a chopper amplifier can be done in Matlab. A Matlab model similar to Fig. 2.12 is developed. The only difference is that, instead of generating 1/f noise in Matlab, the noise of the amplifier obtained around its DC operating point from noise analysis is used. Simulation in SpectreRF is also

done to cross verify the results.

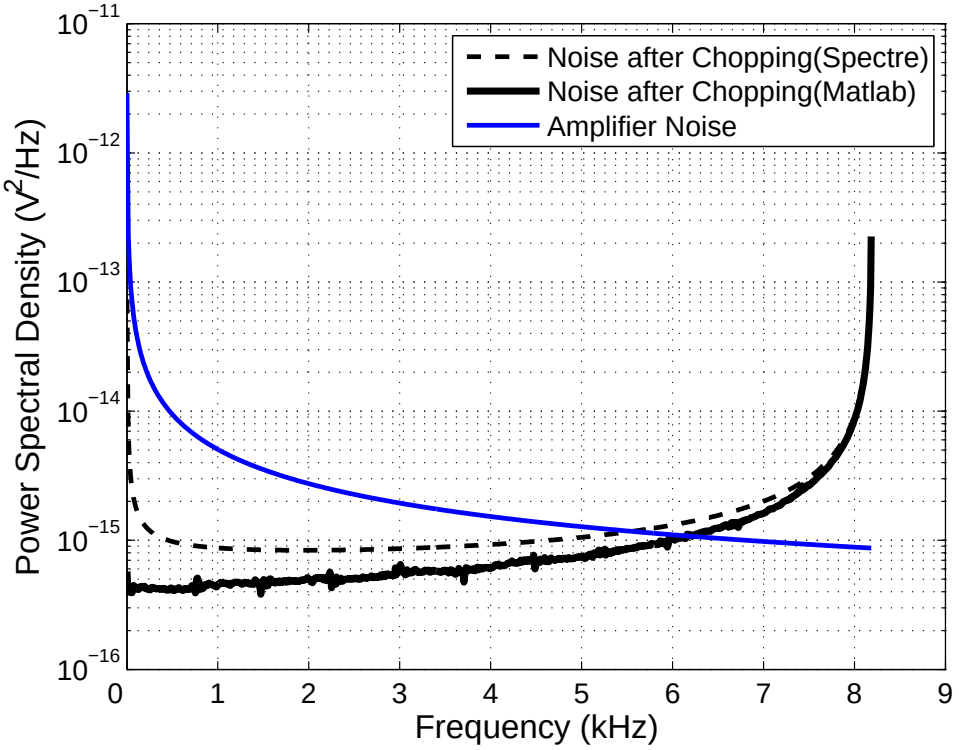


Figure 2.13: Comparison between SpectreRF and Matlab model for the calculation of noise

The noise plot of the amplifier is obtained through conventional noise analysis. Once the noise of the amplifier is determined, multiple iterations of chopping are performed in Matlab to find out the optimum frequency of chopping. For illustration purpose an amplifier as shown in Fig. 2.9(a) is designed. The amplifier has a gain of 40 dB and bandwidth of 40 kHz. Through Matlab simulations chopping frequency is chosen to be 8.192 kHz. With this clock frequency Pnoise analysis is performed and the noise after chopping is determined from SpectreRF. Noise obtained from both the analysis tools are plotted and shown in Fig. 2.13. As can be seen from the Table 2.1 noise voltage obtained from spectre analysis differs from what is obtained in Matlab, this is because Matlab uses an ideal chopping model and also it does not consider switch noise.

Table 2.1: Integrated amplifier noise (1 Hz - 1.024 kHz)

Amplifier Noise	183.4 μV
Amplifier Noise after Chopping(SpectreRF)	27.58 μV
Amplifier Noise after Chopping(Matlab)	14 μV

The simulation time required to run a Pnoise analysis is longer compared to the time required to estimate the chopped amplifier noise in Matlab. For instance, the spectre simulation in the above example took about a day whereas it took less than a minute in Matlab. Though the results do not match accurately, an approximate estimate is possible using Matlab thus saving considerable simulation time.

CHAPTER 3

Design of the Three-Stage amplifier

A key component of a signal conditioning circuit is a high gain amplifier. An amplifier is used to provide voltage gain and as well to buffer the signal coming from the thermocouple before it is further processed. There are several key parameters that are to be considered when designing an amplifier for a thermocouple application.

Input offset voltage This voltage offset is dependent upon the amplifier's topology and is inversely proportional to the square root of the area of the input transistors. As mentioned in chapter 1, The sensitivity of a standard K type thermocouple is $40\,\mu\mathrm{V}/^{o}\mathrm{C}$ hence the offset and the noise of the block measuring this signal must be smaller than this. For such demanding applications special offset reduction schemes must be employed to achieve offset voltages in the range of few microvolts.

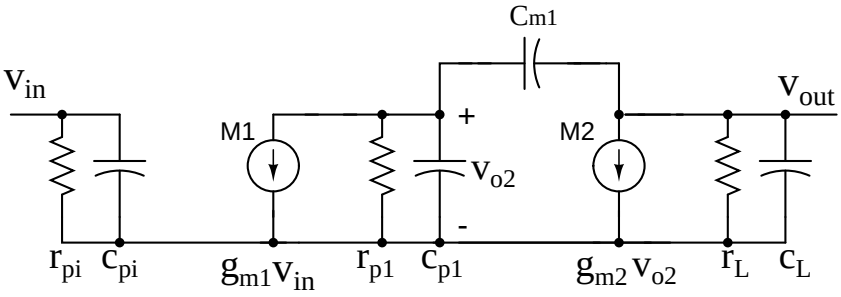
Voltage offset drift The input offset voltage will change with temperature. This error source can be minimized by selecting a low-drift amplifier, such as an amplifier with an autozero based topology or by implementing periodic system corrections to cancel out the offset and drift.

Open loop gain Due to the small input signal generated by the thermocouple, the amplification required is approximately 100 to 500 times. To avoid gain error, high open loop gain is necessary. Temperature drift of open loop gain also will have a deleterious effect on output accuracy. For instance, for a K type thermocouple amplifier with $100\,\mathrm{mV}/^{o}\mathrm{C}$ output sensitivity, needs a closed loop gain of ≈ 2500. An ordinary opamp with a minimum open loop gain of 50,000 would have an initial gain error of $(2500)/(50{,}000) = 5\,\%$. For a gain accuracy less than $1\,\%$ minimum open loop gain must be 250,000.

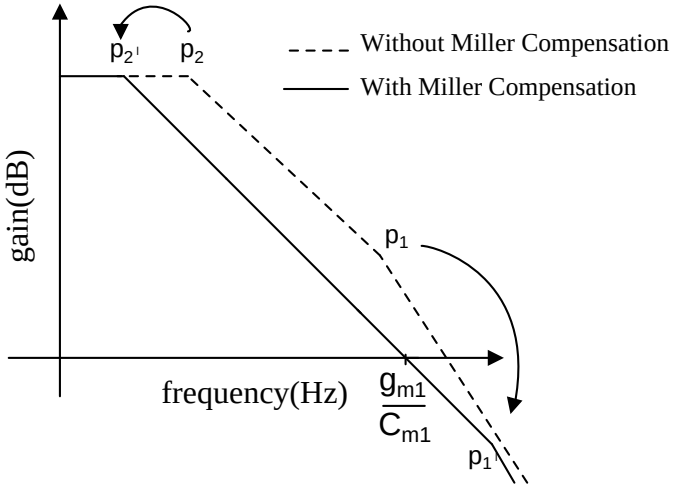
3.1 Nested Miller Compensated Amplifier

For a closed loop gain accuracy of 0.05 % and an output sensitivity of 4 mV/^{o}C the open loop gain of the opamp required is at least 106 dB. A two-stage amplifier cannot provide such a high gain. So a three-stage architecture is chosen. It is required to appropriately compensate it for stability. The Miller compensation technique can be used to compensate amplifiers with more than two stages. To understand the application of Miller compensation to more stages the Bode plot can be inspected.

Fig. 3.1(a) shows the small signal equivalent of a two-stage amplifier with Miller compensation. The Miller compensated amplifier consists of one dominant pole p_2' and a second pole at a much higher frequency p_1' as shown in Fig. 3.1(b).



(a) Small signal equivalent of the two-stage amplifier



(b) Bode plot of two stage Miller compensated amplifier

Figure 3.1

Hence a circuit with three gain stages is also eligible for Miller compensation by

choosing proper values for the compensation capacitors. In Fig. 3.2 the small signal

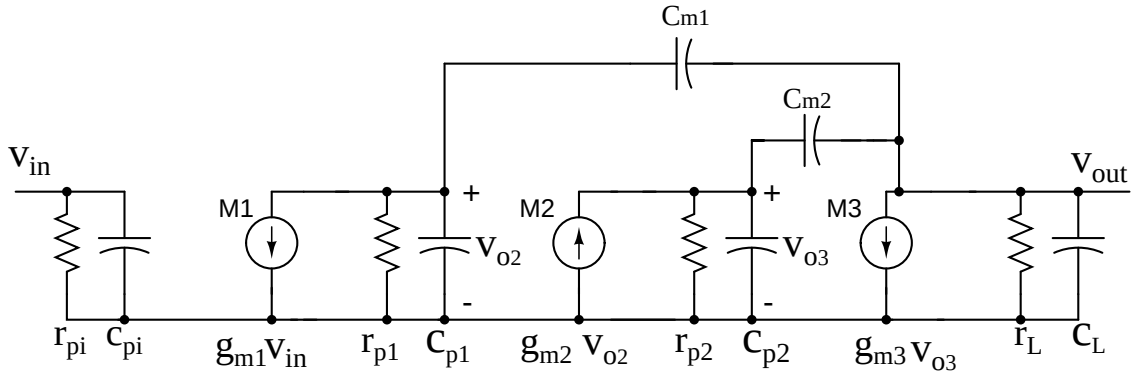


Figure 3.2: Small signal equivalent of the three-stage amplifier

equivalent of a three-stage amplifier with Nested Miller Compensation (NMC) technique is shown. Bode plots of Fig. 3.3 shows the movement of poles after inserting the compensation capacitors C_{m1} and C_{m2}. The dotted line in Fig. 3.2 shows the frequency response of the uncompensated amplifier with three dominant poles. The load impedance consisting of $C_L$and r_L accounts for the output pole p_1. C_{p2}/r_{p2}, the pole p_2 and C_{p1}/r_{p1}, the pole p_3. Inserting the Miller capacitor C_{m2} leads to the solid curve in Fig. 3.3a. This Miller capacitor splits the poles p_1 and p_2 to their new positions p_1' and p_2' respectively. Miller capacitor C_{m1} which closes the second loop, acts on the newly placed pole at p_2' and the additional pole p_3 introduced by M1. Splitting these two poles results in a single dominant pole at p_2'' as shown by the solid curve in Fig. 3.3b.

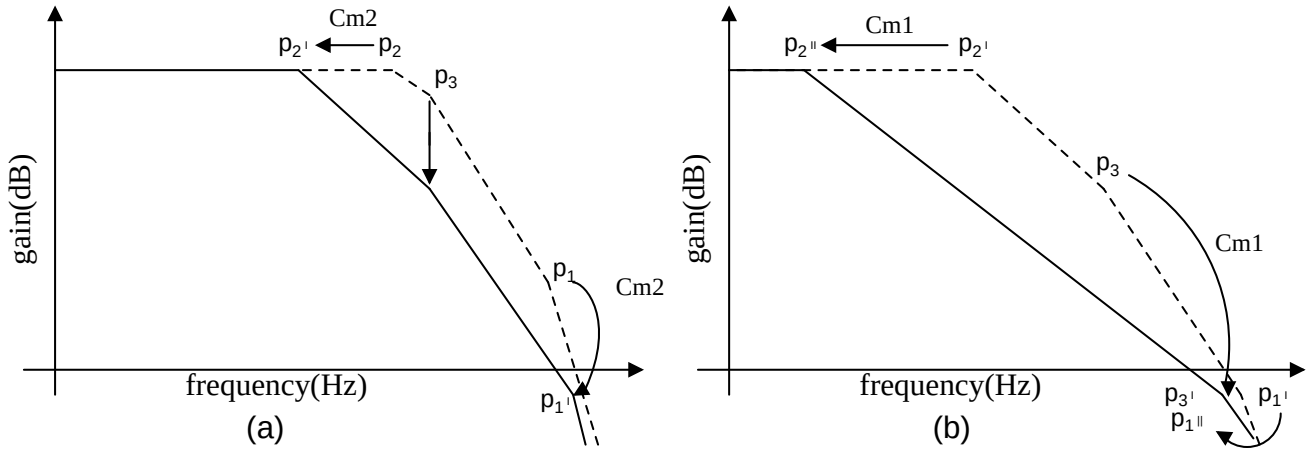


Figure 3.3: Bode plot showing the movement of poles for Nested Miller compensation

3.1.1 Determining the values of the Miller capacitors

The amplifier in unity gain feedback is considered since this is when the fedback signal is maximum from the output to the input and hence the worst case for stability. In this configuration there are three feedback loops. The Miller capacitor C_{m2} and the transistor M3 is the lowest level of the feedback loop. The loop consisting of the Miller capacitor C_{m1} and the transistors M2 and M3 is the next higher level. The overall unity gain feedback is the outermost feedback loop of all. C_{m2} together with transconductance of M2 and M3 constitute a standard Miller compensated two stage amplifier whose transfer function can be written as,

$$\frac{V_{out}}{V_{o2}} = \frac{g_{m2}}{C_{m2}} \frac{1}{s\left(1 + \frac{s}{p_1'}\right)} \tag{3.1}$$

In equation 3.1 V_{o2} is the voltage at the gate of the transistor M2 and V_{out} is the voltage seen at the drain of transistor M3. K_1 is the gain constant which equals the unity gain frequency of the two stage amplifier comprising of transistors M2, M3 and the capacitor C_{m1} : $\frac{g_{m2}}{C_{m2}}$. The transfer function shown in equation 3.1 represents an integrator with its dominant pole p_2' at origin and a secondary pole p_1' at $\frac{g_{m3}}{C_L}$ in the left half s-plane. The pole at the origin is obtained by neglecting the resistances which is an approximation such that it simplifies further calculations. This should not affect the results since during pole splitting the dominant pole moves to a very low frequency, far away from the high frequency poles we are interested in.

To quantify the effect of the addition of the second Miller capacitor C_{m1}, the two stage amplifier with M2 and M3 can be considered to be a single portion with gain A and C_{m1} is the feedback element. At very high frequencies C_{m1} is a short since its value is generally much larger than the interstage capacitance C_{p1}. To calculate the poles, the roots of the characteristic polynomial $\Delta = 1 + A\beta$ are

calculated.

$$A = \frac{K_1}{s\left(1+\frac{s}{p_1'}\right)} \tag{3.2}$$

$$\beta = 1 \tag{3.3}$$

$$\Delta(s) = \frac{1}{K_1 p_1'}s^2 + \frac{1}{K_1}s + 1 \tag{3.4}$$

The roots of this polynomial are p_1'' and p_3' which are the high frequency poles seen in the Fig. 3.3(b). Adding the input stage transistor M1 results in an integrator when seen together with transistors M2, M3 and the capacitors C_{m1} and C_{m2}. The unity gain frequency of this configuration with transistor M1 and C_{m1} is $K_2 = \frac{g_{m1}}{C_{m1}}$. Therefore the total open loop transfer function is,

$$\frac{V_{out}}{V_{in}} = \frac{K_1 K_2}{s\left(\frac{1}{p_1'}s^2 + s + K_1\right)} \tag{3.5}$$

The closed loop transfer function in unity gain feedback is

$$\frac{V_{out}}{V_{in}} = \frac{A}{1+A\beta} = \frac{K_1 K_2 p_1'}{s^3 + p_1' s^2 + K_1 p_1' s + K_1 K_2 p_1'} \tag{3.6}$$

Since we need a maximally flat closed loop response, this equation can be equated to a standard third order butterworth polynomial $\left(\frac{s}{\omega_0}\right)^3 + 2\left(\frac{s}{\omega_0}\right)^2 + 2\left(\frac{s}{\omega_0}\right) + 1$. Comparing the respective coefficients we get

$$K_1 = \frac{g_{m2}}{C_{m2}} = \frac{p_1'}{2} \tag{3.7}$$

$$K_2 = \frac{g_{m1}}{C_{m1}} = \frac{p_1'}{4} \tag{3.8}$$

The above equations describe the design procedure to build a Nested Miller compensated amplifier [8]. The detailed transfer function is shown in equation 3.9 [9].

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}g_{m2}g_{m3}r_{p1}r_{p2}r_L\left(1 - s\frac{C_{m2}}{g_{m3}} - s^2\frac{C_{m1}C_{m2}}{g_{m2}g_{m3}}\right)}{(1+sC_{m2}g_{m2}g_{m3}r_{p1}r_{p2}r_L)\left[1 + s\frac{C_{m2}(g_{m3}-g_{m2})}{g_{m2}g_{m3}} + s^2\frac{C_L C_{m2}}{g_{m2}g_{m3}}\right]} \tag{3.9}$$

Since the s^2 term is negative in the numerator, there is one right-half-plane (RHP) zero and one left-half-plane (LHP) zero. The LHP zero increases the phase margin while the RHP zero does the reverse, so just eliminating the RHP zero is sufficient. To do so a nulling resistor R_m is included as shown in Fig. 3.4. The final design equations are summarized below [9] [10].

$$g_{m3} \gg g_{m2},\, g_{m1} \tag{3.10}$$

$$C_{m1} = 4\,\frac{g_{m1}}{g_{m3}}\,C_L \tag{3.11}$$

$$C_{m2} = 2\,\frac{g_{m2}}{g_{m3}}\,C_L \tag{3.12}$$

$$R_m = \frac{1}{g_{m3}} \tag{3.13}$$

3.2 Design details

Using the technique explained above, a differential three-stage opamp is designed. The common mode of each stage is separately controlled. The differential signal path is compensated using the Nested Miller compensation (NMC) technique discussed above. The overall structure of the three-stage opamp is shown in the Fig. 3.4. g_{m2} and g_{m3} together constitute a system with single dominant pole, hence

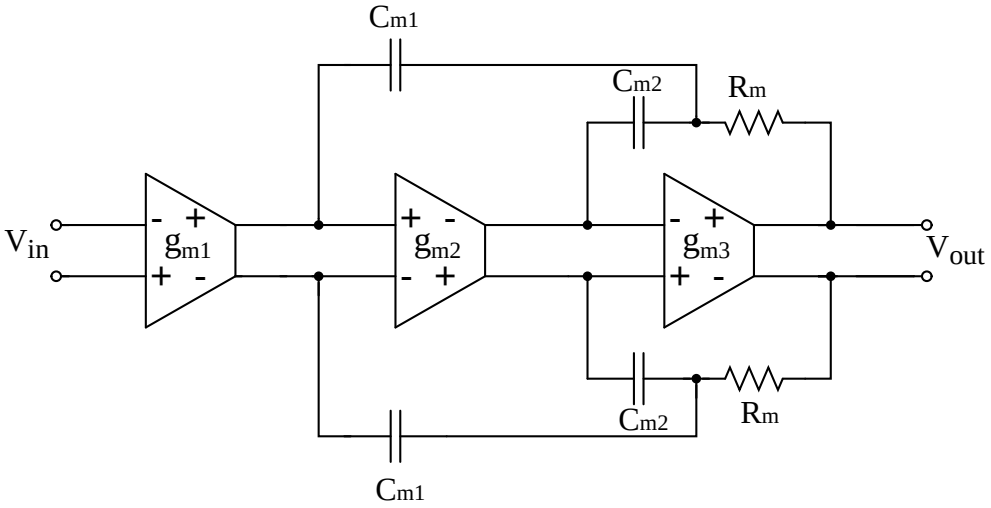


Figure 3.4: Three-stage NMC fully differential opamp

the common mode sensing opamp (g_{m4}) which stabilizes the output common mode

voltage, is compensated using the two-stage Miller compensation technique. The common mode feedback compensation is shown in the Fig. 3.5. R_m is chosen such that the right half plane zero can be shifted to the left half plane [9]. Maximum

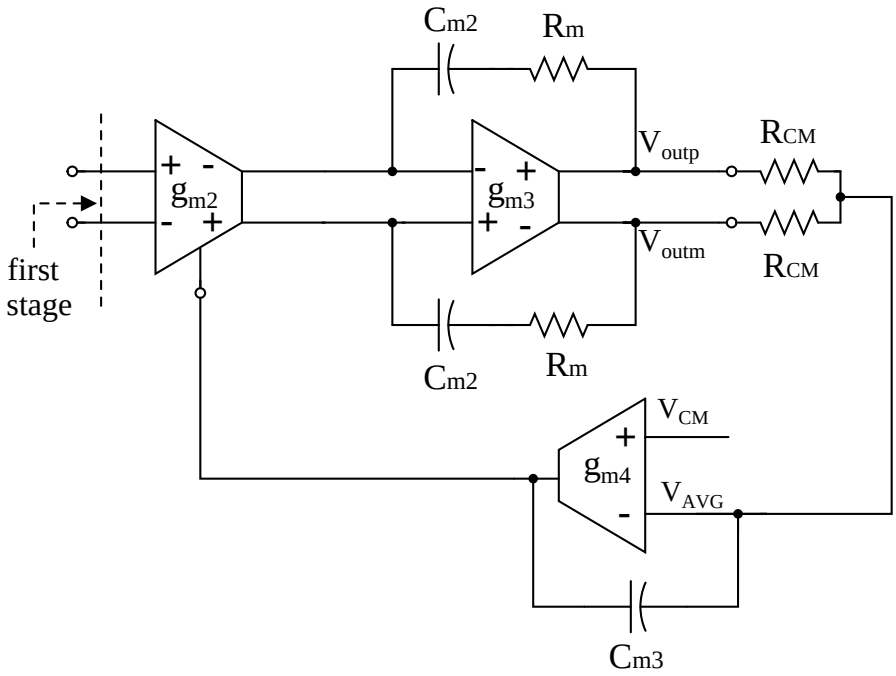


Figure 3.5: Common mode feedback scheme

gain is sought from the first stage of the opamp. Hence a telescopic cascode stage is chosen. Cascoding helps in increasing the gain as well decoupling the input transistor's capacitance C_{GD} to the output. A folded cascode structure is the optimum second stage opamp architecture that can be implemented. This is because we intend to have a class AB output stage to reduce the quiescent power consumption. The output impedance arm of the folded cascode opamp can bear the translinear circuit needed to bias the final output class AB stage. As discussed in section 2.2.1 choppers are placed within the amplifier as shown in Fig. 3.6. In the first telescopic cascode stage, choppers are placed at the cascode nodes between the transistors M1-M2 and M3-M4 and as well between M5-M6 and M7-M8. PMOS switches are used in the chopper modulator present at the input PMOS section while NMOS switches are placed near the load NMOS transistors. Choppers are placed only in the first stage of the three-stage opamp since the offset and noise contributed by the second and third stages would be insignificant when compared

to the first stage. The NMC amplifier is built with the following transconductance and capacitance values.

$$g_{m1} = 320\,\mu S \tag{3.14}$$

$$g_{m2} = 236\,\mu S \tag{3.15}$$

$$g_{m3} = 1.6\,mS \tag{3.16}$$

$$\Rightarrow C_{m1} = 6\,pF \tag{3.17}$$

$$\Rightarrow C_{m2} = 3\,pF \tag{3.18}$$

$$\Rightarrow R_m = 700\,\Omega \tag{3.19}$$

The circuit details of the opamp used for common mode stability is shown in the Fig. 3.7. The output of this circuit V_{cmfb} is used to tweak a NMOS current source present in the second stage of the three-stage opamp.

3.3 Simulation Results

3.3.1 Frequency Response

The frequency response of the three stage opamp is shown in the Fig. 3.8. The frequency response is measured with a load capacitor of 10 pF. The opamp has a DC gain of 114 dB.

3.3.2 Noise

The opamp is placed in voltage-series feedback to attain a closed loop gain of 40 dB. This structure is similar to the one shown in Fig. 2.8. Clock frequency within the 3 dB bandwidth of the amplifier is chosen so that the signal is not attenuated. Noise analysis with and without chopping is performed and the results are plotted in the Fig. 3.9. Chopping is done at a clock frequency of 10 kHz. The noise of the amplifier before and after chopping is tabulated in Table 3.1. Noise reduction achieved in configuration 2 is compared against configuration 1. Noise analysis

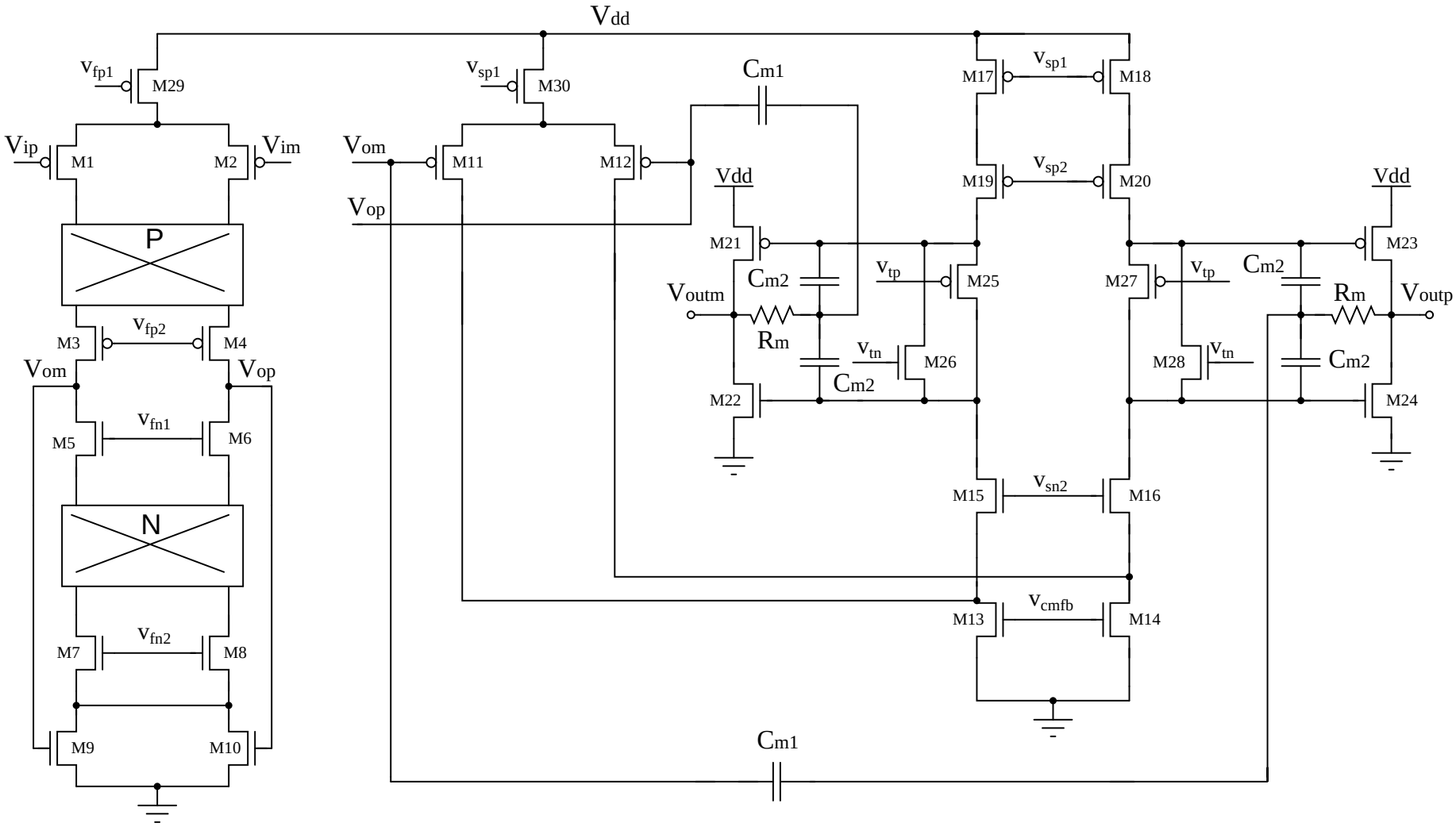


Figure 3.6: Three-stage NMC opamp circuit

FIRST STAGE	SECOND STAGE	THIRD STAGE
M29 : 40 (2 µm/.5 µm)	M30 : 160 (1 µm/.5 µm)	M25,M27 : 10 (.45 µm/.18 µm)
M1,M2 : 96 (2 µm/2 µm)	M11,M12 : 20 (1 µm/1 µm)	M26,M28 : 10 (.45 µm/.18 µm)
M3,M4 : 80 (1 µm/1 µm)	M17,M18 : 40 (1 µm/.5 µm)	M21,M23 : 36 (.48 µm/.36 µm)
M5,M6 : 40 (1.2 µm/1 µm)	M19,M20 : 40 (1 µm/.5 µm)	M22,M24 : 16 (.48 µm/.36 µm)
M7,M8 : 80 (1.2 µm/1 µm)	M15,M16 : 20 (.24 µm/.18 µm)	
M9,M10 : 32 (2 µm/4 µm)	M13,M14 : 36 (.48 µm/.48 µm)	

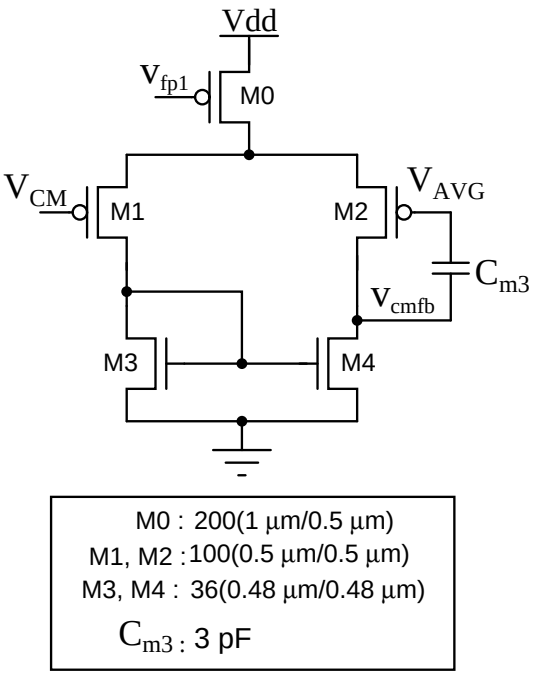


Figure 3.7: Circuit details of the CMFB opamp

Table 3.1: Integrated input referred noise of the amplifier(1 Hz - 1 kHz)

Without Chopper Stabilization	8.16 μV
With Chopper Stabilization: 1	758 nV
With Chopper Stabilization: 2	763 nV

with non-ideal choppers i.e, made of transistor switches, placed as shown in Fig. 2.9 is also done. Since the second and the third stage opamp's noise are also chopped in configuration 1, the integrated noise voltage is lesser than that is obtained from configuration 2.

3.3.3 Offset

Mismatch of any three-stage opamp will be dominated by its first stage. Fig. 3.6 shows the transistor sizes used in the first stage amplifier. Mismatch in MOS transistors is modelled as a function of device channel length L (μm) and device channel width W (μm). The difference in threshold voltage (V_{th}) is described by its standard deviation.

$$\sigma_{V_{th}} = \frac{A_{V_t}}{\sqrt{WL}} \tag{3.20}$$

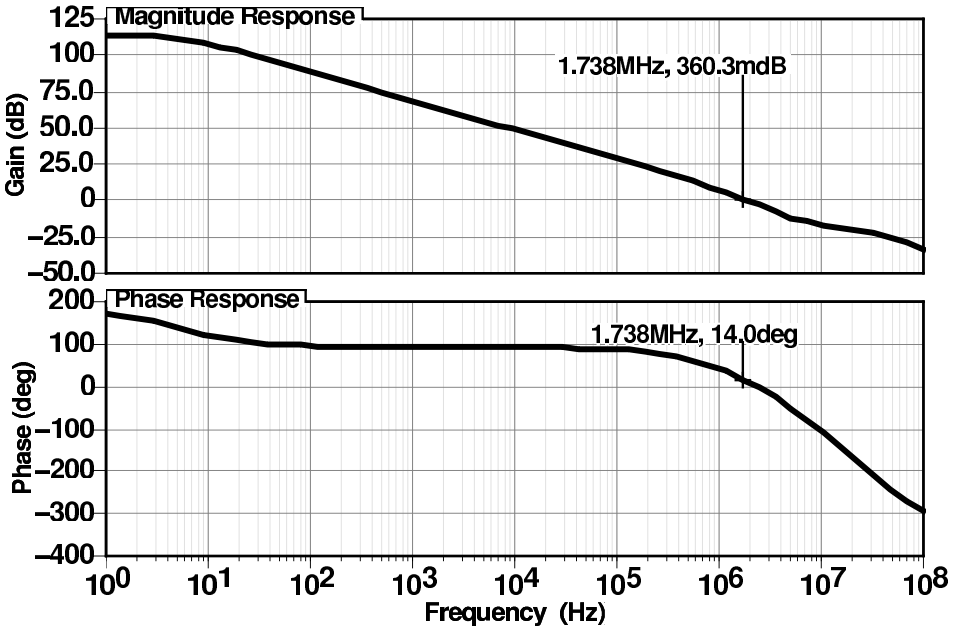


Figure 3.8: Frequency Response of the three-stage NMC opamp

where A_{V_t} is the mismatch coefficient. For $0.18\,\mu$m process its value is $3.5\,\text{mV}\,\mu$m. The input referred voltage mismatch is theoretically calculated as follows,

$$\begin{aligned}\sigma^2_{V_{OS}} &= \sigma^2_{V_{t12}} + \sigma^2_{V_{t78}}\left(\frac{g_{m78}}{g_{m12}}\right)^2 + \sigma^2_{V_{t34}}\left(\frac{\frac{g_{m34}}{1+\frac{g_{m34}}{gds_{12}+gds_{34}}}\frac{1}{g_{m12}}}\right)^2 \\ &\quad + \sigma^2_{V_{t56}}\left(\frac{\frac{g_{m56}}{1+\frac{g_{m56}}{gds_{56}+gds_{78}}}\frac{1}{g_{m12}}}\right)^2 \end{aligned} \tag{3.21}$$

The current mismatch due to β factor is also calculated in a similar manner. A_β is $1\,\%\,\mu$m.

$$\begin{aligned}\sigma^2_{\frac{\triangle I}{I}} &= \sigma_{\frac{\triangle\beta_{12}}{\beta_{12}}}{}^2 + \sigma_{\frac{\triangle\beta_{78}}{\beta_{78}}}{}^2 + \frac{\sigma_{\frac{\triangle\beta_{34}}{\beta_{34}}}{}^2}{g^2_{m34}}\left(\frac{g_{m34}}{1+\frac{g_{m34}}{gds_{12}+gds_{34}}}\right)^2 \\ &\quad + \frac{\sigma_{\frac{\triangle\beta_{56}}{\beta_{56}}}{}^2}{g^2_{m56}}\left(\frac{g_{m56}}{1+\frac{g_{m56}}{gds_{78}+gds_{56}}}\right)^2 \end{aligned} \tag{3.22}$$

The equivalent offset voltage due to β mismatch is negligible when compared to the offset voltage contributed by threshold voltage mismatch. Input referred mismatch $3\sigma_{V_{OS}} \approx 2.25\,\text{mV}$. This is the offset voltage that can be expected from this opamp without any offset cancellation scheme.

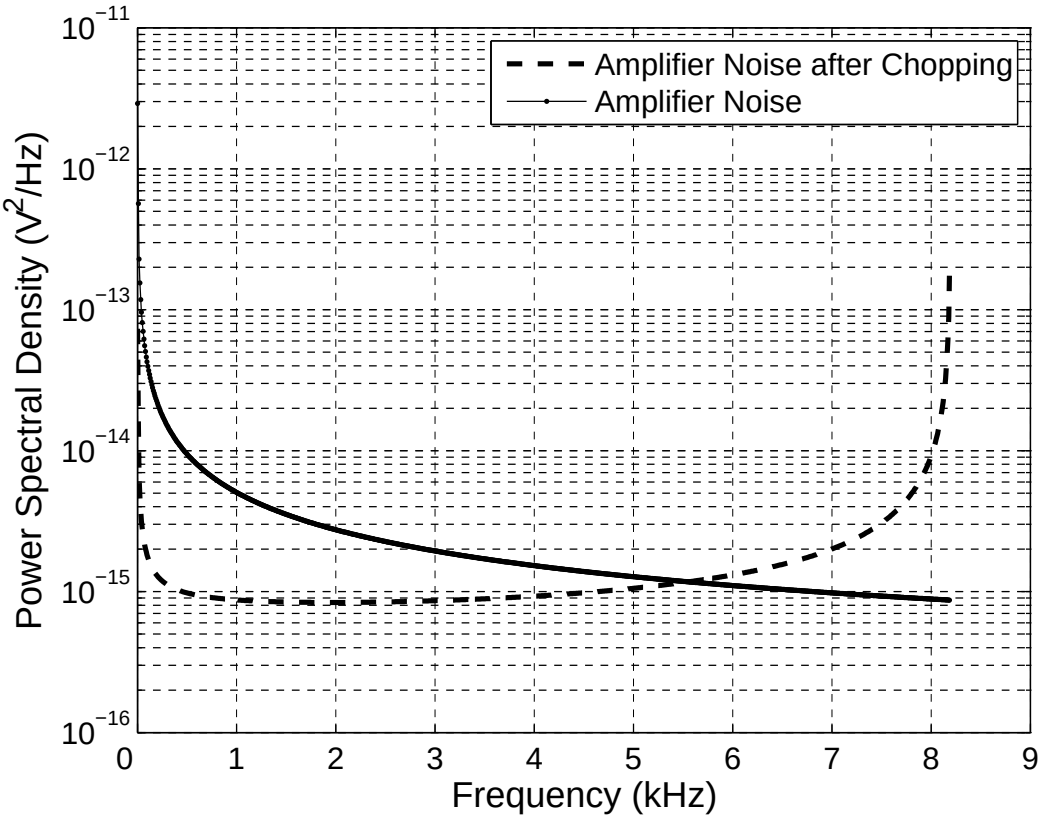


Figure 3.9: Comparison of noise spectral density

3.3.3.1 Resistor Mismatch

Irregularities in layout will also lead to offsets. Care is taken to maintain the differential symmetry of the circuit during layout. For matching purposes, feedback resistor R_2 is kept as a multiple of R_1, the input resistor. Hence multiple copies of R_1 are laid out in series to achieve R_2. $R_2 = \sum_1^{100} R_1$. For ease of calculation it is assumed that the deviation in the resistor value for each copy of R_1 is the same and is equal to the mean of deviation of all the copies in the resistor array, i.e in here $R_2 + \triangle R_2 = \sum_{i=1}^{100}(R_1 + \triangle R_i)$. The resistor mismatch is described by,

$$\sigma_{\frac{\triangle R}{R}} = \frac{A_R}{\sqrt{WL}} \tag{3.23}$$

where A_R is obtained from the process documents. With an increase in area of the resistor, the mismatch percentage reduces. Hence to achieve minimal gain error the resistor width is chosen to be $10\,\mu$m. A_R for high resistive poly resistors is

0.0708 $\%\,\mu$m. Unit resistor's value is $1\,\mathrm{k}\Omega$ and resistor length is $10\,\mu$m.

$$\mathrm{A} = \frac{\mathrm{R_2}}{\mathrm{R_1}} = 100 \tag{3.24}$$

$$\mathrm{R_2} = \sum_{1}^{100} \mathrm{R_1} \tag{3.25}$$

$$\text{Due to mismatch, } \mathrm{R_2} = \sum_{\mathrm{i}=1}^{100} (\mathrm{R_1} + \triangle \mathrm{R_i}) \tag{3.26}$$

$$\mathrm{A} + \triangle \mathrm{A} = \frac{\sum_{\mathrm{i}=1}^{100} (\mathrm{R_1} + \triangle \mathrm{R_i})}{\mathrm{R_1}} \tag{3.27}$$

$$\triangle \mathrm{A} = \sum_{1}^{100} \frac{\triangle \mathrm{R_1}}{\mathrm{R_1}} \tag{3.28}$$

$$\frac{\triangle \mathrm{A}}{\mathrm{A}} = \frac{1}{\mathrm{A}} \sum_{1}^{100} \frac{\triangle \mathrm{R_1}}{\mathrm{R_1}} \tag{3.29}$$

$$\sigma^2_{\frac{\triangle \mathrm{A}}{\mathrm{A}}} = \frac{1}{\mathrm{A}^2} \sum_{1}^{100} \sigma^2_{\frac{\triangle \mathrm{R_1}}{\mathrm{R_1}}} = \frac{100}{\mathrm{A}^2} \sigma^2_{\frac{\triangle \mathrm{R_1}}{\mathrm{R_1}}} \tag{3.30}$$

$$\sigma_{\frac{\triangle \mathrm{A}}{\mathrm{A}}} = \frac{10}{\mathrm{A}} \sigma_{\frac{\triangle \mathrm{R_1}}{\mathrm{R_1}}} \tag{3.31}$$

$$\sigma_{\frac{\triangle \mathrm{A}}{\mathrm{A}}} = \frac{1}{10} (0.00708\,\%) \tag{3.32}$$

$$\sigma_{\frac{\triangle \mathrm{A}}{\mathrm{A}}} = 0.000708\,\% \tag{3.33}$$

The layout of the chopper amplifier is shown in Fig. 3.10.

3.3.4 Performance Summary

The simulation results have been tabulated in Table 3.2.

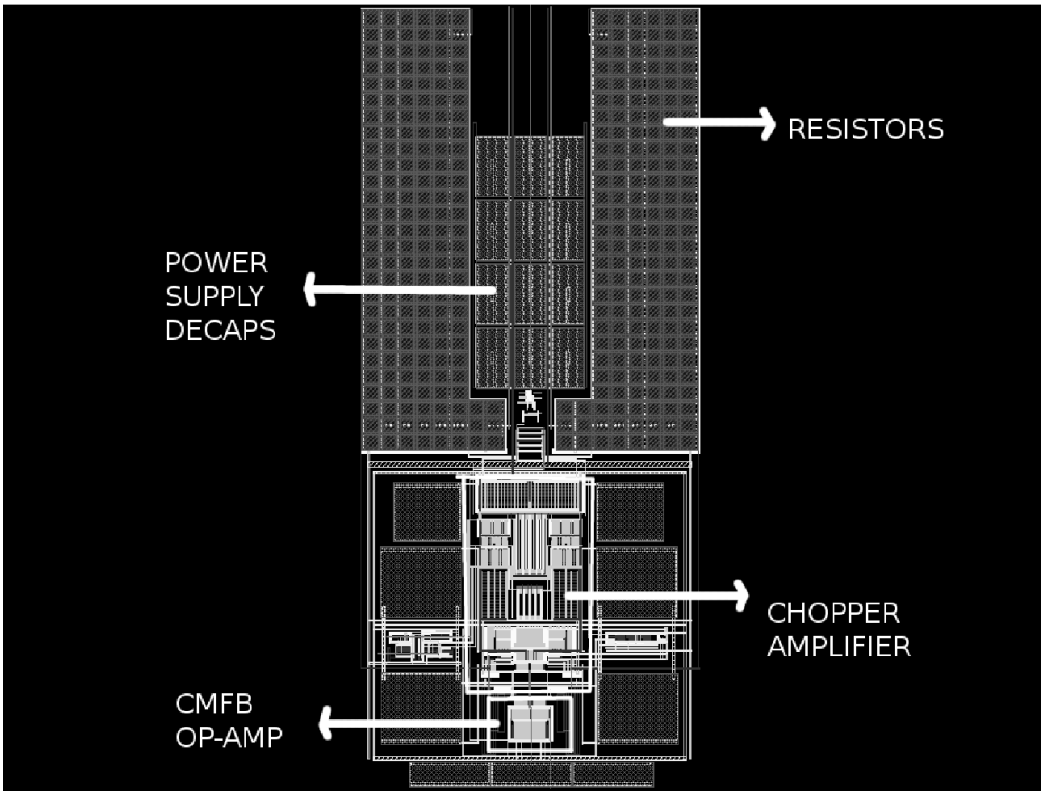


Figure 3.10: Chopper amplifier layout

Table 3.2: Opamp parameters

Parameter	**Value**
Technology	UMC 0.18 μm CMOS
Supply Voltage	1.8 V
Supply Current	360 μA
Input Referred Noise(1 Hz - 1 kHz)	763 nV
β	1/101
Unity Gain Frequency	1.75 MHz
DC Loop Gain($\mid A\beta \mid$)	85 dB
Phase Margin(180- $\measuredangle A\beta$)	81 °
CMRR @ 50 Hz	160 dB
PSRR @ 50 Hz	82 dB
Area	0.215 mm^2

CHAPTER 4

Measurement Results

This chapter deals with the measurement results of the fabricated design along with the details of the test board. The chopper amplifier was fabricated in 0.18 μm CMOS process from UMC through the multi project wafer (MPW) program of Europractice. The die was housed in a 84 pin JLCC package. The pin details of the chip are given in Appendix C. The setup to test the amplifier is shown in the Fig. 4.1.

4.1 Design of Test board

A two layer printed circuit board was designed to characterise the chopper amplifier. The dimensions of the PCB are 3.2" x 4". A photograph of the populated board is shown in the Fig. 4.2.

4.2 Measurement of Gain

The closed loop DC gain of the amplifier is measured by providing a sine wave input of 1 $\mathrm{mV_{pp}}$. The output of the amplifier is seen in an oscilloscope. This is

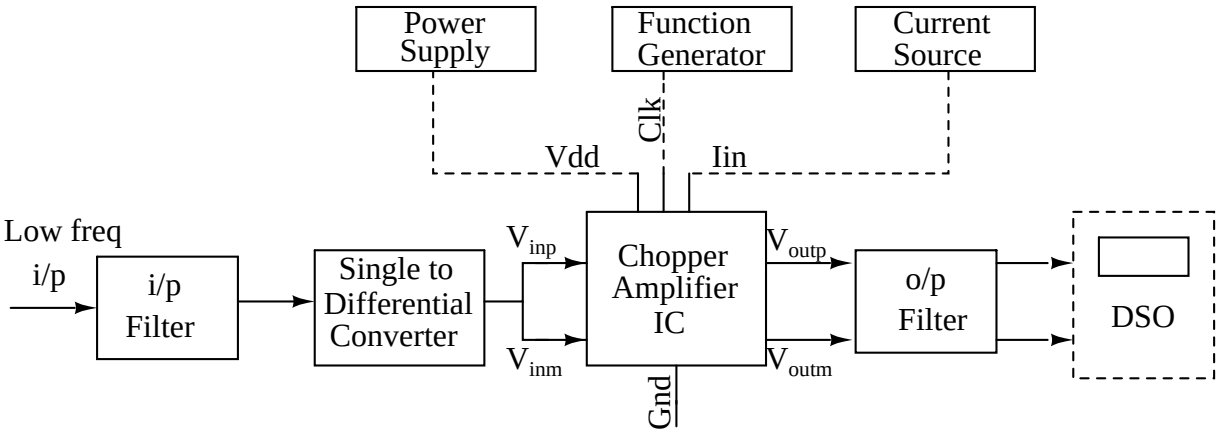


Figure 4.1: Block level representation of the test set-up

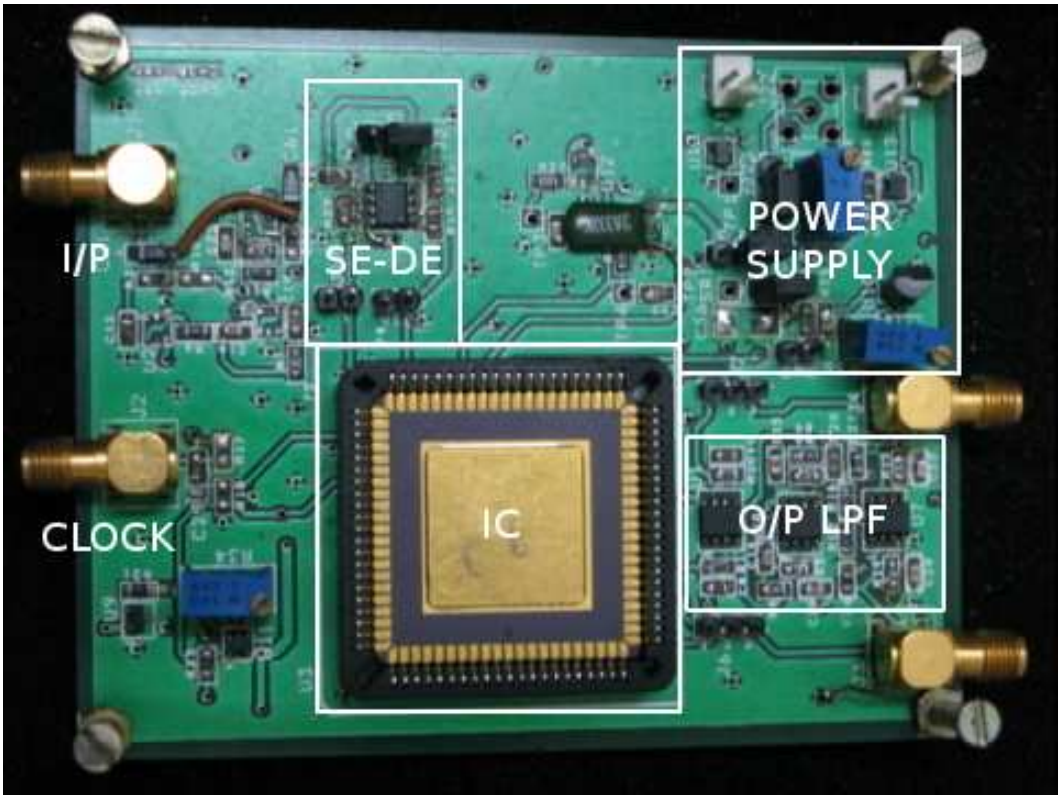


Figure 4.2: Test board

repeated for various frequencies from 1 Hz to 250 kHz. The chopper amplifier has a DC gain of 40 dB and a bandwidth of 130 kHz.

4.3 Measurement of Offset

The inputs of the amplifier are shorted to their respective common mode voltages and the output voltages are measured. Table 4.1 shows the offset readings taken from one of the sample chips.

Table 4.1: Offset measurements

V_{clk}	V_{outp} **(mV)**	V_{outm} **(mV)**	V_{offset} **(mV)**
LOW	959.2	853.6	105.5
HIGH	874.3	929.2	-54.9

The offsets at the two clock phases are not identical. Hence chopping with a clock of 50 % duty cycle will not eliminate the offset completely. The reason for this asymmetry in offset values is explained in the following section.

4.3.1 Analysis of Offset results

4.3.2 Transistor Mismatch Offset

The first stage of the three-stage opamp is separately analysed. Fig. 4.3 shows the circuit schematic of the first stage opamp with its V_{TH} mismatch modelled as a voltage source at the gates of the transistors.

- Mismatch is modelled with voltage sources placed at the gates of the transistors. $V_{op} - V_{om}$ when V_{ip} and V_{im} are held at V_{CM} is the offset.
- $Vbias_{34}$, $Vbias_{56}$ and $Vbias_{78}$ are the bias voltages of M3-M4, M5-M6 and M7-M8 respectively.
- Superposition principle is used to analyse the offset offered by each transistor pair.

Vos_{12} As depicted in Fig. 4.4, during Φ_1 I flows from M1-M3 to V_{om} and I+ΔI_{12} flows from M2-M4 to V_{op}. During Φ_2 the opposite happens i.e., I+ΔI_{12} flows into V_{om} from M2-M3 and I flows into V_{op} from M1-M4. Therefore the offset caused in the output due to Vos_{12} will change in sign at both the clock phases with the magnitude being the same.

Vos_{34} Similarly from Fig. 4.5 it is seen that at Φ_1 again I flows to V_{om} and I+ΔI_{34} flows to V_{op}. During Φ_2 still I flows into V_{om} and I+ΔI_{34} flows into V_{op}. At the alternate clock phases, the arms of M3-M5 and M4-M6 do not interchange hence the offset offered by Vos_{34} does not change either in sign or in magnitude.

Vos_{56} Offset offered by Vos_{56} will follow the same behaviour as seen by Vos_{34}. During Φ_1 and Φ_2, I is drawn out of V_{om} and I+ΔI_{56} is drawn out of V_{op}.

Vos_{78} Offset offered by Vos_{78} will follow the same behaviour as seen by Vos_{12}, since the drain arms of M7 and M8 changes its connectivity.

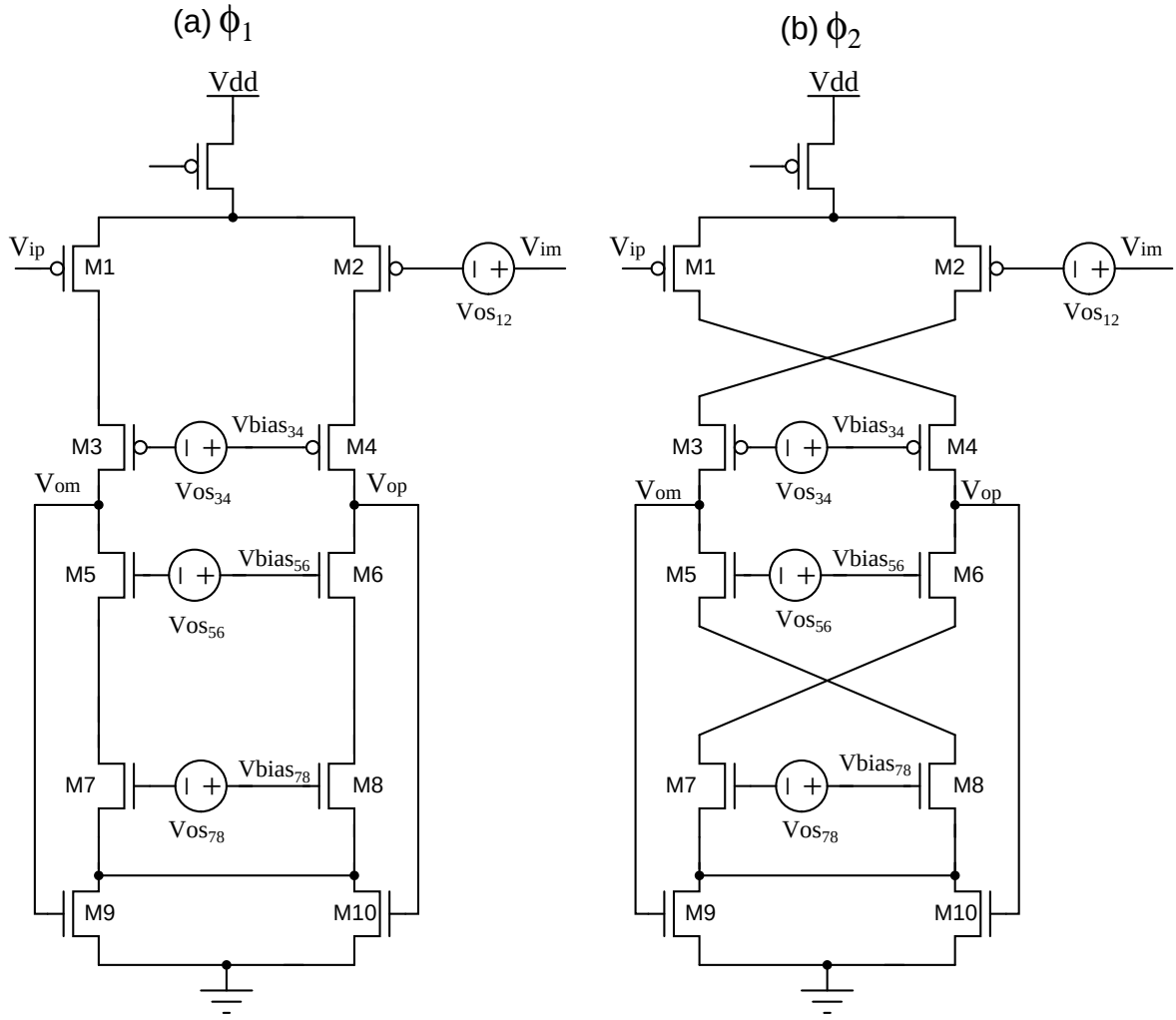


Figure 4.3: Opamp structure in the two clock phases

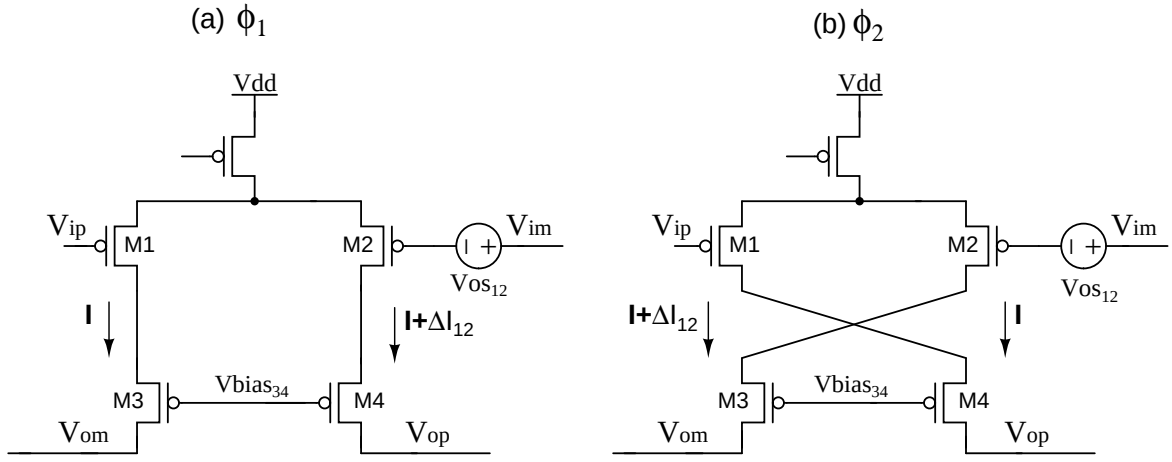


Figure 4.4: Offset due to Vos_{12}

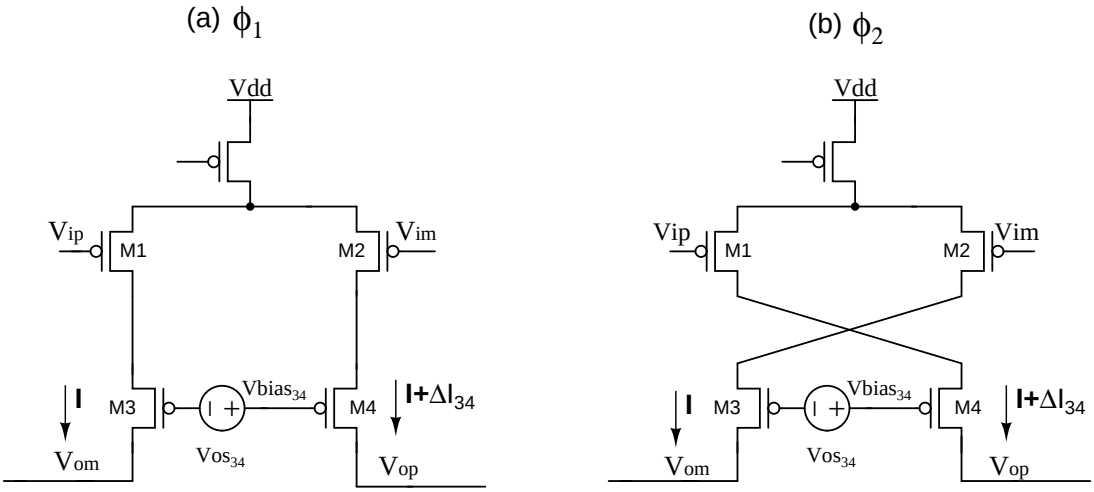


Figure 4.5: Offset due to Vos_{34}

The above analysis proves that during the two clock phases the offset voltage is different.

4.3.2.1 Switch Mismatch Offset

Mismatch between the switches is modelled as a difference in ON-resistance. The equivalent voltage difference due to ΔR is $I_{BIAS}\Delta R$ as shown in the Fig. 4.6. This error voltage can be moved to the drain terminal from the source terminal of M4 since the effect of them at the output is the same. Hence the offset due to switch mismatch is similar to the effect of Vos_{34} to the output offset.

$$\begin{aligned} R &= \frac{1}{\beta((V_{gs}-V_t)-V_{ds})} \\ \frac{\delta R}{\delta V_{gs}} &= \frac{-\beta}{(\beta(V_{gs}-V_t)-V_{ds})^2} \\ \Delta R &= \frac{-\beta}{(\beta(V_{gs}-V_t)-V_{ds})^2}\Delta V_{gs} \\ \Delta V_{gs} &= 3\sigma_{V_{switch}} \end{aligned}$$

Vos_{34} due to cascode transistors M3, M4 is 1.17 mV and Vos_{34} due to the PMOS switches is 1.73 μV. Hence the major contributor to the difference in offset at different clock phases are the cascode transistors. This problem is very specific to the architecture in our design since choppers are placed at the cascode nodes of

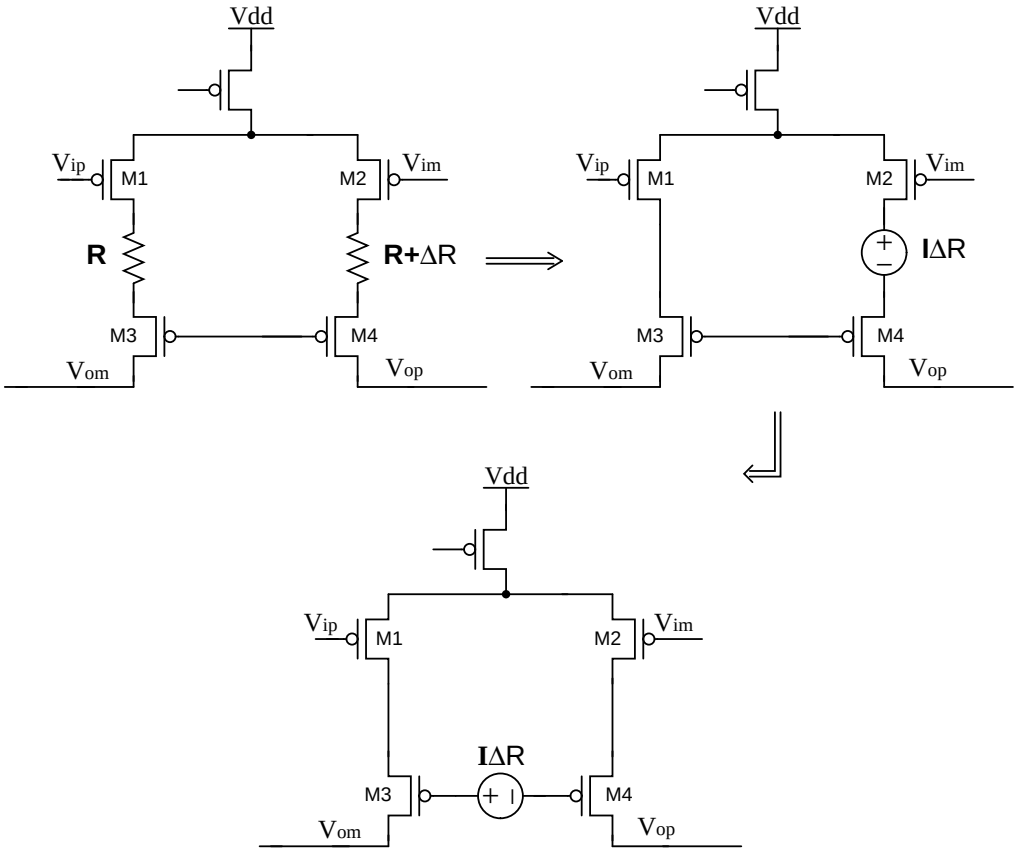


Figure 4.6: Offset due to chopper switches

the opamp. Offset of the cascode transistors do not get chopped. The contribution of each individual transistor's mismatch to the output offset is theoretically calculated and tabulated in Table 4.2. $V_{OS\_OUT} = (V_{OS\_IN})$ X (101). Though the cascode transistor's offset voltage is multiplied by $\frac{g_{ds}}{g_m}$, this factor is still large enough to deteriorate the accuracy.

4.4 Measurement of Noise

To measure noise of the chopper amplifier alone, the inputs are again shorted and noise spectrum is seen at the output. The amplifier has a DC gain of 40 dB. The output of the amplifier is fed as input to a Delta Sigma Modulator (DSM) whose dynamic range in the bandwidth of interest is sufficient to measure the noise power of the chopper amplifier.

- Differential Outputs of the amplifier are connected to the Delta Sigma Mod-

Table 4.2: Calculation of offset voltage

Transistor	V_{OS_IN}	V_{OS_OUT}
M1-M2	$V_{OS_{12}}$	54 mV
M3-M4	$\frac{\frac{gm_{34}}{1+\frac{gm_{34}}{gds_{12}+gds_{34}}}V_{OS_{34}}}{gm_{12}}$	6.4 mV
M5-M6	$\frac{\frac{gm_{56}}{1+\frac{gm_{56}}{gds_{78}+gds_{56}}}V_{OS_{56}}}{gm_{12}}$	18 mV
M7-M8	$\frac{gm_{78}V_{OS_{78}}}{gm_{12}}$	147 mV

ulator board's inputs

- A clock of 6.144 MHz is required for the DSM block
- The output is captured in a Logic Analyzer from which the output spectrum is obtained after further processing in Matlab

Readings are taken with and without chopping of the amplifier. A clock of 10 kHz is used for chopping. Peaks at multiples of clock frequency are seen at the output spectrum as shown in Fig. 4.7. Increasing the clock frequency suppresses the 1/f noise even further. The close up view of the measured noise in the bandwidth of interest is shown in Fig. 4.8. Table 4.3 compares the simulated as well measured integrated noise of the amplifier seen at the output over a bandwidth of 1 Hz to 1 kHz. The simulated and measured results from the chip closely match each other. Accuracy of the measured result is limited by the maximum number of samples that can be acquired by the Logic Analyzer to plot the power spectral density.

Table 4.3: Output integrated noise of the amplifier

Clock	**Simulated:**$V_{N\_OUT}(\mu V)$	**Measured:**$V_{N\_OUT}(\mu V)$
No Clock	209.54	228
10 kHz	76.34	92.927
50 kHz	50.53	64.44

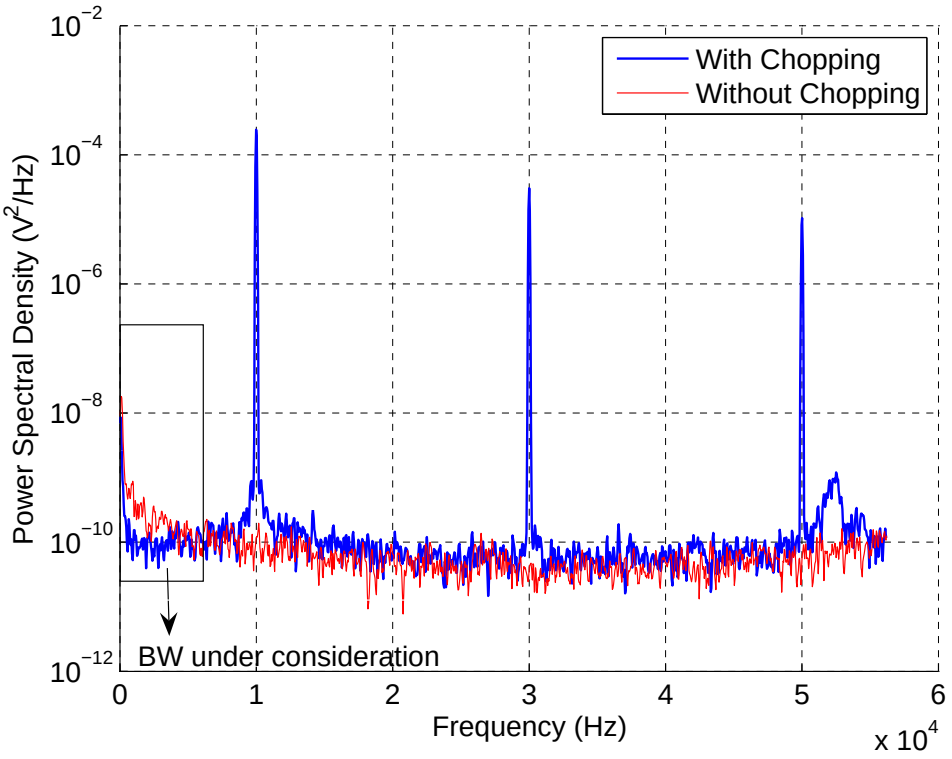


Figure 4.7: Noise measured at the output of the amplifier before and after chopping

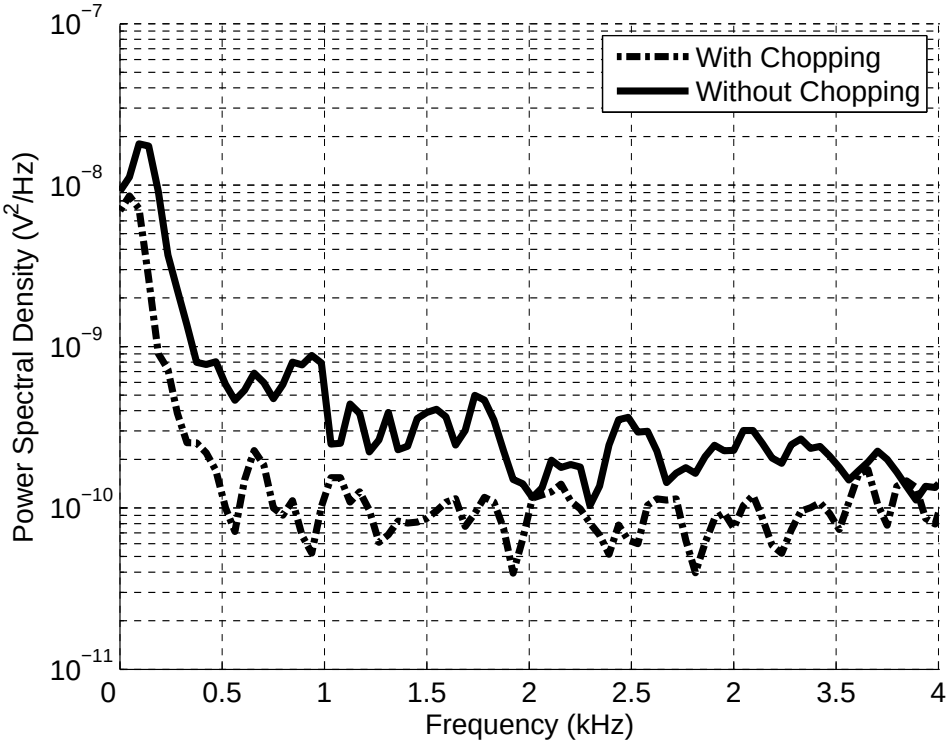


Figure 4.8: Close up view of measured noise before and after chopping

Table 4.4: Consolidated results

Parameter	**Value**
Gain	40 dB
Bandwidth	130 kHz
Input referred Noise Voltage (1 Hz - 1 kHz)	929 nV
Input referred Offset	506 μV

4.5 Inference

The measured results are consolidated in Table 4.4. The contribution of the offset from the cascode transistor is considerable in the above design. Through careful design this value of offset can be brought down but cannot be eliminated completely. To achieve lesser than microvolts of offset further modifications to the architecture needs to be done. Chapter 5 discusses a technique by which the above discussed problem can be solved.

CHAPTER 5

Thermocouple Signal Conditioner

The chopper amplifier is one of the blocks needed to condition a thermocouple signal. Cold junction compensation also needs to be performed for which a room temperature sensor is required. A complete solution for the thermocouple signal conditioner is also desired. The range of temperature that needs to be measured is from -100 ^{o}C to 1000 ^{o}C. With such a wide input range, the outputs also need to swing widely. This requires a supply voltage higher than 1.8 V. Hence a process (0.35 μm) with higher voltage tolerance is used. The design of each block in the signal conditioner is described below.

5.1 Chopper Amplifier

The three-stage Nested Miller Compensated opamp designed in 0.18 μm process is exported to 0.35 μm technology. It is then further modified to work properly in 0.35 μm process. The opamp is placed in voltage-series feedback with appropriate gain which is referred to as the chopper amplifier. The input voltage range to be measured is 40 μV to 40 mV. The maximum output voltage that can be attained is limited by the supply voltage (3.3 V). Hence the gain of the chopper amplifier must be less than 80. A value of 50 i.e. 34 dB is chosen. Test results of the first cut design showed that the contribution of offset from the cascode transistors were considerable enough to degrade the accuracy, since they are not chopped by the choppers. To counter this problem, the contribution of offset from the cascode transistors must be reduced in order to meet the accuracy specification. This requirement is taken care in the new design and Table 5.1 enumerates the offset voltage contribution of each pair of transistors of the first stage opamp to the output, that can be expected from this design. The circuit structure can be referred from Fig. 3.6. The standard deviation in relative threshold voltage

mismatch of each device is calculated from the formula, $\sigma_{V_{TH}} = \frac{A_{V_T}}{\sqrt{WL}}$ where A_{V_T} is the MOS threshold voltage mismatch parameter, which is found to be 9.5 mV μm for NMOS transistor and 14.5 mV μm for PMOS transistor in 0.35 μm technology. The sizes of the transistors used in the first stage of the three-stage opamp are shown in Table 5.1 from which the maximum deviation limit $3\sigma_{V_{TH}}$ is calculated. The respective transconductances and output conductances of each device are also shown from which the contribution of every transistor's mismatch voltage referred to the input of the chopper amplifier is calculated (i.e V_{OS_IN}). During design the transistors were sized such that the offset voltage contribution from the cascode devices are to a minimum since they are not chopped by the choppers. V_{OS_OUT} = V_{OS_IN} X 51, since the closed loop gain of the chopper amplifier we have set here is 50.

Table 5.1: Offset Voltages of first stage opamp

Transistor	**W/L** (μm/μm)	**3$\sigma_{V_{TH}}$** (mV)	g_m/g_{ds} (μS/μS)	**V_{OS_IN}** (mV)	**V_{OS_OUT}** (mV)
PMOS input (M1-M2)	80/2	3.44	356.2/1.1	3.44	175
PMOS cascode (M3-M4)	100/1	4.35	514.1/1.971	0.0375	1
NMOS cascode (M5-M6)	48/1	4.11	559.4/5.734	0.087	1
NMOS load (M7-M8)	96/2	2.056	562.3/1.89	3.245	138

The three-stage NMC opamp designed in 0.35 μm technology has the following parameters.

$$G_{m1} = 356\,\mu S \tag{5.1}$$

$$G_{m2} = 245\,\mu S \tag{5.2}$$

$$G_{m3} = 1.8\,mS \tag{5.3}$$

The three-stage opamp is compensated with Miller capacitors C_{m1} and C_{m2} which is calculated for a load capacitor of 10 pF and found to be 7.6 pF and 2.7 pF respectively. Correspondingly C_{m1} and C_{m2} are chosen as 8 pF and 3 pF. R_m was chosen to be 2 kΩ. The circuit details of the design in shown in Fig. 5.1.

The frequency response of the three-stage NMC opamp is shown in Fig. 5.2.

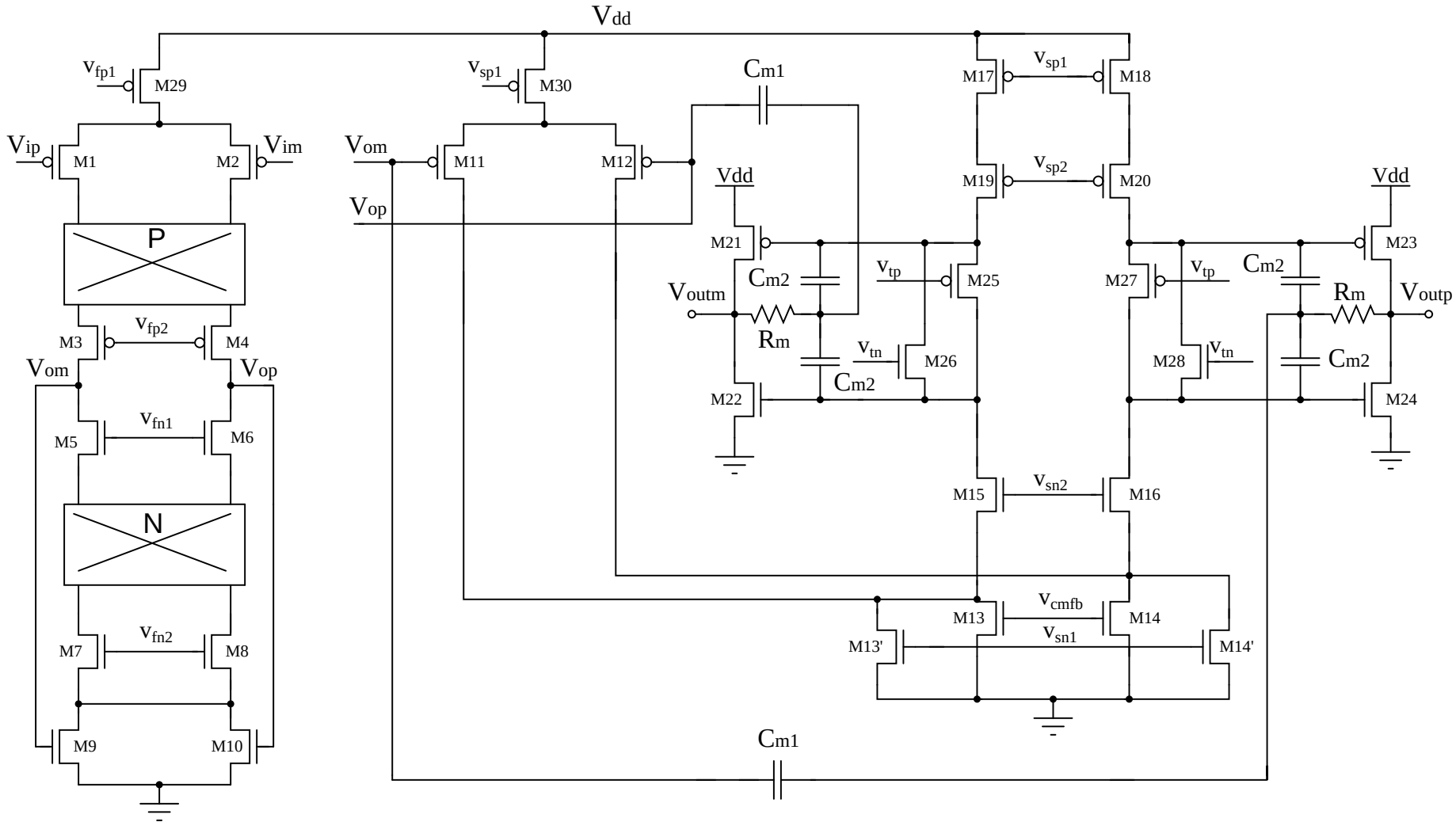


Figure 5.1: Three-stage NMC opamp circuit in 0.35 μm technology

FIRST STAGE	SECOND STAGE	THIRD STAGE
M29 : 80 (1 µm/.5 µm)	M30 : 80 (1 µm/2 µm)	M25,M27 : 18 (.9 µm/.35 µm)
M1,M2 : 80 (1 µm/2 µm)	M11,M12 : 20 (1 µm/1 µm)	M26,M28 : 18 (.9 µm/.35 µm)
M3,M4 : 40 (2.5 µm/1 µm)	M17,M18 : 80 (1 µm/2 µm)	M21,M23 : 54 (1.5 µm/.7 µm)
M5,M6 : 40 (1.2 µm/1 µm)	M19,M20 : 80 (1 µm/1 µm)	M22,M24 : 27 (1.5 µm/.7 µm)
M7,M8 : 80 (1.2 µm/2 µm)	M15,M16 : 20 (.5 µm/.35 µm)	
M9,M10 : 40 (1 µm/4 µm)	M13,M14 : 10 (.65 µm/.65 µm)	
	M13',M14' : 50 (.65 µm/.65 µm)	

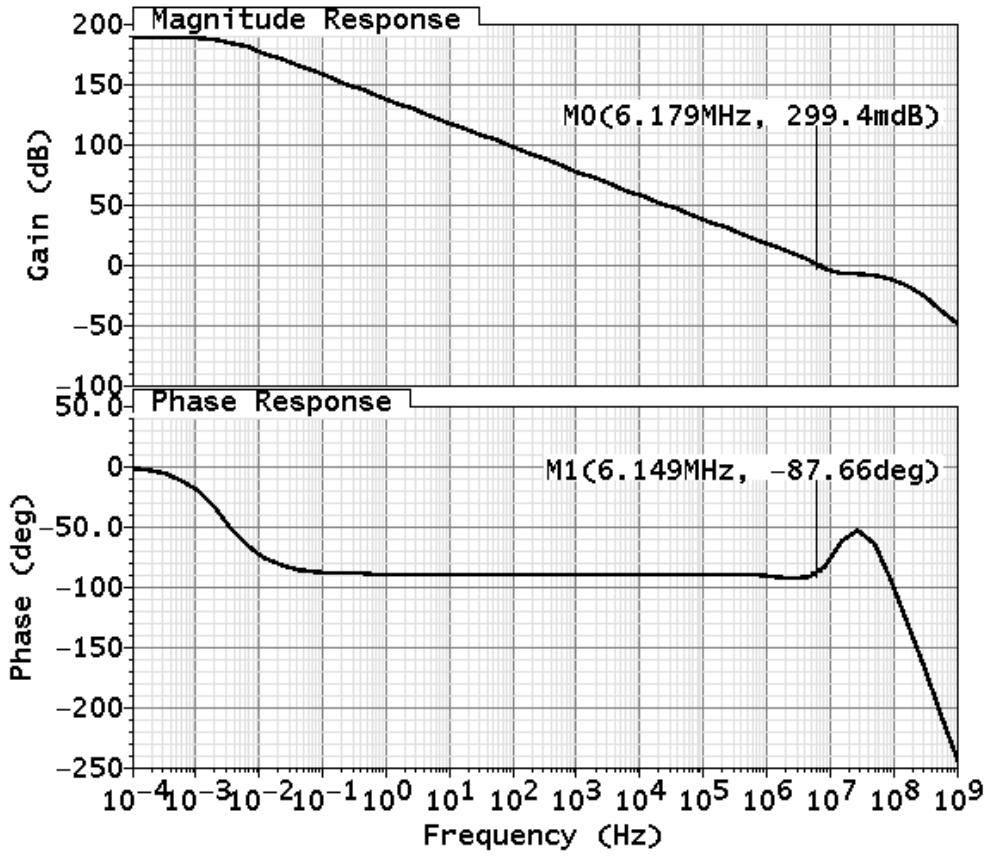


Figure 5.2: Magnitude and phase frequency response of the NMC opamp

5.1.1 Nested Chopping

Though careful design of the opamp reduces the offset of the cascode transistors, to achieve offsets in the range of nanovolts another set of choppers are placed to chop away the residual offsets that might remain due to switching [11] as well as the offsets of the cascode transistors. This is referred to as Nested Chopping. Fig. 5.3 shows the basic idea of nested chopping. The offset of the amplifier is reduced by applying another pair of choppers, but now operating at a lower frequency. This frequency can be lower than the 1/f noise corner frequency of the amplifier since that is already removed by the inner choppers [12]. The outer pair of choppers is running at a much lower frequency than the inner pair, hence the residual offset due to spikes of these choppers is negligible. Even though the outer choppers are working at a much lower frequency than the inner choppers, the switching

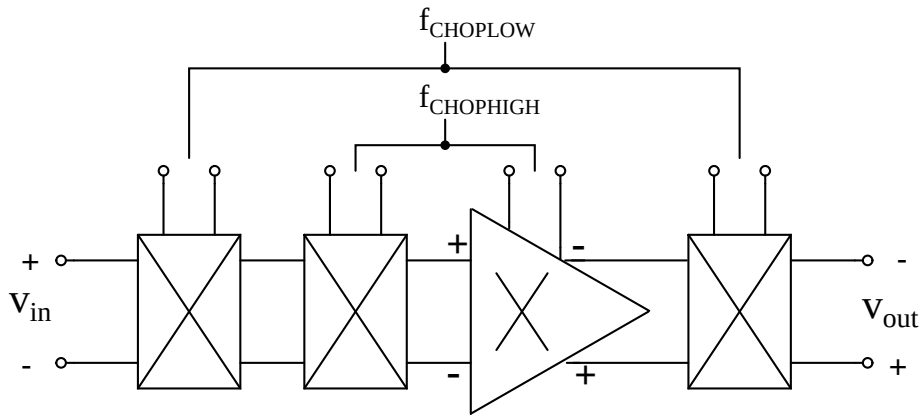


Figure 5.3: Principle of nested chopping

noise is directly coupled to the output. To avoid this problem the choppers are absorbed within the opamp. The possible location of the outer choppers are shown in Fig. 5.4.

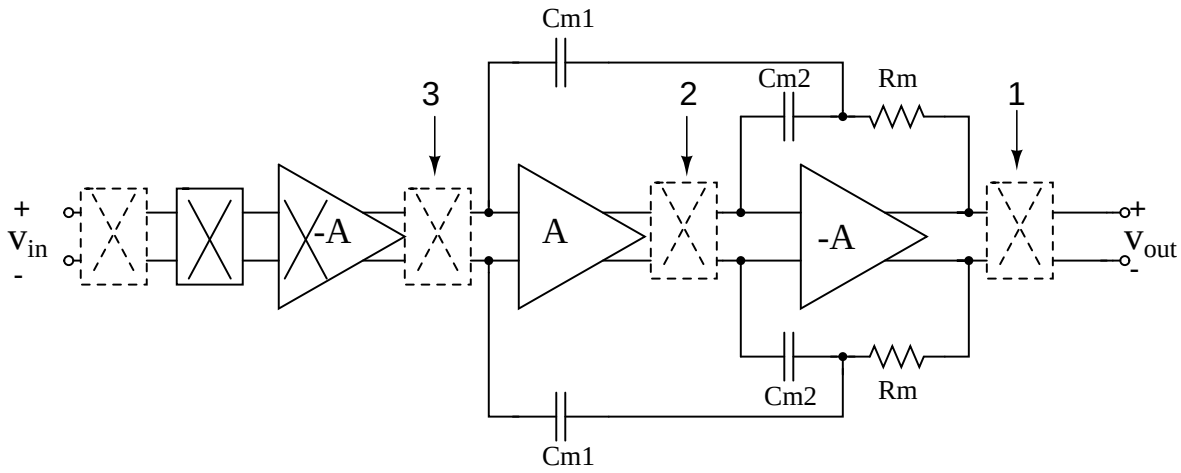


Figure 5.4: Possible location of outer choppers in NMC opamp

The choppers shown in dotted lines are operating at a lower switching frequency. The signal is modulated by both the choppers running at lower and higher frequencies before amplification. First level of demodulation occurs at the first stage opamp which has choppers running at $f_{CHOPHIGH}$. The second level of demodulation can be carried out by placing the low frequency chopper either at location 1 or 2 or 3.

- The advantage of placing the chopper circuit at location '1' is that the offset due to mismatch between the devices in the second stage opamp as well as

the third stage opamp is removed. But since this is the output node chopping at this node involves breaking the feedback loop periodically at $f_{CHOPLOW}$. This causes slight ringing in the output which settles to the right value once the feedback is restored. The residual offset due to the ringing at the output is more than the offset contributed by the second and third stage opamps. Hence placing the chopper should not be placed in location '1'.

- The chopper circuit cannot be placed at location '2' because the phase of the NMC amplifier is affected. In one of the clock phases the switches of the chopper circuit will be connected in such a way that C_{m2} and R_m cannot perform Miller compensation because they will be in positive feedback. With the amplifier uncompensated in one of the clock phases, placing it in feedback causes either oscillation or saturation to the rails in the output.

- By placing the chopper circuit at location '3' neither the amplifier's phase response affected nor the feedback loop broken at the output node. Like discussed before in Chapter 2 the switch non-linearities are reduced by a factor of their loop gain. Though the offset voltages from the second stage opamp and third stage opamp are not removed, they contribute to a small fraction that it is ignored.

PSS analysis is done to see the effect of nested chopping to the noise of the amplifier. The amplifier is simulated with clocks running at 5 kHz and 40 kHz. $f_{CHOPLOW}$ is chosen to be a factor of $f_{CHOPHIGH}$ so that the solution is periodic at $f_{CHOPLOW}$ and PSS analysis can be used. Pnoise analysis is performed after PSS analysis. The voltage noise spectral density of the amplifier with and without nested chopping is shown in Fig. 5.5. The solid line represents the input referred noise voltage of the NMC amplifier and the dashed line shows the input referred noise voltage after chopping. Small peaks at 5 kHz and 15 kHz can be seen which are the clock and its harmonics. A ten fold reduction in noise voltage can been seen from the plots. The input referred noise voltage integrated over a bandwidth of 1 Hz to

1 kHz is 3.66 μV before chopping and after chopping the same becomes 355 nV.

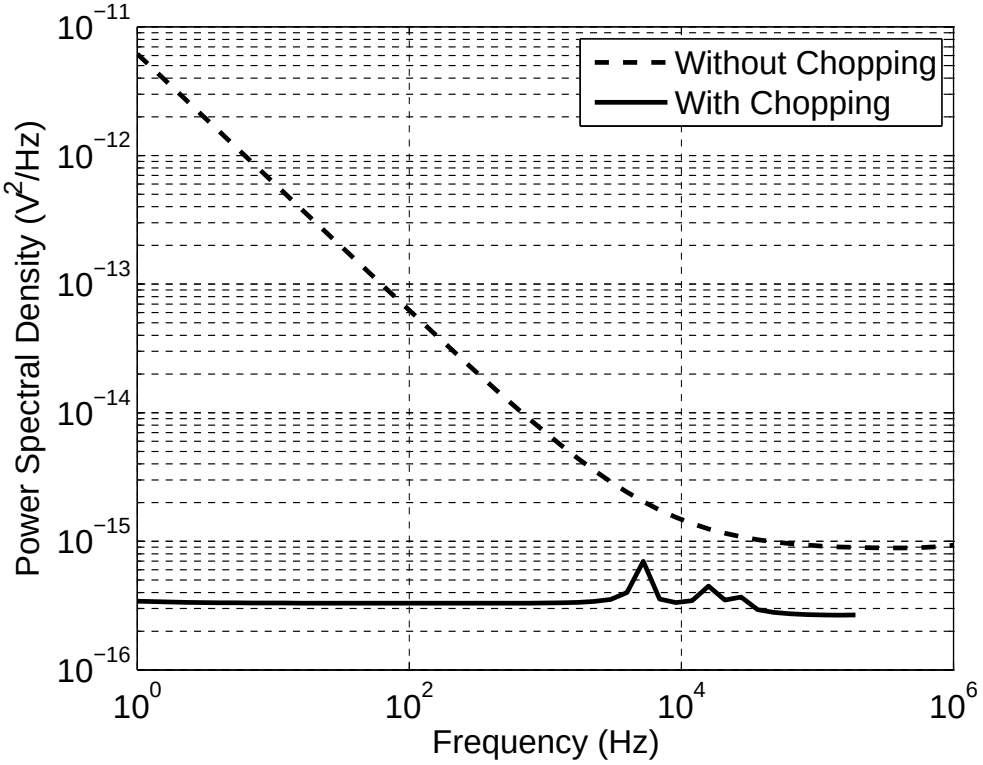


Figure 5.5: Input referred noise spectral density of the NMC opamp

The other parameters of the opamp are tabulated in Table 5.2. Offset of the

Table 5.2: NMC opamp parameters

Parameter	**Value**
Technology	AMS 0.35 μm CMOS
Supply Voltage	3.3 V
Quiescent Current	600 μA
Unity Gain Bandwidth	6 MHz
β	1/51
DC Loop Gain($\mid A\beta \mid$)	154 dB
Phase Margin(180- $\angle A\beta$)	89^o
Slew Rate	6.5 V/μs
PSRR @ 50 Hz	87 dB
CMRR @ 50 Hz	160 dB

chopper amplifier which is our primary concern, is simulated using the Monte-Carlo model present in 0.35 μm technology. Fig. 5.6 shows the histogram plot of the input referred offset voltage of the chopper amplifier without chopping. The offset voltage of the chopper amplifier without chopping follows a gaussian

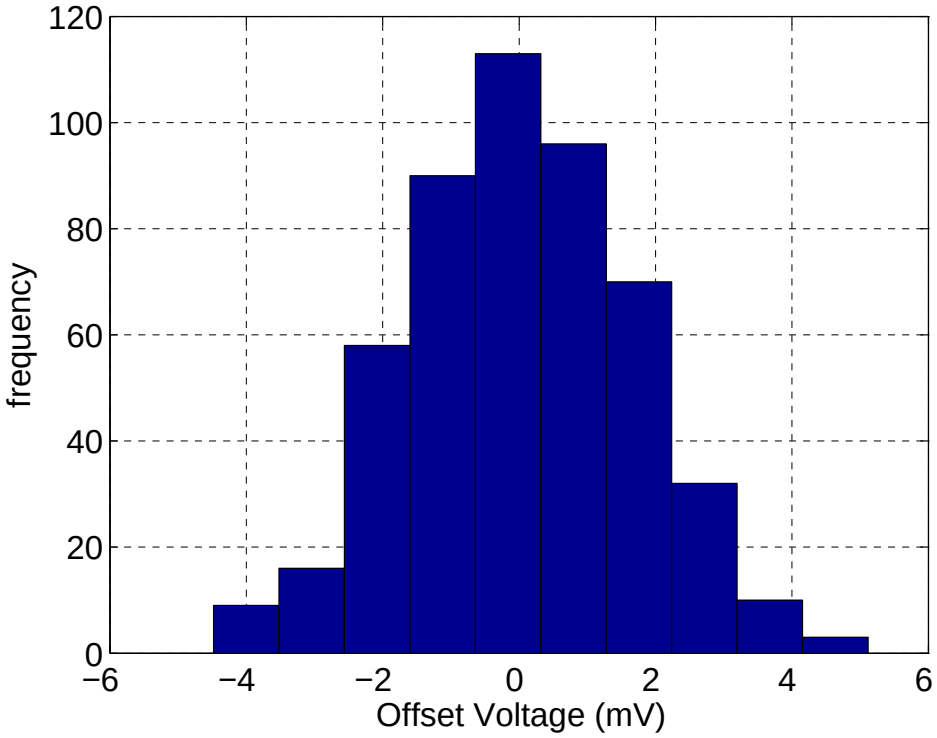


Figure 5.6: Histogram of the input referred offset voltage

distribution with a $3\sigma_{V_{OS}}$ of 5 mV. This closely matches with the theoretically calculated value of 6.8 mV.

5.2 Oscillator

The clocks required for the chopping amplifier can be obtained from an external clock generator or an on chip oscillator can be designed for a full system solution. Frequency in the range of few tens of kHz is required. In 0.35 μm technology the delay of an inverter with a PMOS-to-NMOS size ratio of 2 and W=20 μm, L=10 μm is 25 ns. To achieve frequencies in the range of kilohertz a ring oscillator with a chain of more than hundred inverters will be required. Hence a relaxation oscillator is chosen for this application. Fig. 5.7 shows the circuit diagram of a simple Schmitt trigger based oscillator [13]. The time period is given by the formula $2RC\ln(\frac{1+\lambda}{1-\lambda})$. The derivation of this formula is detailed in Appendix B. Where $\lambda = \frac{R_1}{R_1+R_2}$. R_1 is chosen to be equal to $R_2 = 100\,k\Omega$, and so $\lambda = \frac{1}{2}$.

The absolute value of these two resistors is decided based on the current sourcing capability of the output stage of the opamp used in positive feedback. Due to area constraints the capacitor's value is limited to 1 pF and the resistor's value is chosen appropriately. The R value to generate a frequency of 100 kHz with C of 1 pF is 4.5 MΩ. A clock divider is used to generate the lower and the higher frequencies required for nested chopping of the amplifier. Tunability is obtained by placing capacitances in parallel with switches controlled by external bits that is provided off-chip.

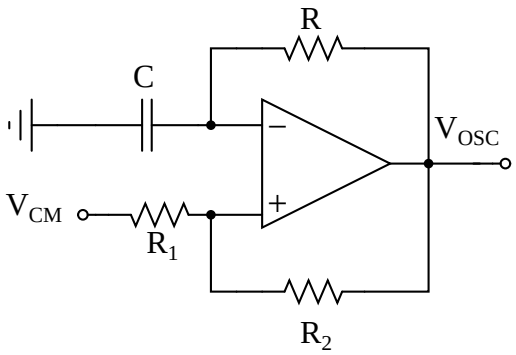


Figure 5.7: Relaxation oscillator

5.2.1 Design details

Once the frequency of oscillation is decided, the specifications of the opamp are obtained. The unity gain frequency of the opamp must be higher than the frequency of oscillation required. Offset and Gain error in the amplifier will change the threshold point at which switching occurs in the Schmitt trigger that will change the frequency of oscillation. Equation below shows the effect of the above errors to the frequency of oscillation,

$$\mathrm{T} = 2\mathrm{RCln}\left[\frac{1+\lambda-\Delta\lambda}{1-\lambda+\Delta\lambda}\right] \tag{5.4}$$

The analysis of the circuit errors to the frequency of oscillation is shown in Appendix B. The opamp is designed choosing $\Delta\lambda = 0.01$. The circuit details of the opamp is shown in the Fig. 5.8. The opamp designed has a gain of 60 dB with an

input referred offset voltage of 10 mV.

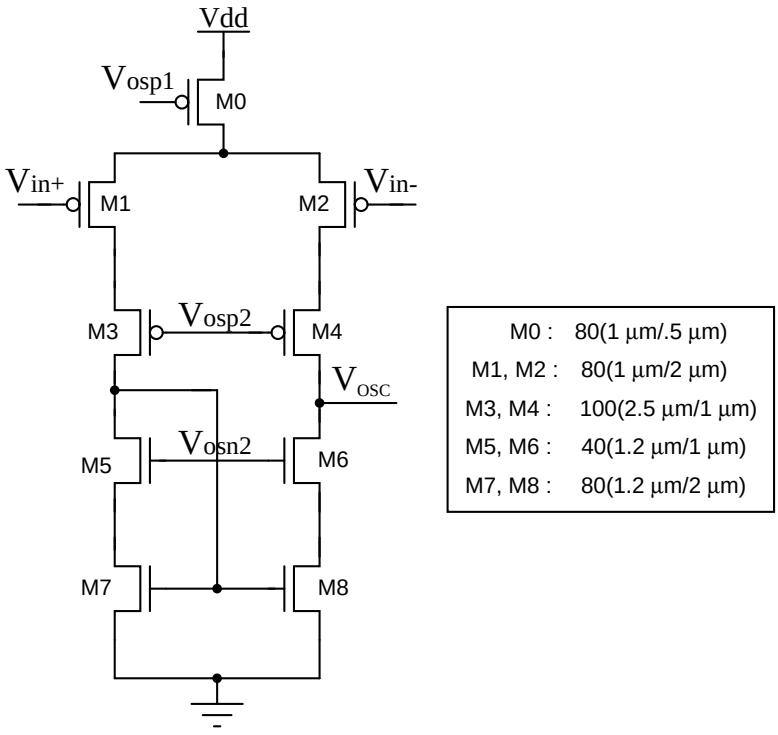


Figure 5.8: Transistor schematic of the opamp present in the relaxation oscillator

5.3 CJC Buffer

For Cold Junction Compensation, the room temperature is sensed from an external BJT. The base-emitter voltage of bipolar transistors exhibit a negative temperature coefficient. $\frac{\partial V_{BE}}{\partial t} \approx$-2 mV/^{o}C. V_{BE} is buffered, level shifted and amplified with an appropriate gain such that the thermocouple amplifier's output is the sum of the room temperature as well as the input. K type thermocouple's temperature sensitivity is approximately 40 μV/^{o}C and the gain of the chopper amplifier is 34 dB. With this we can obtain an voltage output of 2 mV/^{o}C. Since the temperature sensitivity of V_{BE} is -2 mV/^{o}C, it requires a gain of -1 to exactly nullify the room temperature difference. The cold junction compensation follows the relation,

$$V_{OUT} = A\ V_{IN} + V_{CJC} \tag{5.5}$$

5.3.1 Design details

The output of the CJC buffer must provide an output of 700 mV when the reference junction is at 25 ^{o}C. To achieve this, bias current into the BJT is tuned such that, at 0 ^{o}C it reads 650 mV which will be level shifted to match the V_{CM} level of the amplifier. Fig. 5.9 shows the buffer along with the level shifter circuit. The V_{CM}

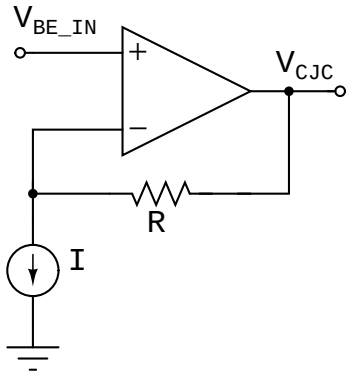


Figure 5.9: CJC buffer and level shifter

of the amplifier is 1.65 V, hence V_{BE} must be level shifted by 1 V.

$$V_{CJC} = V_{BE\_IN} + IR \tag{5.6}$$

The IR drop accurately has to be 1 V across all corners, process and resistant to supply variations. This can be achieved by providing a mechanism wherein either R or I changes with corners and process such that IR drop remains constant. Fig. 5.10 shows the circuit with which a constant IR drop can be obtained. The opamp buffer's output is given by the relation,

$$V_{CJC} = V_{BE\_IN} + \frac{V_{REF}}{R_{REF}}\ n\ R \tag{5.7}$$

where 'n' is the current mirroring factor. The resistors R and R_{REF} are matched resistors (i.e, made from common resistor segments in the same type of resistor material). Resistor tolerances will track each other therefore providing control of the level shifting. Cascode transistors are used to provide precise mirroring of the reference current. The only circuit imperfections that might affect the accuracy

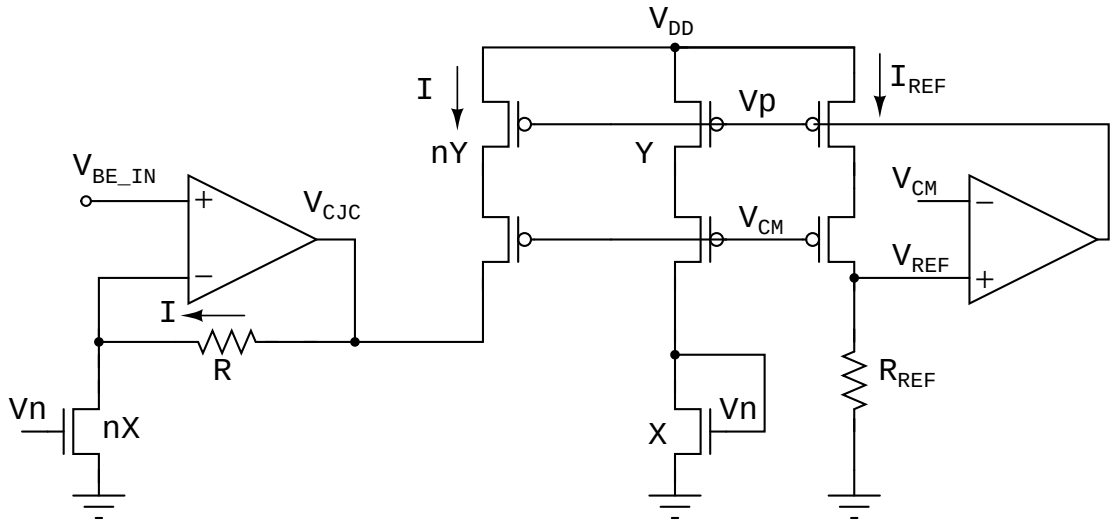


Figure 5.10: Transistor level schematic of the level shifter

of the level shifter are the opamp's offset and noise. The noise and offset can be modelled as a voltage source placed at the non-inverting terminals of the opamp. Let V_{OS1} be the offset voltage of the opamp in the reference generator and V_{OS2} of the opamp in the level shifter. The effect of these imperfections is shown as follows,

$$V_{CJC} = V_{BE\_IN} + V_{OS2} + \frac{V_{REF} + V_{OS1}}{R_{REF}} nR \tag{5.8}$$

$$\Delta V_{CJC} = V_{OS2} + V_{OS1} \frac{nR}{R_{REF}} \tag{5.9}$$

The effect of V_{OS1} can be reduced by increasing R_{REF} or reducing 'n'. Increasing R_{REF} would mean an increase in resistor area. Reducing the current mirroring ratio would imply burning an increased current in the reference generator circuit. Hence an optimum value is chosen to minimise the effect of offsets. In our design, $R_{REF} = 16.5\,k\Omega$, $R = 10\,\Omega$, n = 1 therefore $I = I_{REF} = 100\,\mu A$.

Next step is to design the opamps. Based on the application at hand appropriate topology is chosen. For instance, the opamp present in the level shifter circuit, opamp OA1 shown in Fig. 5.11 must cater to two specifications.

- Gain must be high
- Output of the opamp = Input of the opamp + 1 V

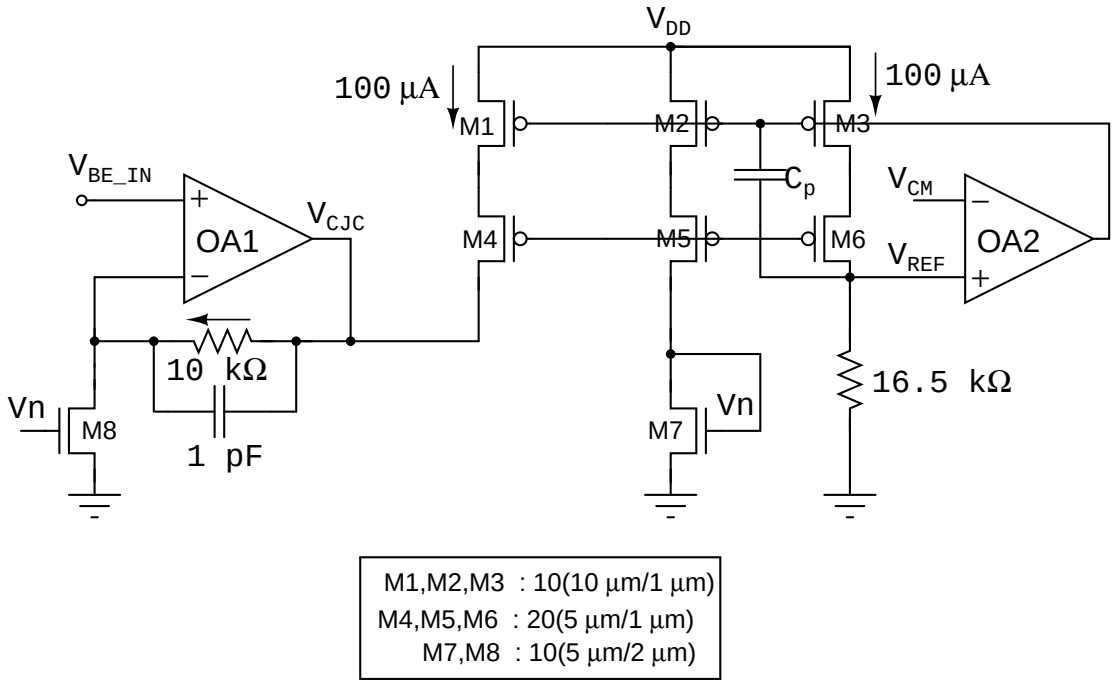


Figure 5.11: Final schematic with compensation capacitors

A single stage opamp is not suitable since the second clause cannot be met. This is because

- Input common mode level of the opamp will be 650 mV. The V_{TH} of the transistors in 0.35 μm technology is 0.6 V for NMOS and 0.9 V for PMOS. Hence a PMOS input pair topology is only best suitable.
- For a PMOS transistor to remain in saturation $V_{DG} \leq V_{TH}$. Hence V_D can atmost be V_G+V_{TH}. Therefore V_D (i.e the o/p terminal of the opamp) of the input PMOS pair cannot reach 1.65 V whilst remaining in the saturation region.

A two stage architecture only would be a suitable topology for this particular circuit. The circuit details of the two-stage opamp is shown in the Fig. 5.12 Similarly, for the opamp in the reference generator (opamp OA2) a high gain topology is be used. Two stage and folded cascode opamp structures provide high gains and large swings. A two-stage topology is avoided since stability is an issue. The output of the opamp OA2 is fed to bias a transistor current source. This current source will

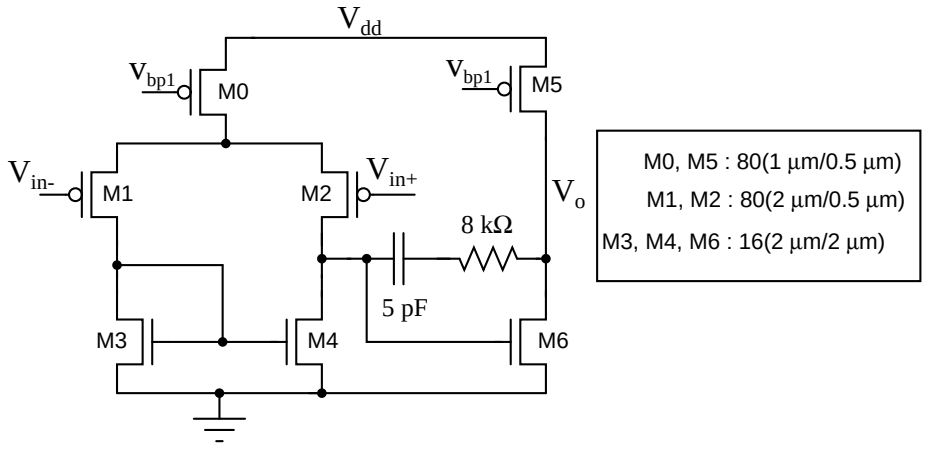


Figure 5.12: Transistor schematic of OA1

introduce at least one pole in the open loop transfer function, making it difficult to guarantee stability while placed in feedback. For this reason, a folded cascode topology is the preferred choice here. The folded cascode opamp along with the current source becomes a two stage opamp structure in closed loop. To ensure stability Miller compensation is done by placing capacitor $C_p = 1\,pF$ as shown in Fig. 5.11. Another capacitor of 1 pF is placed in parallel to the 10 kΩ resistor. This is to ensure high frequency stability of OA1. The circuit details of the folded cascode opamp is shown in the Fig. 5.13.

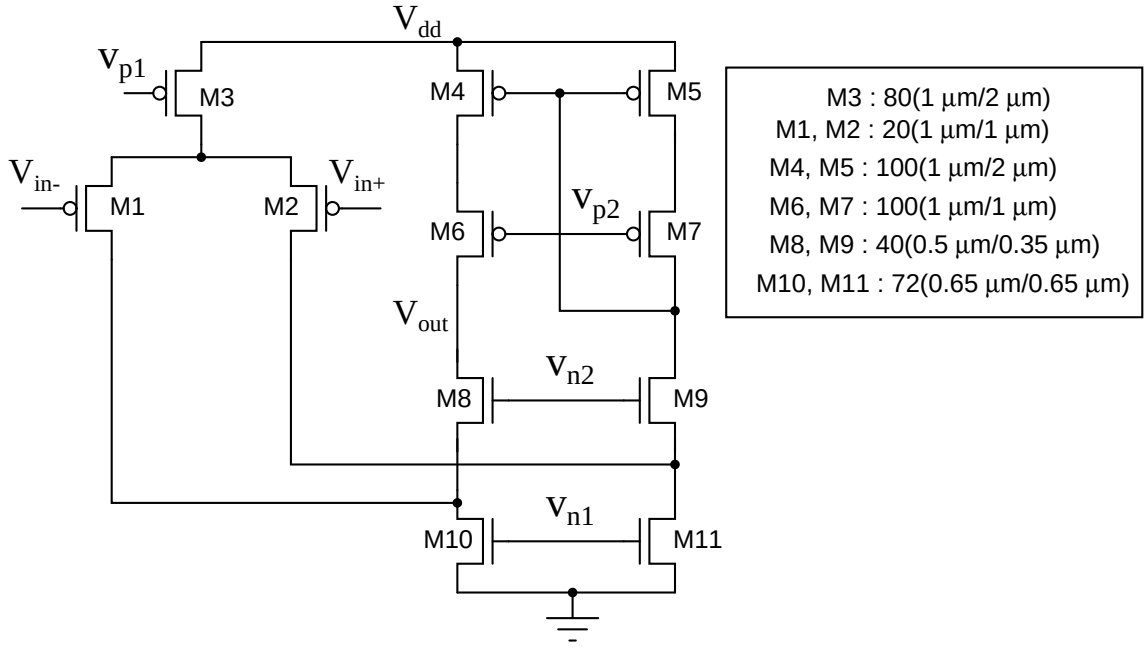


Figure 5.13: Transistor schematic of OA2

Table 5.3 is indicative of the efficiency of the buffer implemented. An input of 650 mV is given, and the buffer output is observed for all corners. This buffer draws 610 μA of current from a supply of 3.3 V.

Table 5.3: Corner simulation result of the CJC buffer

Corner	$\mathbf{V_{CJC}}$ **(V)**
Typical	1.650
Worstone	1.652
Worstpower	1.655
Worstspeed	1.648
Worstzero	1.651

5.4 Differential to Single ended converter

A single ended analog output which directly indicates the absolute temperature of the source is required. The differential outputs of the chopper amplifier needs to be converted to a single ended one which swings between 0 V and 5 V. Since

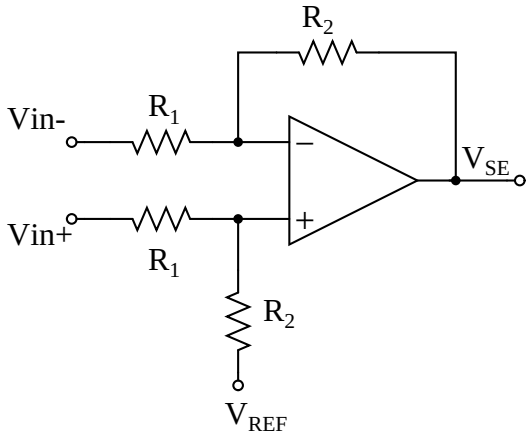


Figure 5.14: Differential to single ended converter

no further gain is required all the resistors are chosen to be same. The absolute value of them is decided based on the output resistance of the chopper amplifier and the noise as well current capability of the opamp used in the Differential to Single ended (DE-SE) converter. The output of the DE-SE converter is given by the equation,

$$V_{SE} = (Vin_{+} - Vin_{-}) + V_{REF} \tag{5.10}$$

Table 5.4: DE-SE characteristics

Parameter	Value
R_1,R_2	50 kΩ
Open loop gain	100 dB
Phase Margin	97^o
Input referred noise (1 Hz - 1 kHz)	350 μV
Supply Voltage	5 V
Quiescent Current	387 μA

V_{REF} is an external reference of 2.5 V. 5 V devices present in 0.35 μm technology are used in the opamp design present in DE-SE block.

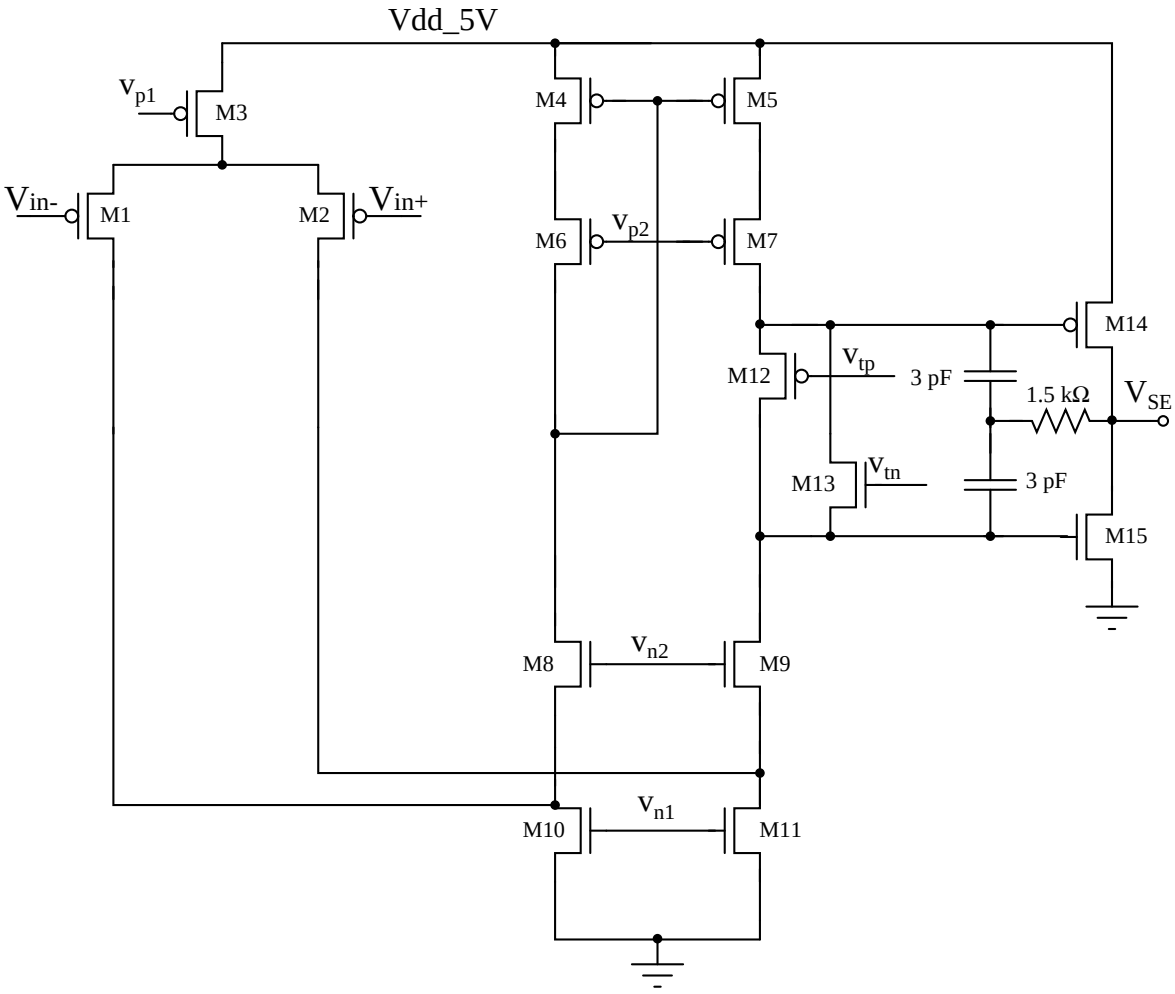
5.4.1 Design details

A two stage topology with class AB output stage structure is used to build the opamp. The circuit details of the opamp is shown in the Fig. 5.15
An elegant way to null the offset would be to tune the V_{REF}. The DC offset of the output stage can be measured with a no input condition, and tuned appropriately to null its effect. The electrical characteristics of the opamp used in the DE-SE converter is tabulated in Table 5.4.

5.5 Integrated Structure

The integrated block diagram of all the above blocks is shown in the Fig. 5.16. The CJC buffer senses the base-emitter voltage of a BJT device which is an indication of the room temperature. The thermocouple input is fed to the chopper amplifier. The buffered voltage is then added to the amplifier's output which is finally obtained in a single-ended format from the DE-SE converter block. The various clocks for the chopping operation are obtained from the clock generation block.

Chopping frequency can be varied by controlling the tuning bits C1 and C2. Table 5.5 shows the possible frequencies achievable.
The 'CLOCK DIVIDER' block divides V_{osc} by two and sixteen to generate V_{FAST}



M1-M2 : 20(1 µm/1 µm)	M14: 36(1.5 µm/0.7 µm)
M4-M5 : 80(1 µm/2 µm)	M15: 18(1.5 µm/0.7 µm)
M6-M7 : 80(1 µm/1 µm)	M1: 80(1 µm/2 µm)
M8-M9 : 50(0.65 µm/0.65 µm)	M12: 40(2 µm/0.5 µm)
M10-M11 : 100(0.65 µm/0.65 µm)	M13: 40(1 µm/0.5 µm)

Figure 5.15: Circuit Details of the opamp in DE-SE block

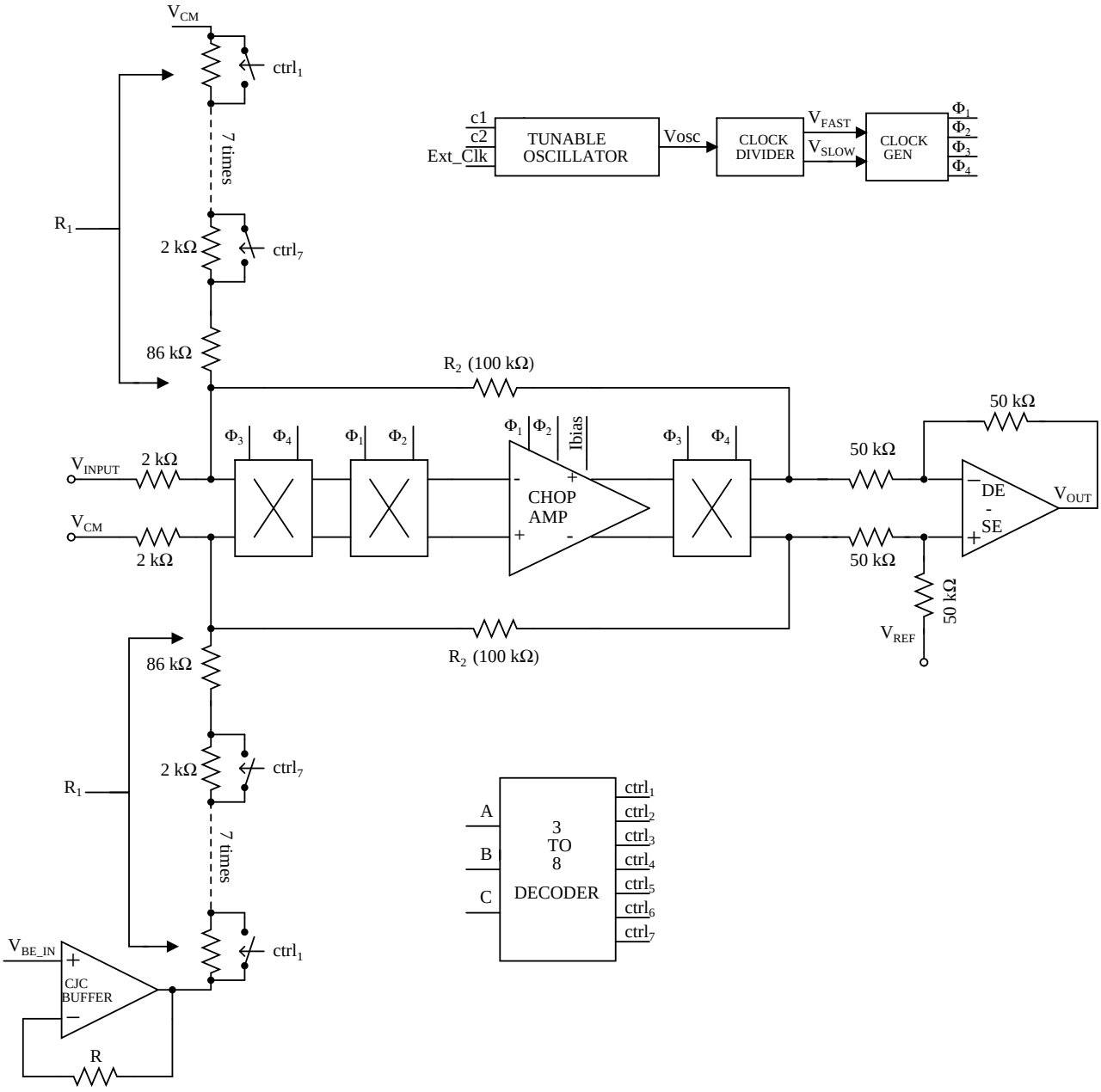


Figure 5.16: Block diagram of the signal conditioner

Table 5.5: Frequency control in the oscillator

C1	C2	Frequency
0	0	External Clock
0	1	71.4 kHz
1	0	58 kHz
1	1	50.5 kHz

and V_{SLOW} clock frequencies respectively. Non-overlapping clocks needed for chopping are generated by the 'CLOCK GEN' block. The gain of the chopper amplifier is 34 dB, hence after amplification of the input thermocouple signal the output sensitivity is 2 mV/^{o}C. The temperature sensitivity of BJT's base-emitter voltage is approximately -2 mV/^{o}C. Hence this signal does not require amplification, therefore can be directly inverted and buffered to be added to the output thus compensating for the room temperature. But in practise $\frac{\partial V_{BE}}{\partial t}$ is not exactly -2 mV/^{o}C but ranges across -1.8 mV/^{o}C to -2 mV/^{o}C. Hence to provide gain tunability to the CJC buffer's signal, resistor trimming is done and controlled with bits A, B and C. Table 5.5 illustrates the possible gains achieved using the control bits A, B and C.

Table 5.6: Gain control of the CJC buffer

BJT's temperature sensitivity (mV/^{o}C)	A	B	C	R_1($k\Omega$)	R_2($k\Omega$)	Gain
-2	0	0	0	100	100	1
-1.96	0	0	1	98	100	1.02
-1.92	0	1	0	96	100	1.042
-1.88	0	1	1	94	100	1.064
-1.84	1	0	0	92	100	1.087
-1.8	1	0	1	90	100	1.11
-1.76	1	1	0	88	100	1.136
-1.72	1	1	1	86	100	1.163

Fig. 5.17 shows the layout of the thermocouple signal conditioner. The integrated design occupies an area of 1 mm^2 consuming 6 mW of power. For testing purpose and due to the availability of silicon area, the chopper amplifier, CJC buffer and the DE-SE converter were separately placed additional to the above thermocouple signal conditioner. The 5 mm^2 die is housed in a JLCC 44 pin package. The

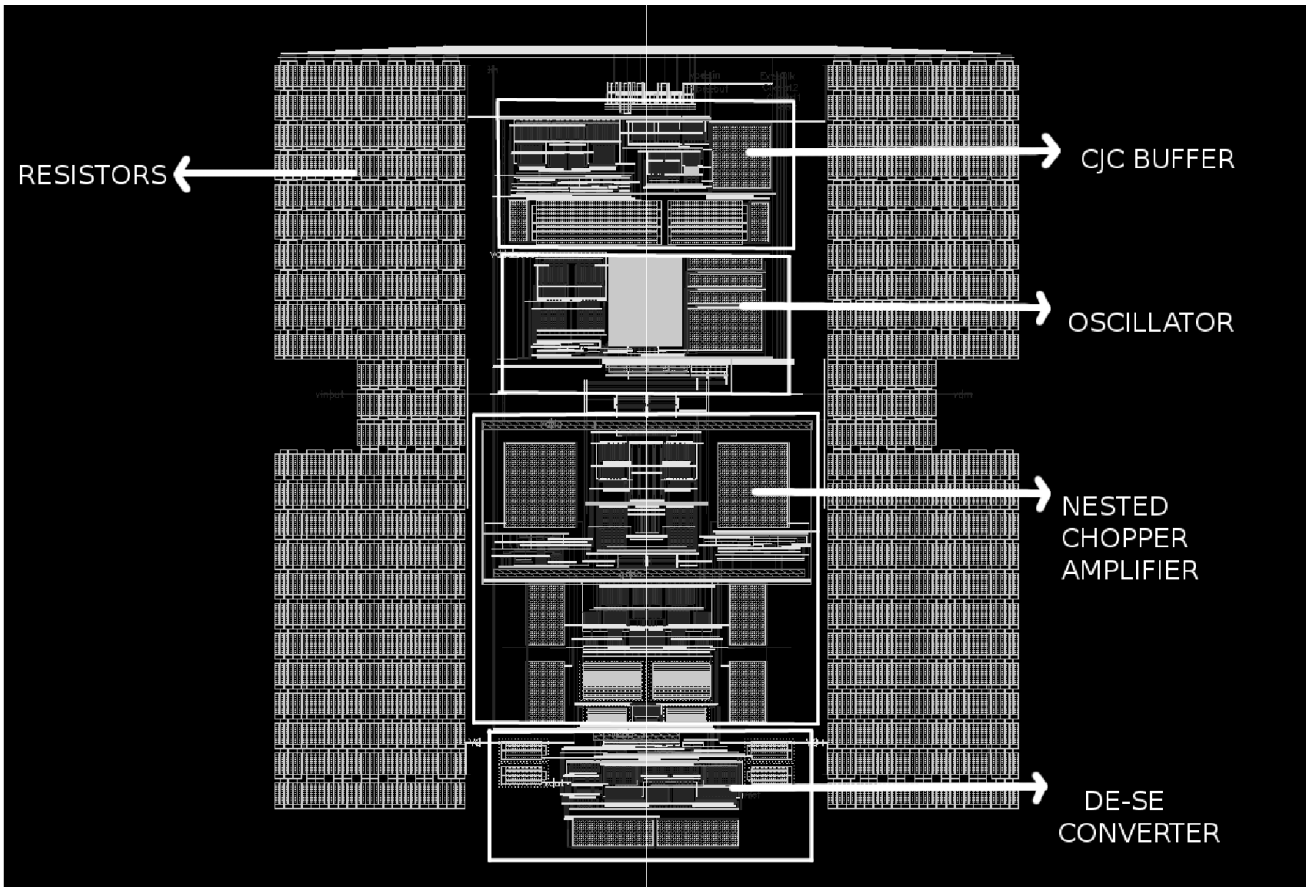


Figure 5.17: Layout of the signal conditioner

simulated results of the integrated structure is tabulated in Table 5.7. The voltage equivalent for a particular temperature is found from a thermocouple datasheet which is fed as V_{INPUT}. V_{OUT} is the amplified version of the input.

Table 5.7: Simulated result of the integrated design

Source Temp (^oC)	**Room Temp** (^oC)	$\mathbf{V_{INPUT}}$ **(mV)**	$\mathbf{V_{OUT}}$ **(V)**
100	0	4.096	2.704
100	30	2.851	2.704
99	0	4.055	2.702
101	80	0.838	2.706

CHAPTER 6

Conclusions

This thesis describes the analysis and design of precision sensor measuring circuits. In this work it is demonstrated that Chopper stabilization is the preferred choice over autozeroing, when the system is linear and low baseband noise is the most important requirement. Chopper stabilized amplifiers are best suited for low power, portable, very low noise, very small offset and offset drift, high performance applications such as electronic sensors. The problem of residual offset contributed by the cascode transistors is very specific to the architecture chosen in our design. Nested chopping is performed to eliminate this residual offset. After nested chopping the amplifier has an integrated input referred noise of 355 nV over a bandwidth of 1 Hz - 1 kHz by chopping at 5 kHz and 40 kHz. Traditionally chopping is performed with square wave of 50 % duty cycle. To deal with asymmetric offset as seen in the prototype design of the chopper amplifier, an asymmetric square wave sequence can be used to nullify its effect. But this cannot be predicted before fabrication and it varies from one sample to another. Hence a provision for tuning the duty cycle of the chopping square wave can be added. Chopping results in strong tones in the output spectrum of the amplifier at the chopping frequency and its odd harmonics. If these strong tones are unacceptable, even after filtering chopping can be done by a pseudo-random sequence. The idea of chopping within the opamps can be extended to different other architectures. Also instead of Miller compensation, feed forward opamps can be used to reduce power and area.

In the final design of a complete signal conditioning module, trimming of resistors is provided to compensate the gain of the CJC block for any variations in temperature sensitivity of the external BJT. The integrated circuit designed has

an output sensitivity of $2\,\mathrm{mV}/^{o}\mathrm{C}$. The thermocouple signal conditioner consumes around $6\,\mathrm{mW}$ occupying $1\,\mathrm{mm}^2$ of area. Thermocouple signal conditioning block senses the room temperature via an external BJT placed close to the cold junction. This can also be done using a PTAT CMOS temperature sensor.

APPENDIX A

Noise Reduction due to Autozeroing

The autozero principle can be used to cancel the amplifier's low frequency noise. The efficiency of this process will depend on the correlation between consecutive noise samples. It is equivalent to subtracting from the time varying noise a recent sample of the same noise. This indicates autozeroing effectively high pass filters the noise. The equivalent circuit for noise sampling is shown in the Fig. A.1. The voltage on the capacitor C is an ideal sample and hold signal. If kT_s are the sampling instants and h(t) the hold function, the voltage on the capacitor $V_C(t)$ is given by equation A.1.

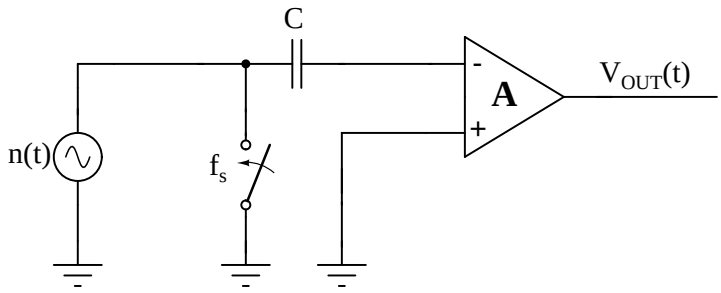


Figure A.1: Noise equivalent of the Autozero amplifier

$$V_C(t) = \sum n(kT_s)h(t - kT_s) \tag{A.1}$$

The output spectrum [14] can be calculated as follows,

$$\begin{aligned}
V_{OUT}(t) &= n(t) - \sum_{k=-\infty}^{k=+\infty} n(kT_s)h(t - kT_s \\
V_{OUT}(f) &= N(f) - \mathrm{sinc}(\pi f T_s)e^{-j\pi f T_s} \sum_{k=-\infty}^{k=+\infty} N(f - \frac{k}{T_s}) \\
V_{OUT}(f) &= N(f) - \mathrm{sinc}(\pi f T_s)e^{-j\pi f T_s}N(f) - \mathrm{sinc}(\pi f T_s)e^{-j\pi f T_s} \sum_{k=-\infty, k\neq 0}^{k=+\infty} N(f - \frac{k}{T_s}) \\
H_o(f) &= 1 - \mathrm{sinc}(\pi f T_s)e^{-j\pi f T_s}, k = 0
\end{aligned}$$

The output power spectral density can be decomposed into two parts. One is the baseband noise which is reduced by the autozeroing process and the other is due to the fold over components introduced by aliasing.

$$S_{V_{OUT}}(f) = |H_o(f)|^2 S_N(f) + \mathrm{sinc}^2(\pi f T_s) \sum_{k=-\infty, k\neq 0}^{k=+\infty} S_N(f - \frac{k}{T_s}) \qquad (A.2)$$

In conclusion, autozero amplifiers reduce the offset and 1/f noise by using sampling techniques at the expense of increased white noise in the baseband.

APPENDIX B

Relaxation Oscillator

A schmitt trigger based oscillator is shown in Fig. B.1. λ is given by $\frac{R_1}{R_1 + R_2}$ which decides the threshold point for the switching to occur from the positive rail to the negative rail.

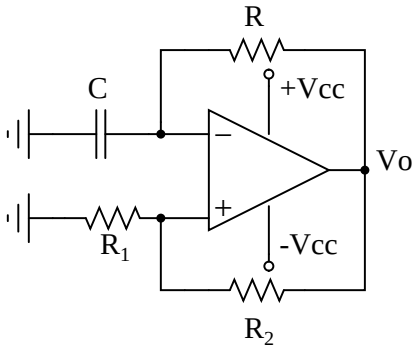


Figure B.1: Schmitt Trigger based Oscillator

When the voltage across the capacitor reaches $+\lambda V_{CC}$ as shown in Fig. B.2 then the switch to -V_{CC} at the output occurs. The capacitor has charged to $+\lambda V_{CC}$ and now will begin to discharge.

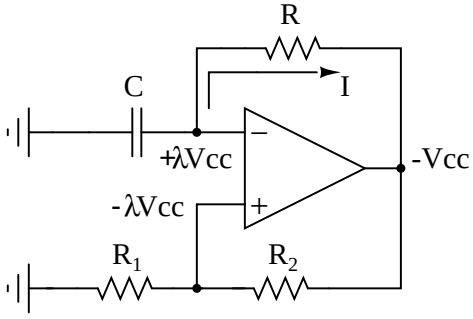


Figure B.2: Charging of the capacitor in the Oscillator

The general charging equation of a capacitor which already has an original charge is ,

$$v(t) = V_\infty(1 - e^{-t/RC}) + V_0 e^{-t/RC} \tag{B.1}$$

For this case, V_∞=-V_{CC} and V_0=+λV_{CC}. Hence,

$$v(t) = -V_{CC}(1 - e^{-t/RC}) + \lambda V_{CC} e^{-t/RC} \tag{B.2}$$

Now when the voltage across the capacitor gets to -λV_{CC} another switch will occur. This time is half the period of the square wave so it will be represented as T/2. At this time,

$$-\lambda V_{CC} = -V_{CC}(1 - e^{-T/2RC}) + \lambda V_{CC} e^{-T/2RC} \tag{B.3}$$

The above equation when solved for T gives

$$T = 2RC\ln\left[\frac{1+\lambda}{1-\lambda}\right] \tag{B.4}$$

Fig. B.3 shows the oscillator with the amplifier's offset and gain error modelled as a voltage source placed at its non-inverting terminal. Hence equation B.3 is modified as

$$-\lambda V_{CC} + V_{os\_in} = -V_{CC}(1 - e^{-T/2RC}) + (\lambda V_{CC} - V_{os\_in}) e^{-T/2RC} \tag{B.5}$$

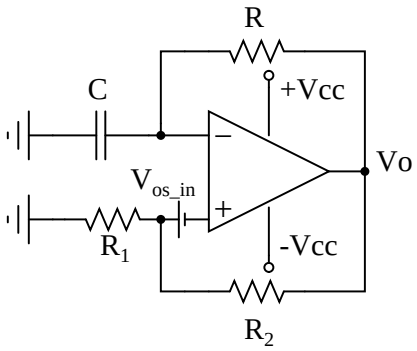


Figure B.3: Oscillator with Offset and Gain error

The time period expression becomes

$$T = 2RC\ln\left[\frac{1+\lambda-\Delta\lambda}{1-\lambda+\Delta\lambda}\right] \tag{B.6}$$

APPENDIX C

Pin Details of the Chopper Amplifier Chip

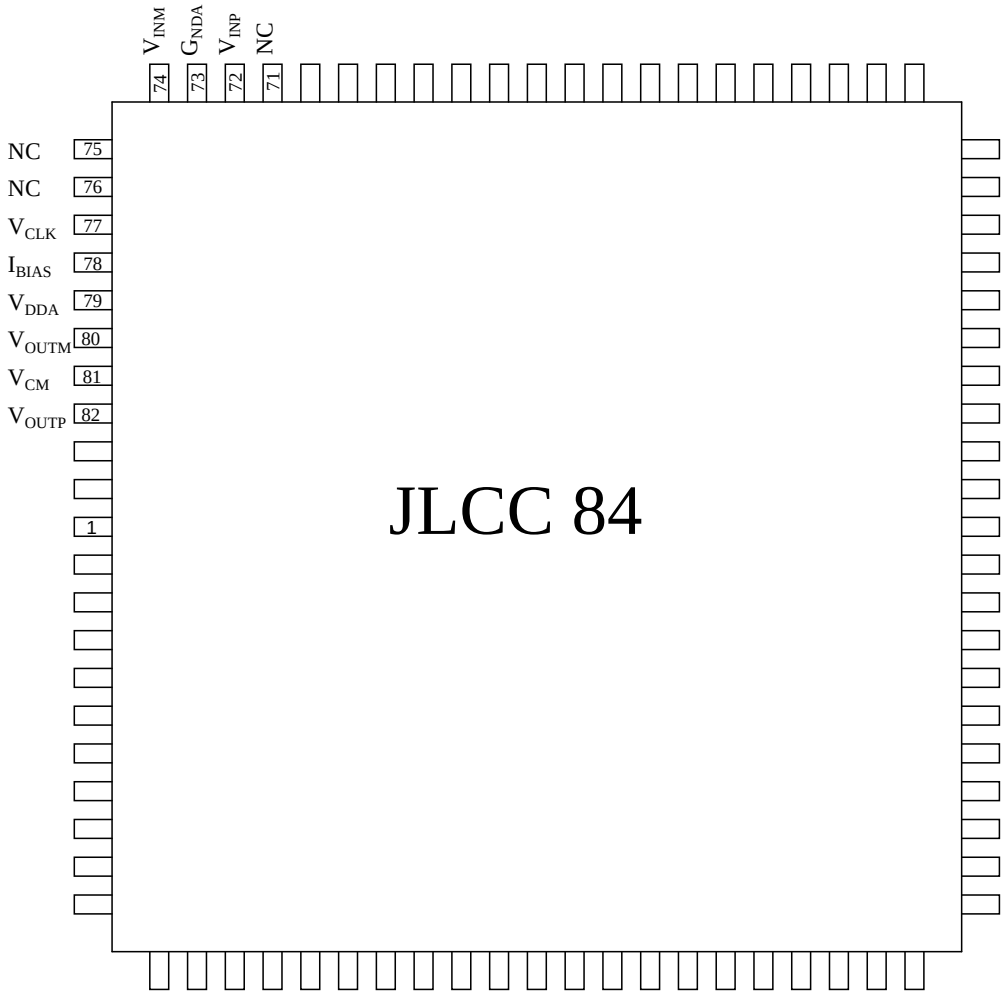


Figure C.1: Chip Pin Details

Table C.1: Functionality of pins of chopper amplifier chip

Pin Number	**Pin Name**	**Functionality**	**Value**
73	G_{NDA}	Ground Pin	
79	V_{DDA}	Supply Voltage Pin	1.8 V
81	V_{CM}	Common-mode reference voltage	0.9 V
78	I_{BIAS}	Bias current for the chopper amplifier	1 μA - 2 μA
74, 72	V_{INM}, V_{INP}	Differential Input Voltage	1 mVpp - 20 mVpp differential sine wave with V_{CM} of 1.65 V
80, 82	V_{OUTM}, V_{OUTP}	Differential Output Voltage	

APPENDIX D

Pin Details of the Thermocouple Signal Conditioner Chip

There are 4 separate blocks present in the chip. The pin details of each block is separately tabulated below.

Table D.1: Chopper Amplifier Pin Details

Pin Number	Pin Name	Functionality	Value
30	Ibias	Bias current for the chopper amplifier	1 μA - 2 μA
27	chop_clk	High frequency clock for chopping	40 kHz - 60 kHz
26	chop_nested_clk	Low frequency clock for chopping	2 kHz - 5 kHz
25	vdda_amp	Supply Voltage for the amplifier	3.3 V
24,23	vinm, vinp	Differential inputs of the chopper amplifier	1 mVpp - 40 mVpp sine wave with Vcm of 1.65 V
22, 19	gnda	Ground Voltage	0 V
20, 21	voutp, voutm	Differential outputs of the chopper amplifier	

Table D.2: CJC Buffer Pin Details

Pin Number	Pin Name	Functionality	Value
29	buf_in	Buffer Input	0.6 V - 0.8 V DC
28	buf_out	Buffer Output	1.6 V to 1.8 V

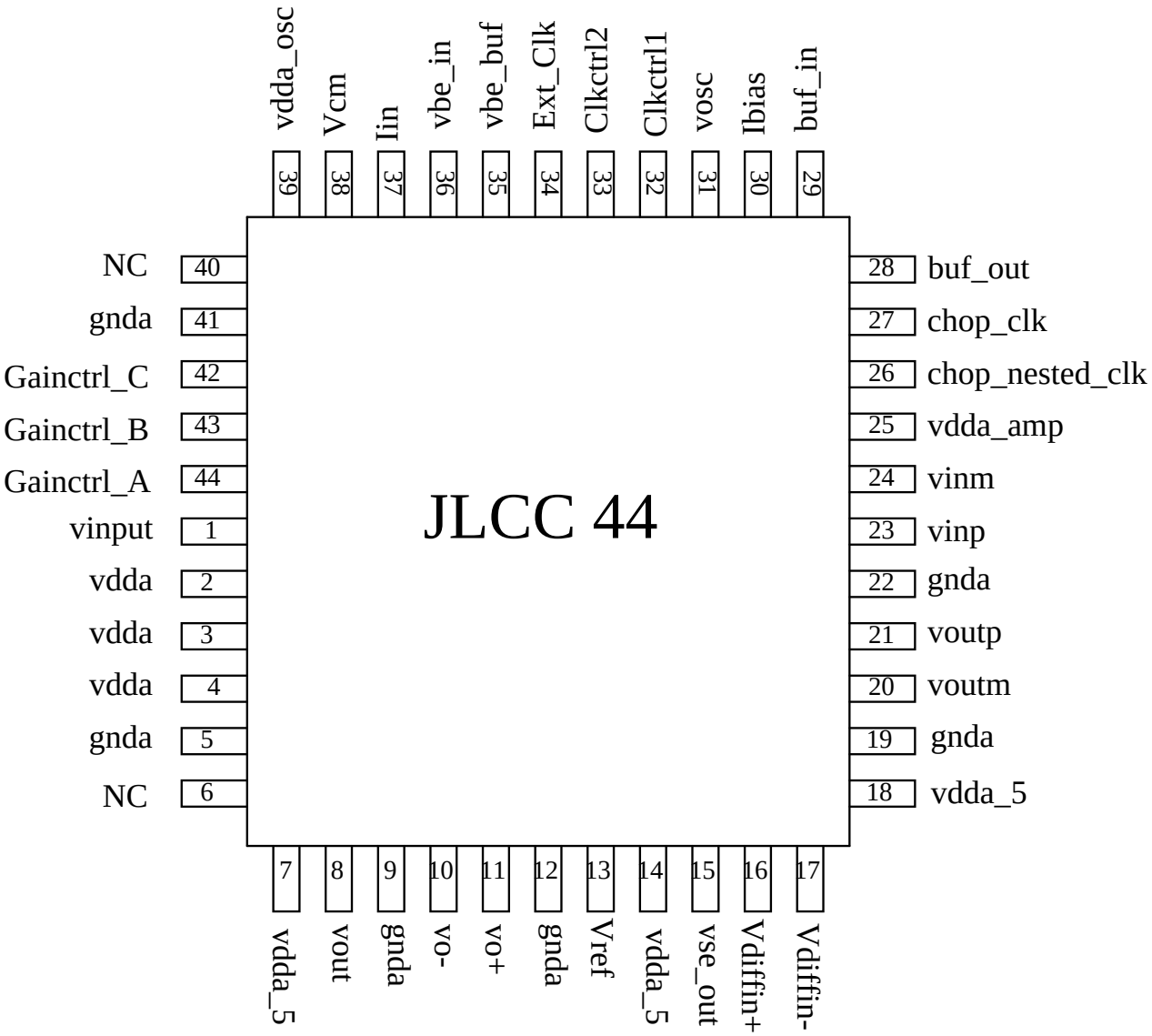

JLCC 44
1 vinput
2 vdda
3 vdda
4 vdda
5 gnda
6 NC
7 vdda_5
8 vout
9 gnda
10 vo-
11 vo+
12 gnda
13 Vref
14 vdda_5
15 vse_out
16 Vdiffin+
17 Vdiffin-
18 vdda_5
19 gnda
20 voutm
21 voutp
22 gnda
23 vinp
24 vinm
25 vdda_amp
26 chop_nested_clk
27 chop_clk
28 buf_out
29 buf_in
30 Ibias
31 vosc
32 Clkctrl1
33 Clkctrl2
34 Ext_Clk
35 vbe_buf
36 vbe_in
37 Iin
38 Vcm
39 vdda_osc
40 NC
41 gnda
42 Gainctrl_C
43 Gainctrl_B
44 Gainctrl_A

Table D.3: DE-SE Pin Details

Pin Number	Pin Name	Functionality	Value
14, 18	vdda_5	Supply Voltage	5 V
16, 17	Vdiffin+, Vdiffin-	Differential inputs	100 mV - 1 Vpp sine wave with Vcm of 1.65 V
15	vse_out	Single ended output	Outputs with Vcm of 2.5 V
13	Vref	Reference Voltage	2.5 V

Table D.4: Integrated Structure Pin Details

Pin Number	Pin Name	Functionality	Value
1	vinput	Input to the signal conditioner	40 μV - 40 mV
2, 3, 4	vdda	Supply Voltage	3.3 V
5, 9, 12,41	gnda	Ground Voltage	0 V
7	vdda_5	Supply Voltage	5 V
8	vout	Output of the signal conditioner	
10, 11	vo-, vo+	Differential outputs of the chopper amplifier present in the signal conditioner	
13	Vref	Reference Voltage	2.5 V
31	vosc	Output of the oscillator	
32, 33	Clkctrl1,Clkctrl2	Control bits to control the frequency of oscillation	
34	Ext_Clk	Clock frequency	40 kHz - 100 kHz
35	vbe_buf	CJC buffer output present in the signal conditioner	
36	vbe_in	BJT's base-emitter voltage as input to the CJC buffer	650 mV - 800 mV
37	Iin	Bias current for the signal conditioner	1 μA - 2 μA
38	Vcm	Reference voltage	1.65 V
39	vdda_osc	Supply voltage for the oscillator	3.3 V
42, 43, 44	Gainctrl_C, Gainctrl_B, Gainctrl_A	Control bits to tune the resistor bank	

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