On Pulse Position Modulation and its Application to PLLs for Spur Reduction

A THESIS

submitted by

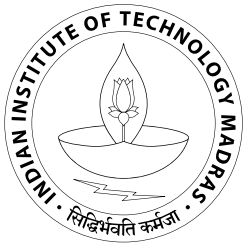
CHEMBIYAN THAMBIDURAI

for the award of the degree

of

MASTER OF SCIENCE

(by Research)



Department Of Electrical Engineering

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October 2011

CERTIFICATE

This is to certify that the thesis titled **On Pulse Position Modulation and its Application to PLLs for Spur Reduction**, submitted by **Chembiyan Thambidurai**, to the Indian Institute of Technology Madras, for the award of the degree of **Master of Science**, is a bona fide record of the work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Date: October 2011

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'Live like you are going to die tomorrow', theme of the movie *Mr.Magorium's Wonder Emporium*, inspired me as an young adult when I first watched it. I believe in searching and pursuing what you are passionate about. As someone who had interests in fields as diverse as choreography, mathematics, literature and physics, I was at crossroads many a times in life unsure of what to choose. Sometimes some decisions I made backfired, some took off well. But through all these experiences I have learnt one thing, that failures are a part of life, avoiding it is like missing a roller coaster ride. Though fearful when you are at it, a remarkable experience to remember later than the successes. After many failed attempts, I finally decided to do research in Circuit design at IIT Madras. This work would not have been possible without the factors that helped me in accomplishing it.

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Through my last two years of work at IIT Madras I owe profoundly to the empty sun heated electric trains of Chennai where many ideas struck me on my journey from home to the institute (and vice versa). Next in line are the beaches of chennai which I frequently visited. Walking on the long and lonely beach of the Triplicane in the afternoons is an experience I can never forget. I felt a connection with it, where the land and water met, I could see the logic and imagination meet in the deep thoughts on research and writing.

Man is a social being, the purpose of his creation is not to 'live and die' but to experience it, share some of its wonderful moments with his fellow men. I m infinitely blessed to have a very few but lifelong friends. First I would like to thank Kiran. We have been friends through the merrier and difficult times, helping each other when we were met with failures. The long trips we had as childhood friends climbing tall mountains and catching fishes in ponds, to the recent frequent trips (12 years later) we had to the 'pizza hut and sanjeevanam' and him putting up with my obsessions of being choosy about food are the experiences I can never forget. I hope he finds the 'girl of his dreams' that he keeps trying and failing at many times.

Good friends stay with us when in times of need. There cannot be a better example than my friends from BITS-Pilani kana (karthik) and state (Srinivasa raghavan), in my case. Without them I would have missed something in life. Each of them well accomplished (kana a Stanford grad, state a cricket player and an 'IBM stalwart') by themselves are people with good hearts. Through all the difficult times, they have kept my spirits up by emails and chats. The treats we had in the biting cold winters at Connaught place where kana ate his favorite mix veg oothappam and state devoured 'anything' that came his way, where we discussed each of our dreams and my dreams of studying at Berkeley are experiences we often recollect to tear filled eyes.

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Finally, my special thanks to my parents who put up with all my idiosyncrasies and patiently waiting for me complete my degree even when they needed my financial assistance. I would like to dedicate this thesis to all the independent minds who produced truly independent work and whose legacy has enabled the sustenance of such a race in this otherwise boring world.

ABSTRACT

Phase lock loops (PLLs) are used in frequency synthesis for modulation and demodulation of base band data in wireless communications and to generate clocks for accurate timing in digital systems like microprocessors. One class of PLLs called the charge pump PLLs has gained wide popularity due to its relative ease of implementation. However due to the discrete time nature of the phase frequency detector and nonidealities in the charge pump, a periodic charge pump current is injected into system in the steady state. This results in spurs in the output spectrum of the PLL. The bandwidth of the PLL is reduced to have low spur levels. A lower PLL bandwidth increases the settling time of the PLL and reduces the frequency range of rejection of the VCO phase noise.

The central idea of this work is to break the periodicity and convert the energy in the spurs into a wideband noise, which enables the PLL to have larger bandwidth and maintain low spur levels. Randomizing the positions of charge pump current pulses in a PLL breaks their periodicity and redistributes the reference spurs into broadband noise. In this work closed form expressions for the spectrum of pulse position modulated (PPM) signals are derived and intuitive explanations for the results are given. The redistributed noise has a highpass shape and does not affect the close in phase noise of the PLL. PPM using a uniformly distributed uncorrelated sequence completely removes the spurs and provides a first order shaping of redistributed noise. Higher order shaping and reduction of redistributed noise at intermediate offset frequencies are possible using PPM with a correlated modulating sequence and pulse repetition. Circuit implementations of these techniques are given and their nonidealities are discussed. The implementation ideas proposed in this work leads to a compact implementation of the techniques and is more

insensitive to delay mismatch. A detailed analysis of the delay line nonidealities is also presented to study their effect on the PLL output phase noise.

Simulation results confirm the results of the analysis and viability of the proposed techniques. In the presence of nonidealities spurs can be reduced by at least 13 dB without any trimming of the delays in the PPM circuits and by 25 dB after trimming the delays within 5% of the nominal value.

A 1 GHz PLL operating from a reference frequency of 20 MHz and a bandwidth of 1 MHz is implemented in 0.18 μm CMOS technology to test the proposed ideas. The spur at -20 MHz offset from the carrier (980 MHz) was measured to be 64 dBc. Enabling the PPM and PR reduces the magnitude of the spur by 8 dB and 9 dB respectively.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABBREVIATIONS

PLL	Phase Lock Loop
CMRR	Common Mode Rejection Ratio
CT	Continuous Time
UGB	Unity Gain Bandwidth
DSM	$\Delta\Sigma$ Modulator
DT	Discrete Time
NTF	Noise Transfer Function
PSD	Power Spectral Density
PPM	Pulse Position Modulation
PPAM	Pulse Position and Amplitude Modulation
PR	Pulse Repetition
SPPM	Shaped Pulse Position Modulation

CHAPTER 1

Introduction

1.1 Charge pump PLL basics

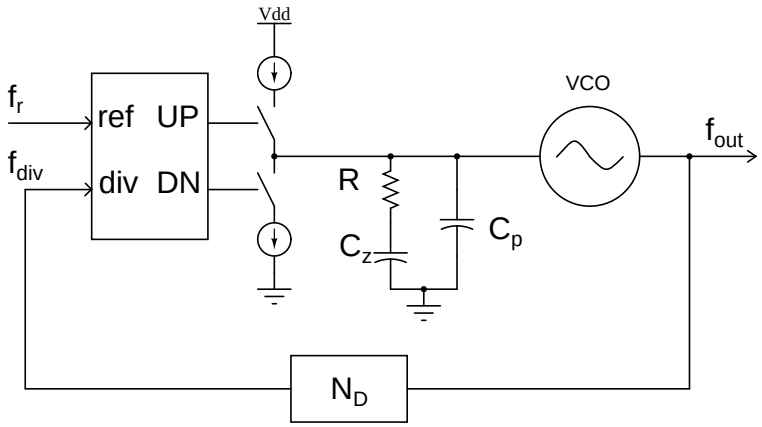

Figure 1.1: Standard charge pump PLL architecture.

Charge pump PLLs are widely used for frequency synthesis in transceivers and clock generation in microprocessors. A large body of work can be found in the literature that deals with the analysis of charge pump PLLs [1], [2], [3]. So a brief introduction of its details is presented in this chapter.

The widely used architecture of a charge pump PLL is shown in Fig. 1.5. A PLL is a feedback system that forces the output signal frequency (phase) to track the input frequency (phase) or a multiple of the input frequency. It consists of a phase frequency detector (PFD) that measures the phase error between the input reference clock and the feedback (divide) clock. The PFD produces two digital signals called UP and DN, which are converted into current pulses (whose pulse widths are proportional to the phase error) by the charge pump. The current pulses are fed into the loop filter generating a voltage that is a linear function of the phase

error. The generated voltage is used to control the frequency of the voltage controlled oscillator (VCO). The PFD, charge pump and the loop filter convert the phase-error information to control voltage of the VCO. In the steady state the net output of the charge pump current is zero and the divided output frequency equals the input frequency.

1.1.1 Discrete-time behaviour of the PLL

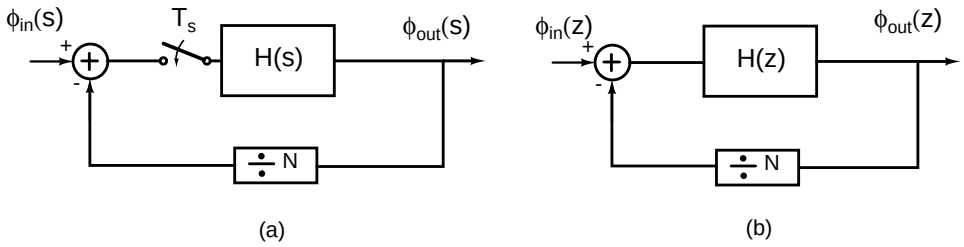

Figure 1.2: (a) Continuous-time PLL model, (b)Discrete-time PLL model.

The PFD measures the phase error every reference cycle and the charge pump outputs current pulses proportional to the phase error. Close to the steady state, the phase error between the reference and divide signals is much smaller than 2π. That is when the time difference between the rising edges of the reference and divide signals is much smaller compared to the reference clock period T and the charge pump outputs very narrow current pulses. The narrow current pulses occurring every reference period can be modeled as impulses with amplitudes equal to area under the pulses (the phase error). Thus the PFD and the charge pump behaviour can be modeled as a discrete time system, sampled at the input reference frequency $f_r = 1/T$ [2]. But the loop filter and the VCO operate in a continuous time fashion. This hybrid nature of the PLL makes it hard to analyze the system. However when the bandwidth of the PLL is much smaller than the reference frequency one can conveniently represent the PLL as a linear continuous-time system.

Due to the discrete nature of the PFD and charge pump, it is more accurate

to analyze the PLL as a sampled data system with the phase errors sampled at $f_r = 1/T$ [2]. The discrete time model of the PLL will reveal if there are any instability problems due to the sampling delay incurred by the discrete nature of the PFD that may not be seen in a continuous-time model [1]. As shown in Fig. 1.2

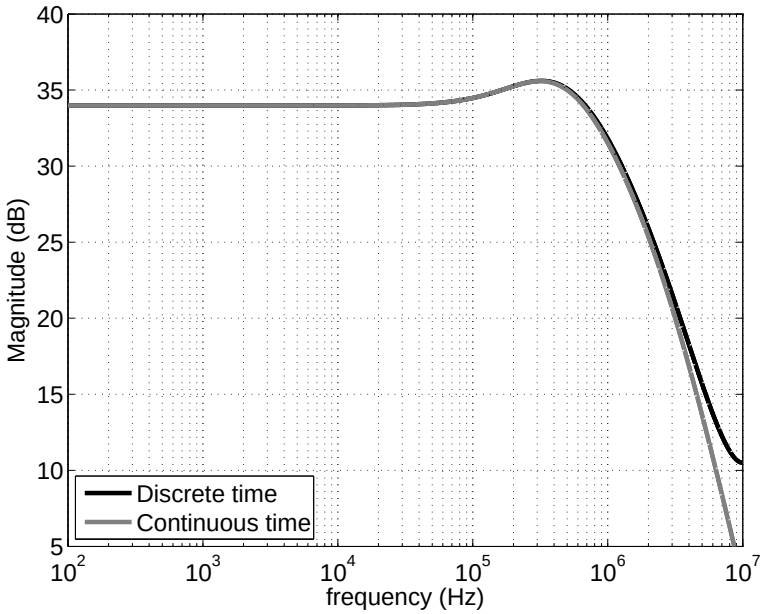

Figure 1.3: Closed-loop PLL magnitude response from the continuous and discrete time models.

the continuous-time model can be transformed into its sampled equivalent by replacing the open loop continuous time filter $H(s)$ with the sampled equivalent $H(z)$ using an impulse invariance transformation. Fig. 1.3 shows the magnitude response of the PLL obtained from the discrete model overlaid with the response of the continuous time linear model. The two responses are identical over most of the frequency range except for a small peaking of 0.2 dB in the discrete-time model near the 3 dB bandwidth of the PLL. Hence the continuous time approximation can be used without any additional stability concerns for bandwidths smaller than $f_r/10$.

To see how the settling behaviour of the actual PLL is approximated by the continuous-time linear model, we simulated the PLL behaviourally and then used a continuous-time model to compare the time domain responses to a small step in the frequency. Fig. 1.4 shows the LTI response overlaid with the actual step

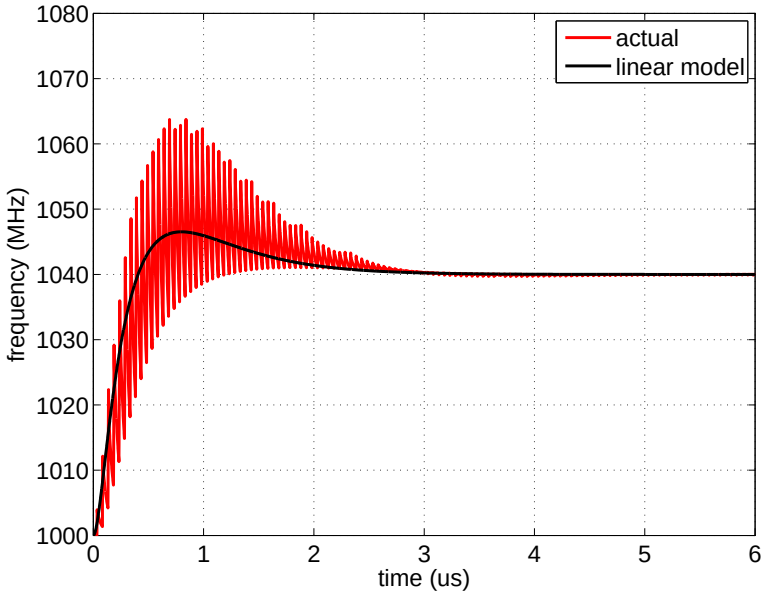

Figure 1.4: Response of the control voltage to a frequency step. The response of an actual PLL matches the response obtained from a linear model in an average sense.

response of the PLL for a certain step in the frequency. The PLLs step response matches the linear model in an average sense. Hence it is common to use LTI analysis to characterize the PLL loop dynamics.

1.1.2 Continuous time model of the PLL

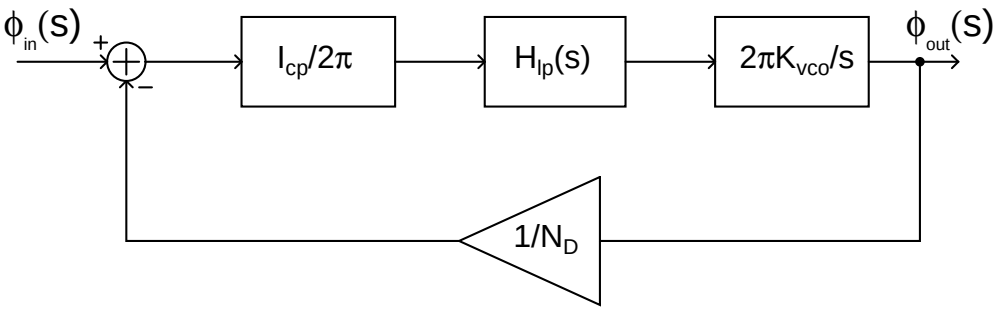

Figure 1.5: Linear model of the PLL.

The input of the system is the reference phase $\phi_{in}(s)$ and the output of the system is the phase of the VCO output $\phi_{out}(s)$. The open loop transfer function $H(s)$ of

the linear phase domain model of the PLL is given by

$$H(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{I_{cp}K_{vco}}{(C_z + C_p)N_D}\left(\frac{1}{s^2} + \frac{RC_z}{s}\right)\frac{1}{(1 + \frac{s}{\omega_p})} \tag{1.1}$$

where I_{cp} is the charge pump current, K_{vco} is the VCO gain in Hz/V, N_D is the divide value and $\omega_p = 1/(RC_z||C_p)$.

The unity gain bandwidth (UGB) of the PLL is given by

$$\omega_u \approx \frac{I_{cp}K_{vco}R}{N_D} \tag{1.2}$$

Table 3.1 shows the parameters of the example[1] PLL used to demonstrate the

Table 1.1: PLL parameters.

	Parameters
Input frequency	20 MHz
PFD	Tri-state PFD
Charge pump current	$I_{cp} = 56\,\mu$A
Loop filter	R = 21.7 kΩ, C_z = 37.25 pF, C_p = 1.99 pF
VCO	$f_{vco} = 1$ GHz, $K_{vco} = 300$ MHz/V
Divider	$N_D = 50$
unity gain bandwidth	$f_u = 1$ MHz
closed-loop 3dB bandwidth	$f_{3dB} = 1.9$ MHz
Phase margin	PM= 52.55^0

operation and problems associated with the charge pump PLLs.

1.2 Problem of reference spurs

A major drawback of the charge pump PLL is the presence of reference spur in the output spectrum. In the steady state of a charge pump PLL, the reference and divide edges are aligned by the feedback action of the PLL. The phase error is zero and thus the output of the PLL does not have any spur at the reference frequency.

[1]The same specifications given in the example is used for the PLL designed in this work.

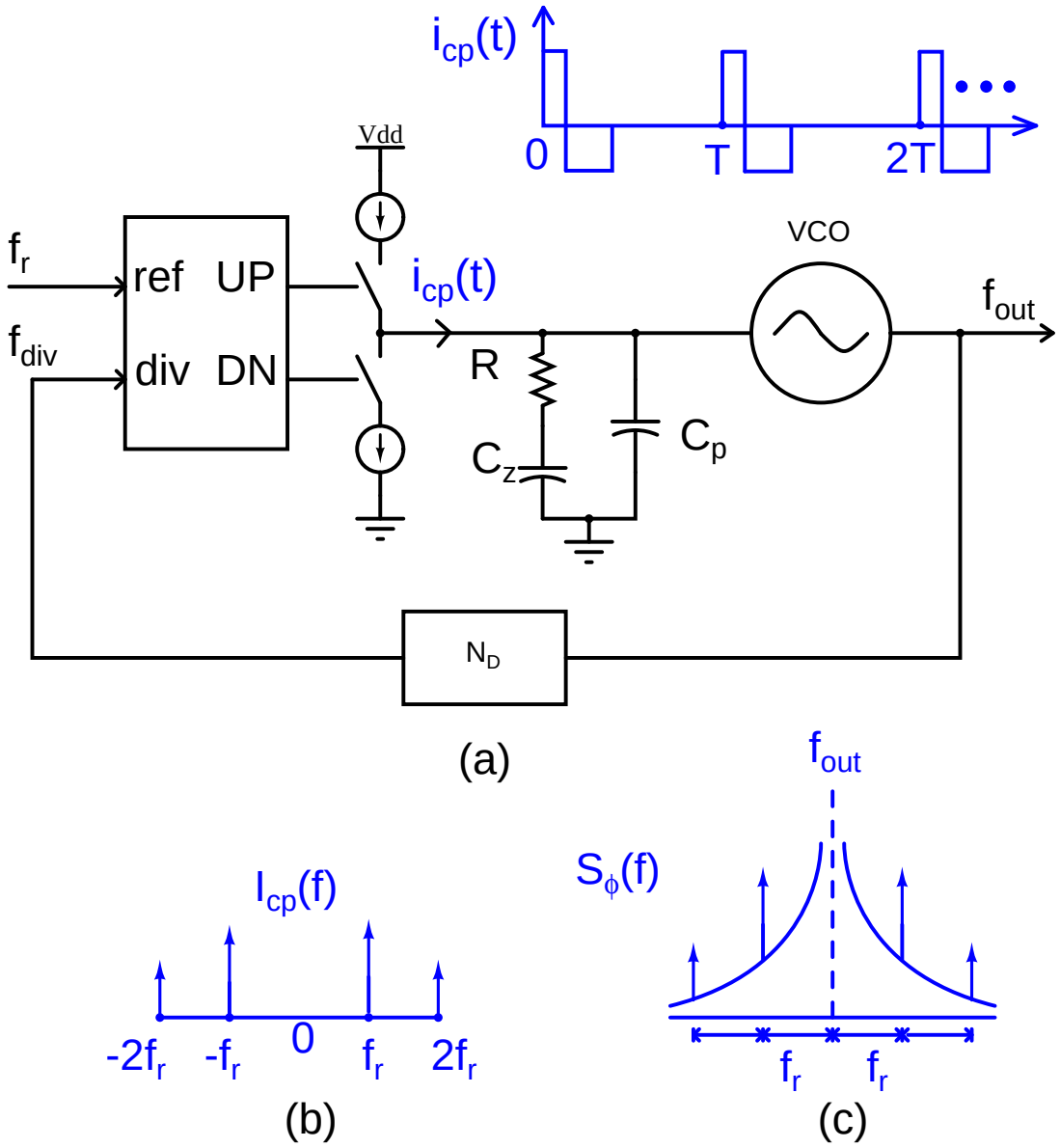

Figure 1.6: (a) Standard charge pump PLL architecture showing the periodic nature of the charge pump current, (b) the spectrum of the steady state charge pump current and (c) the PLL output spectrum showing the up conversion of the charge pump spurs.

However in the presence of nonidealities in the PFD and charge pump, a periodic non-zero error current with zero average value flows into the loop filter as shown in Fig. 1.6. This results in a periodic disturbance of the control voltage, which frequency modulates the VCO and results in a spurs at the reference frequency and its harmonics[2].

The nonidealities in the PFD, charge pump and loop filter that cause reference

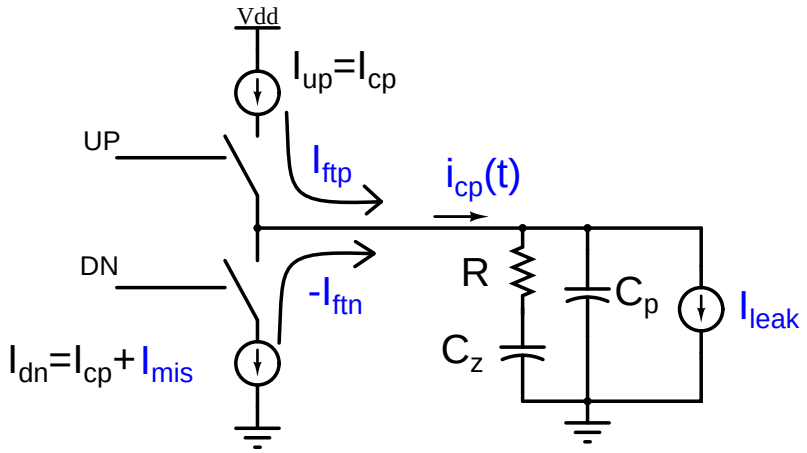

Figure 1.7: Charge pump nonidealities

spurs are

- mismatch in the UP and DN signal paths of the PFD
- mismatch in the UP and DN currents of the charge pump
- feed through of the charge pump switches
- leakage current in the loop filter capacitors

The charge pump current injected into the loop filter every reference cycle (T) is a pair of impulses (narrow triangular pulses) spaced reset delay (T_{rst}) apart in the presence of the feed through (I_{ft}) of charge pump switches and a pulse in presence of charge pump current mismatch (I_{mis}) or loop filter leakage (I_{leak}). The illustrative pulse shapes of the charge pump current are shown in the Fig. 1.8(a), 1.8(b) and 1.8(c) respectively. This non-zero periodic current generates a periodic

[2]In time domain this appears as jitter in the output and in frequency domain as discrete components at integer multiples of reference frequency away from the output frequency.

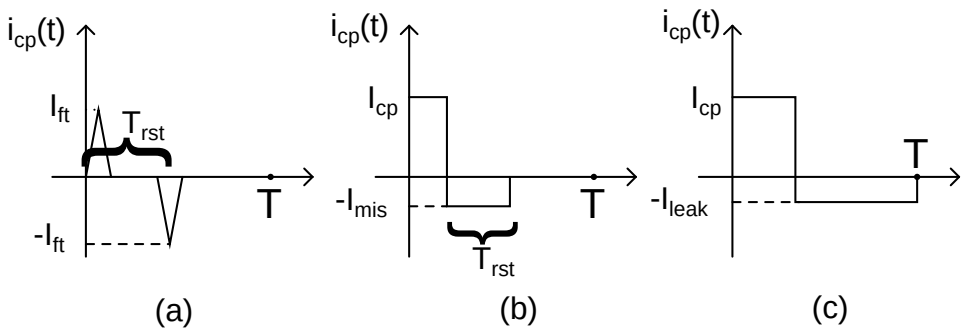

Figure 1.8: Illustrative pulse shapes of the charge pump current injected into the loop filter every reference cycle in steady state

disturbance on the control voltage and manifests itself as a reference spur at the PLL output. The magnitude of the spur at a frequency offset f_r from the carrier

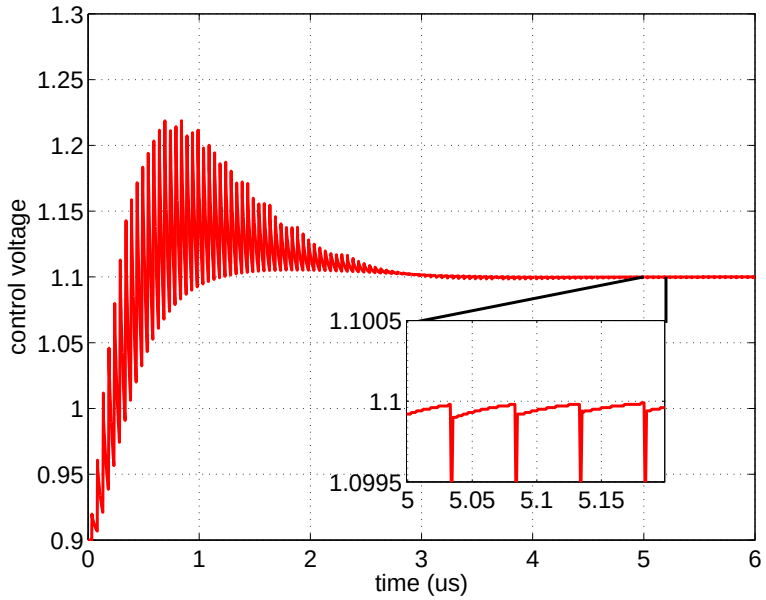

Figure 1.9: Periodic disturbance on the control voltage in steady state

at the PLL output can be expressed in dBc as [4]

$$S_\phi(f) = 10 \log \left(S_{cp}(f) \left| \frac{Z(f)\, K_{vco}}{f} \right|^2 \right) \tag{1.3}$$

Where $S_{cp}(f)$ is the spectral density of $i_{cp}(t)$. When $i_{cp}(t)$ is periodic at f_r, $S_{cp}(f)$ (and hence $S_\phi(f)$) consists of impulses, or spurs, at integer multiples of f_r. A PLL was simulated with the PFD and charge pump at schematic level and the remaining blocks at behavioural level. Fig. 1.9 shows the periodic disturbance on the control voltage once the PLL has settled. Fig. 1.10 shows the phase noise of

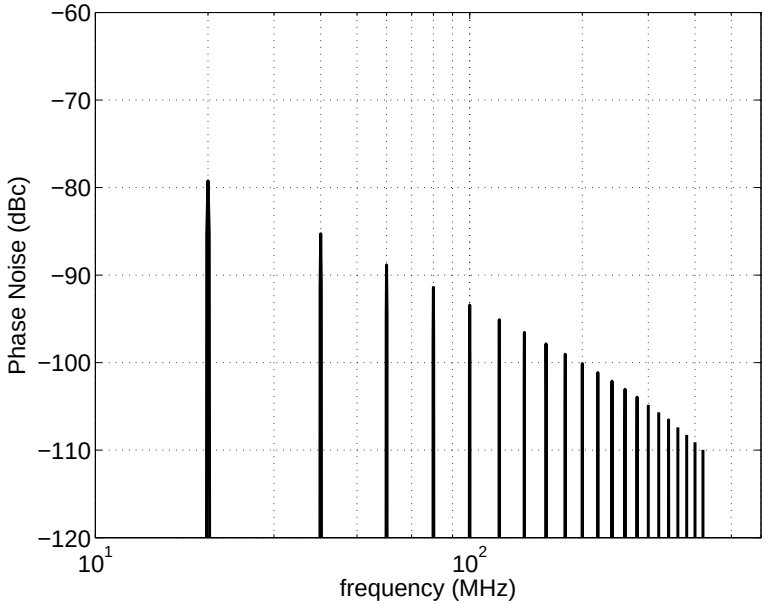

Figure 1.10: Spurs at PLL output at harmonics of reference frequency offset from the carrier.

the PLL output in the presence of the periodic disturbances on the control voltage. The presence of reference spurs at multiples of the reference frequency (20 MHz in the above example) can be clearly seen from the figure.

Eq. (1.3) implies that a low spur level at the output is achieved by having a low VCO gain (K_{vco}) or a low loop filter impedance ($Z(f_r)$). But reducing these two parameters reduces the bandwidth of the PLL, leading to longer settling time and lower noise filtering of the VCO. Therefore, there is a trade-off between settling time and tolerable reference spur levels.

Several techniques have been proposed to minimize the spurs while maintaining a higher bandwidth. [5] addresses the issue based on the technique of delay-sampling the control voltage. This converts the periodic disturbances to dc, but it is not effective in the presence of loop filter capacitor leakage. [6] minimizes the charge pump mismatch thereby reducing the spur, at the cost of increased settling time. [7] uses distributed charge pump and PFD with pulse position randomization to reduce the spur. Using distributed PFD and charge pumps can cause the total size of the charge pump switches to be larger, increasing the net feed through error besides increasing the implementation complexity.

The central work of the thesis is to eliminate the spurs by spreading the energy present in the spurs to all frequencies. To accomplish this, the charge pump current pulse positions are modulated within a single reference period by modulating the pulse positions of the UP and DN pulses as shown in Fig. 1.11. Random positioning

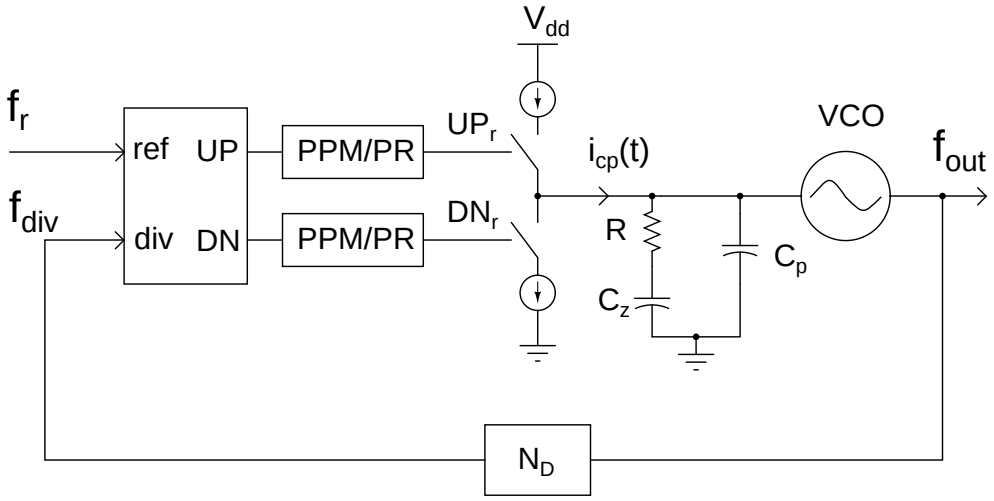

Figure 1.11: The modified PLL architecture with pulse position modulator/pulse repeater shown at block level.

of the charge pump current pulses $i_{cp}(t)$ within the reference period T ([7],[8]), in other words, pulse position modulation (PPM) by a random sequence, breaks the periodicity and distributes the energy in the reference spurs into wideband phase noise. In order to quantify this effect, the spectral density of the charge pump current ($S_{cp}(f)$ in Eq. 1.3) after applying the random PPM has to be determined. In this work, we present a general analysis of pulse trains whose amplitude and pulse positions are modulated by independent stationary sequences with arbitrary probability distributions and give closed form expressions for the spectral density. This analysis is simpler and more intuitively understood compared to previously published results [9]. We also analyze the effects of pulse repetition (PR) within a reference period [7], and a combination of PPM and PR.

The proposed spur reduction techniques can be implemented in a more compact manner compared to previously published ones because they involve delaying UP and DN signals which control $i_{cp}(t)$ by random amounts, which can be accomplished using digital delay lines and a MUX controlled by a random sequence [8].

A similar approach also results in a simpler implementation of PR compared to [7]. The proposed implementation is less sensitive to delay line mismatch than when the delay lines are placed before the PFD [7]. Unlike the latter, it requires delaying narrow pulses with a minimum width equal to the reset delay of the PFD. Design trade offs due to these constraints are analyzed. Modifications to the implementation are suggested for cases when the reset delay is very small.

1.3 Overview of the thesis

The rest of the thesis is organized as follows

- Chapter 2 discusses the spectral analysis of PPM signals and ways to reduce reference spurs at a system level. The performance of the proposed techniques in the presence if delay line nonidealities is also discussed in detail.
- Chapter 3 explains the details of the circuits of the implemented PLL.
- Chapter 4 explains the implementation details of the supply regulated PLL used for delay tuning.
- Chapter 5 shows the circuit level simulation results of the PLL.
- Chapter 6 presents the measured results taken from an actual silicon implementation.
- Chapter 7 concludes the thesis and suggests future work to be carrier out.
- Appendix A discusses the unified spectral analysis of digitally modulated signals in the presence of nonidealities.
- Appendix B discusses the basics of linear and non-linear ring oscillators.
- Appendix C discusses the asymmetric sidebands in the presence of both AM and FM.

CHAPTER 2

Spur Reduction Techniques

2.1 Introduction

As discussed in the previous chapter, the periodicity in the steady state charge pump current is the cause of the spurs at the output. The central idea of this work is to break the periodicity in the charge pump current pulses by applying pulse position modulation based techniques. In theory this randomizing effect redistributes the energy of the current pulses concentrated at the harmonics of reference frequency to all the frequencies making it appear as wideband noise. The resulting "redistributed noise" is further filtered by the loop-filter and the VCO. Ideally this approach can eliminate spurs completely. To quantify the effects of the redistributed noise on the PLL output phase noise, spectra of different pulse position modulation schemes are analyzed and optimum schemes are derived to tackle the reference spurs based on the analysis.

2.2 Mathematical formulation

Let x_k and a_k be two stationary sequences. Then

$$x_p(t) = \sum_{k=-\infty}^{\infty} x_k \delta(t - kT) \tag{2.1}$$

is a pulse amplitude modulated (PAM) signal [10] of period T, and

$$r_p(t) = \sum_{k=-\infty}^{\infty} x_k \delta(t - kT - a_k T_d) \tag{2.2}$$

is a pulse position and amplitude modulated (PPAM) signal whose pulse positions $a_k T_d$ are modulated by the sequence $a_k \in [0,\ N-1]$ and pulse amplitudes are modulated by x_k. The pulse shape $p(t)$ is assumed to be an impulse for simplicity of expressions. Fig. 2.1 illustrates PAM and PPAM signals for $N = 8$ and $T_d = T/N$. The signals $x_p(t)$ and $r_p(t)$ are cyclostationary random processes [10] when the

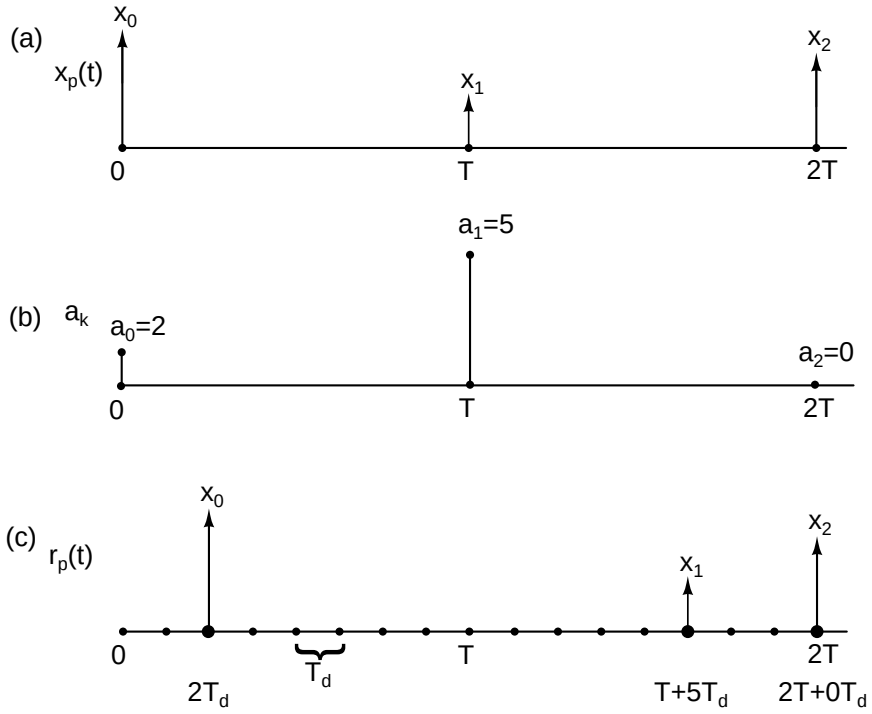

Figure 2.1: (a) PAM with sequence x_k, (b) Pulse position modulating sequence a_k, (c) PPAM with sequences a_k and x_k for $N = 8$.

modulating sequences x_k and a_k are stationary. The power spectral density (PSD) $S_{xp}(f)$ of the PAM signal in Eq. (2.1) is given by [10]

$$S_{xp}(f) = \frac{1}{T} S_x(f) \tag{2.3}$$

where $S_x(f)$ is the PSD of the stationary sequence x_k (with an autocorrelation function $R_x(k)$) given by $S_x(f) = \sum_k R_x(k) e^{-j2\pi fkT}$. If the samples of the sequence a_k are iid, the PSD $S_{rp}(f)$ of PPAM signal is given by (Appendix A.1)

$$S_{rp}(f) = \frac{1}{T} S_x(f)|C(f)|^2 + \frac{R_x(0)}{T}[1 - |C(f)|^2] \tag{2.4}$$

where

$$C(f) = \sum_{m=0}^{N-1} P_A(a = m) e^{-j2\pi f m T_d} \tag{2.5}$$

$P_A(a)$ is the probability mass function of the sequence a_k. $C(f)$ is what we call the "Pseudo filter[1]". It is the characteristic function [10] of the modulating sequence's probability mass function. For any arbitrary pulse shape $p(t)$, the PSD of the PAM and PPAM signals is obtained by multiplying the above expressions by $|P(f)|^2$, where $P(f)$ is the Fourier transform of the pulse $p(t)$. When $p(t)$ represents the charge pump current, the pulses are much narrower than the reference period T and have an average value of zero.

2.2.1 Power lost and power redistributed

The spectrum of the PPAM signal can be written as

$$S_{rp}(f) = \underbrace{\frac{S_x(f)}{T}|C(f)|^2}_{\text{Power filtered}} + \underbrace{\frac{R_x(0)}{T}[1 - |C(f)|^2]}_{\text{Power redistributed}} \tag{2.6}$$

Eq. (2.6) shows that the PPAM is equivalent to passing the PAM signal (with a PSD $S_x(f)/T$) through a filter $C(f)$ and adding a component that corresponds to redistributing the power that is filtered out (lost) as continuous wideband noise. The characteristics of the filter and the noise are completely determined by the probability distribution of the randomizing sequence a_k. Since $P_A(a = m)$ is positive for all m and $\sum_m P_A(a = m) = 1$, $C(f)$ is a lowpass filter with unity dc gain and the redistributed power has a highpass shape.

One can intuitively see that, on an average over a large number of clock cycles, the samples of $x_p(t)$ would have occupied the positions mT_d within the single interval T, with weights $P_A(a = m)$. A scaled summation of the delayed versions of the signal $x_p(t)$ is nothing but lowpass filtering of the signal.

[1]Since it is not an actual filter.

2.3 PPM by an uniformly distributed iid sequence

Let $x_i(t)$ be a periodic impulse train of period T, $x_i(t) = \sum_k \delta(t - kT)$. $x_i(t)$ is a PAM signal with x_k always equal to 1, hence $R_x(k) = 1$. Using Eq. (2.3), the PSD $S_{xi}(f)$ of $x_i(t)$ is given by

$$S_{xi}(f) = \frac{1}{T} \sum_k e^{-j2\pi fkT} = \frac{1}{T^2} \sum_k \delta(f - kf_r) \tag{2.7}$$

By virtue of its periodicity, the power of the signal is concentrated only at the harmonics of the fundamental frequency ($f_r = 1/T$). Let a_k be of uniform distribution $\in [0, N-1]$ and $T_d = T/N$. Using Eq. (2.4), the PSD $S_r(f)$ of the resulting N-PPM (N represents the number of pulse positions of the PPM signal) signal $r(t)$ can be computed to be

$$S_r(f) = \frac{1}{T^2} \sum_{k=-\infty}^{\infty} \delta(f - kf_r)|C_N(f)|^2 + \frac{1}{T}\left[1 - |C_N(f)|^2\right] \tag{2.8}$$

Since $P(a_k) = 1/N$, the squared magnitude of the associated pseudo filter $C_N(f)$ from Eq. (2.5) is given by

$$|C_N(f)|^2 = \left| \frac{1}{N} \sum_{l=0}^{N-1} e^{-j2\pi flT/N} \right|^2 = \left(\frac{\sin(\pi fT)}{N \sin(\pi fT/N)} \right)^2 \tag{2.9}$$

$C_N(f)$ is a moving average filter of length N with nulls at kf_r where $k \in ([1, N-1], [N+1, 2N-1], \cdots)$. Thus the spectrum of N-PPM reduces to

$$S_r(f) = \frac{1}{T^2} \sum_{k=-\infty}^{\infty} \delta(f - kNf_r) + \frac{1}{T}\left[1 - |C_N(f)|^2\right] \tag{2.10}$$

Comparing Eq. (2.10) to Eq. (2.7) we can see that the N-PPM signal contains spurs at the harmonics of Nf_r and the harmonics in $[f_r, (N-1)f_r]$ are absent.

The second term in Eq. (2.10) is the 'redistributed noise' $S_{sn}(f)$

$$S_{sn}(f) = \frac{1}{T}\left[1 - |C_N(f)|^2\right] \tag{2.11}$$

The power lost P_{lost} (power in the absent spurs) in the frequency band $[0, Nf_r]$ is

$$P_{lost} = \int_0^{Nf_r} \frac{1}{T^2} \sum_{k=1}^{N-1} \delta(f - kf_r)\, df = \frac{(N-1)}{T^2}$$

The power redistributed P_{sn} in the same band is

$$P_{sn} = \int_0^{Nf_r} S_{sn}(f)\, df = \int_0^{Nf_r} \frac{1}{T}\left[1 - |C_N(f)|^2\right] df = \frac{(N-1)}{T^2}$$

Thus power filtered out P_{lost} is equal to the power redistributed P_{sn}. Randomizing the impulse positions by a uniformly distributed sequence a_k is equivalent to passing it through a moving average filter and the harmonics in the interval $[f_r, (N-1)f_r]$ are eliminated and spread as 'redistributed noise' $S_{sn}(f)$. As $N \to \infty$, all the harmonics of f_r are eliminated and converted to noise. The pseudo filter in the limiting case can be shown to be a sinc filter[2] $|C_\infty(f)| = |\text{sinc}(fT)| = |\sin(\pi fT)/\pi fT|$ and the spectrum of the ∞-PPM signal is given by

$$S_r(f) = \frac{1}{T}\left(1 - \left|\frac{\sin(\pi fT)}{\pi fT}\right|^2\right)$$

Fig. 2.2 shows the simulated spectrum of the periodic signal and an 8-PPM signal. From the figure we can see that the harmonics in $[f_r, 7f_r]$ are absent and spread as noise. The simulated spectral density is coincident with the shape of redistributed noise given by Eq. (2.10). To show the filtering nature of the PPM, Fig. 2.3 shows the spectrum of the 8-PPM signal overlaid with the associated Pseudo filter. We can clearly see the absence of harmonics occurring at the zeroes of the Pseudo

[2]This might seem intuitively correct as we can see that the impulse response of pseudo filter is the pmf of a_k with the samples spaced T/N seconds apart. As N increases the samples come closer and eventually become a continuous pulse of width T and magnitude $1/T$ (as the impulse response is now a continuous probability distribution). The Fourier transform of a pulse is the 'sinc' function.

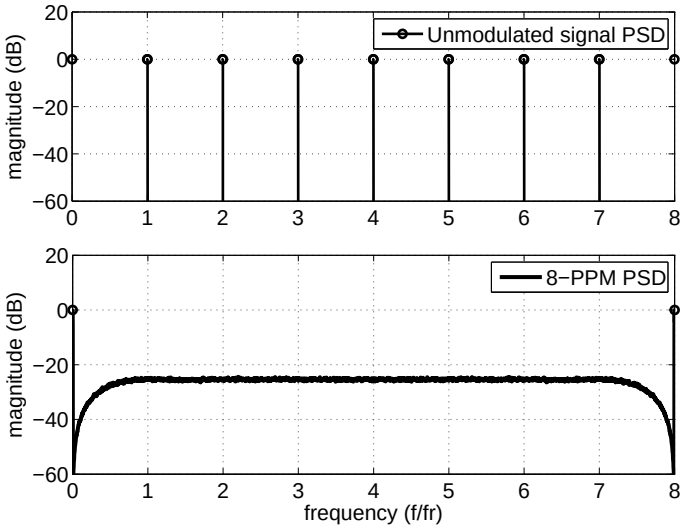

Figure 2.2: The spectrum of the unmodulated impulse train and the spectrum of the 8-PPM signal (PSD computed with a resolution bin width of $f_r/512$).

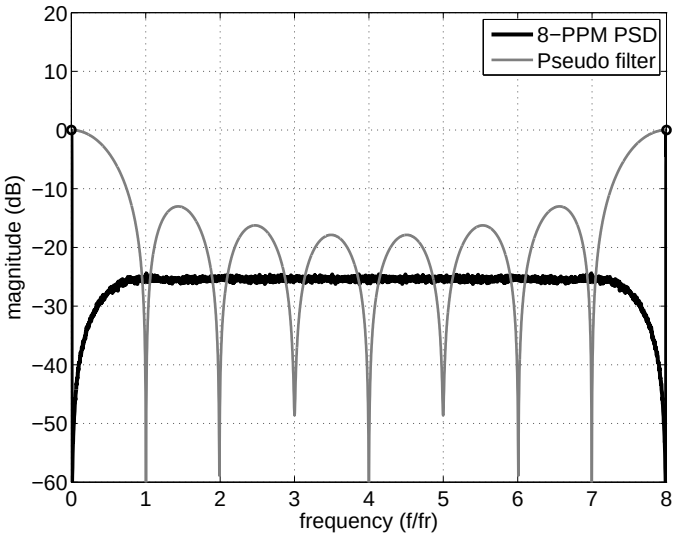

Figure 2.3: The spectrum of the PPM signal modulated by a uniformly distributed sequence overlaid with the associated pseudo filter for $N = 8$ (PSD computed with a resolution bin width of $f_r/512$).

filter.

2.3.1 Shape of the redistributed noise

$C_N(f)$ is a moving average lowpass filter. A moving average filter is a first order shaped low pass filter and hence the redistributed noise has a first order high pass characteristic. We can easily verify that for $(N = 2)$, $S_{sn}(f) = (1/T)\cdot\sin^2(\pi fT/2)$, which is a first order highpass filter. Thus the PPM technique when applied to a PLL does not affect the close-in phase noise or long term jitter of the PLL. Fig. 2.4 shows the redistributed noise on a log scale for different values of N. The shape is similar at low frequencies independent of the value of N.

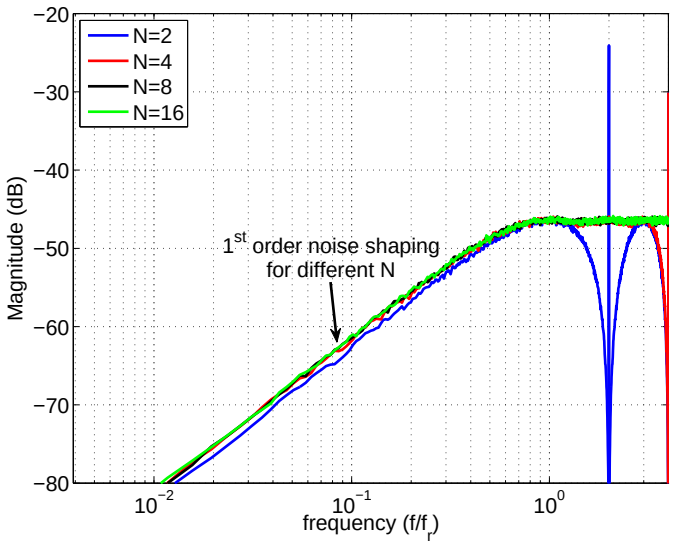

Figure 2.4: Redistributed noise for different values of N (shown in a log scale for better comparison).

2.3.2 Sensitivity to delay variations

The analysis above revealed that increasing N does not increase the noise shaping at low frequencies but eliminates reference spurs up to Nf_r. But increasing N increases the implementation complexity of the PLL with randomization. Usually eliminating the spurs from the first few harmonics of reference frequency is suffi-

cient as the spurs far away are well rejected by the lowpass characteristic of the PLL loop filter itself. So in order to choose N, we consider the sensitivity to delay variations as a measure of performance.

The charge pump current pulses are pulse position modulated by modulating the UP/DN pulse positions[3]. The delays T_d in the implementation of PPM are realized using inverters and are thus prone to systematic variations due to process and temperature. In that case $T_d \neq T/N$ and the pseudo filter is given by

$$|C_N(f)|^2 = \left(\frac{\sin(N\pi f T_d)}{N\sin(\pi f T_d)}\right)^2 \tag{2.12}$$

From Eq. (2.12) we can see that the filtering action introduces zeroes at frequencies

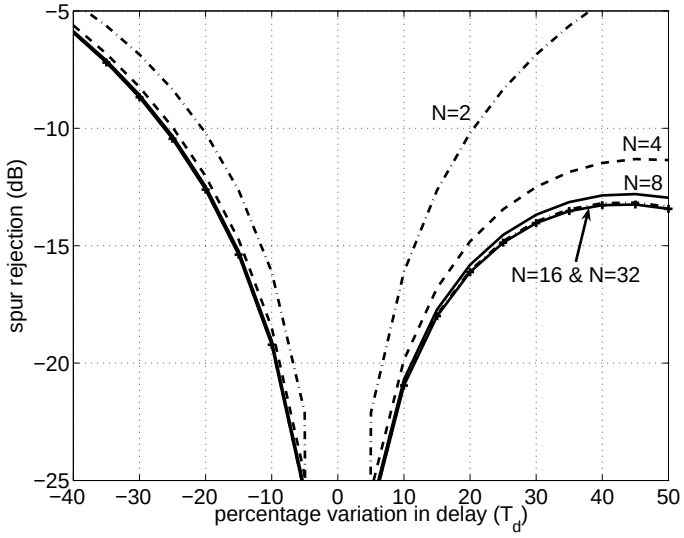

Figure 2.5: Sensitivity to delay variations.

$f_z = k/NT_d$ where k is an integer and $k \neq 0, N, 2N \cdots$. When $T_d = T/N$, the zeroes occur exactly at the multiples of f_r and the reference spurs up to Nf_r are completely eliminated. When $T_d \neq T/N$, the zeroes of the filter do not occur at multiples of f_r and reference spurs appear at the output. Fig. 2.5 shows the spur rejection when the delay T_d varies from the nominal value of T/N. As N increases, the sensitivity to delay variations improves up to $N = 8$ (improvement clearly seen

[3]The UP/DN pulses are delayed by multiples of T_d and one of them is chosen at random to implement the PPM.

for positive % delay variations). Beyond that the improvement becomes marginal and therefore $N = 8$ was chosen for implementation.

In the absence of any delay tuning mechanisms, the delays are prone to large variations ($\pm 40\%$), hence the spur rejection degrades severely especially for lower values of delays $T_d < T/N$ as seen from the figure (6 dB for -40 % variation). So to avoid this problem one can choose a skewed nominal delay such that $T_d \approx 1.3T/N$. As seen from the figure, even for $\pm 40\%$ variations in the skewed delay the spur rejection is at least 13 dB as opposed to 6 dB for the nominal delay. Addition of delay trimming mechanisms for process and temperature variations can reduce the systematic delay variations to $\pm 5\%$ resulting in at least 25 dB spur rejection.

2.4 Spur reduction techniques

The previous section dealt with the analytical study of PPM, where it was shown that PPM by an uniformly distributed iid sequence is equivalent to passing the signal through an N-tap moving average filter and the energy in the reference harmonics were removed and redistributed as wideband noise. In a charge pump PLL, a periodic current is injected into the loop filter in the presence of nonidealities which leads to reference spurs at the PLL output as explained in chapter 1. In the current work, the periodicity in the charge pump current pulses is broken by pulse position modulating the current pulses thereby redistributing the reference spurs as noise. Other spur elimination techniques such as pulse repetition (PR) which involves passing the current pulses through a moving average filter thereby removing the spurs completely without redistributing them as noise are also discussed in detail. Variants of PPM and a combination of PPM and PR that have advantage over a simple uniform PPM is also presented and their advantages are discussed in detail in the remainder of this section.

Fig. 2.6 shows the modified PLL architecture employing the PPM based techniques at a block level, with the illustrative charge pump current pulses before

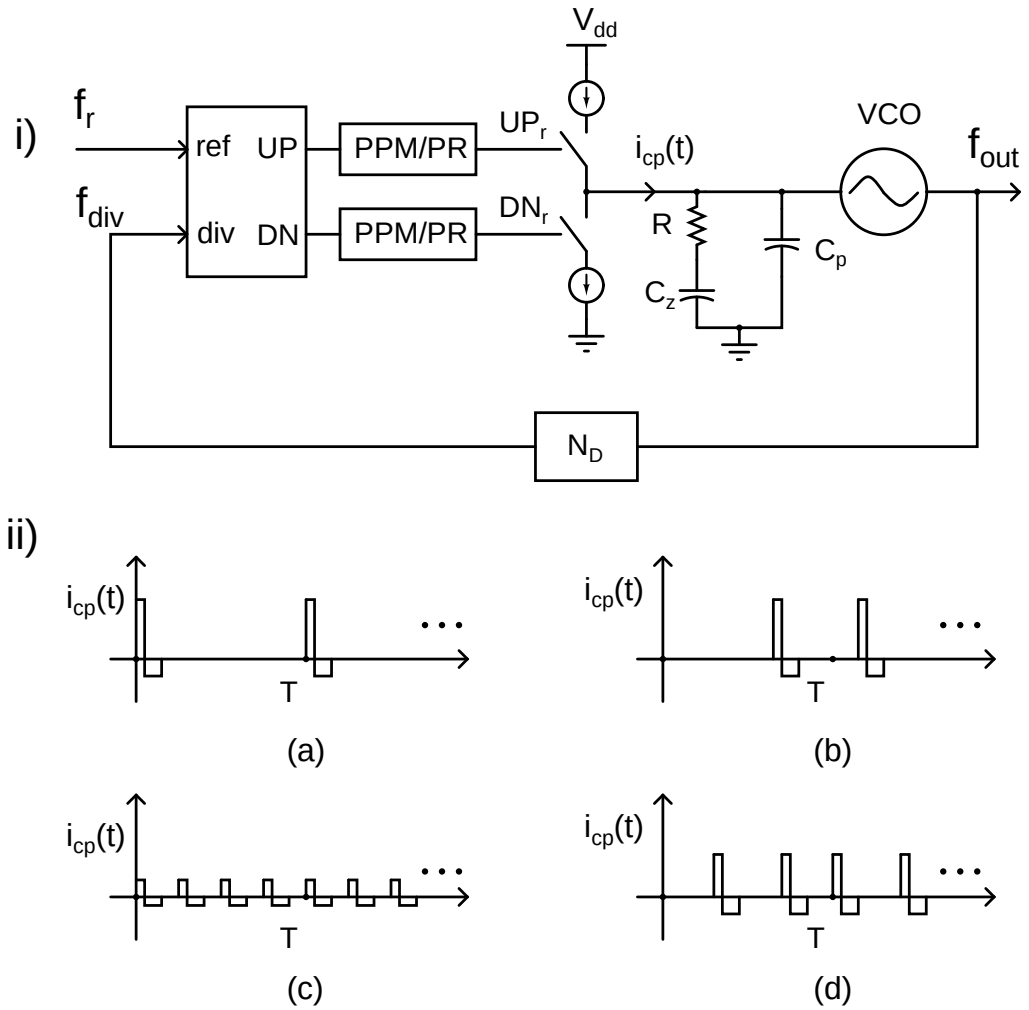

Figure 2.6: i) The modified PLL architecture with pulse position modulator/pulse repeater shown at block level. ii) Illustrative waveforms of charge pump current before and after applying the techniques (a) Standard PLL, (b) PPM, (c) Pulse Repetition (PR), (d) PPM+PR.

and after applying the techniques.

2.4.1 Random pulse position modulation (PPM)

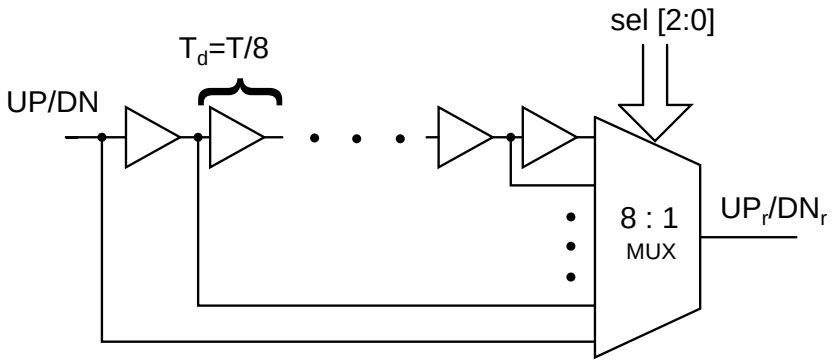

Figure 2.7: Implementation of PPM.

As explained in section 2.3, PPM of charge pump current pulses removes spurs up to Nf_r and converts them to wideband noise. To implement the technique the pulse position of the UP/DN signals is modulated based on a random control signal $sel[2:0]$. Modulating the pulse position can be accomplished by delaying the pulses and choosing one of the 8 delayed versions using a $8:1$ MUX based on the control signal as shown in Fig. 3.11.

2.4.2 Pulse repetition (PR)

Instead of randomizing the pulse positions, we can repeat the pulse N times at intervals of T/N within a single period, making it appear as a high frequency (Nf_r) signal. The charge pump current is reduced by a factor of N to ensure that the charge delivered by the charge pump per reference cycle remains the same. This is same as passing the current pulse through a N-tap moving average filter $C_N(f)$. The PSD $S_{pr}(f)$ of the N-PR (N here refers to the number of the repeated pulse positions) signal is

$$S_{pr}(f) = \frac{1}{T^2}|C_N(f)|^2 \sum_k \delta(f - kf_r) = \frac{1}{T^2} \sum_k \delta(f - kNf_r) \tag{2.13}$$

In N-PR, the harmonics in $[f_r, (N-1)f_r]$ are filtered out and unlike in N-PPM there is no additional redistributed noise.

N-PR is implemented in [7] using N scaled charge pumps driven by delayed UP/DN pulses generated by a distributed phase frequency detector (PFD). This method of implementation increases the complexity as the number of charge pump cells and PFDs increase with N. A much simpler implementation would be to drive a single scaled charge pump with a repeated UP/DN pulse, generated by passing N delayed versions of the UP/DN pulses through an N-input OR gate as shown in Fig. 3.14 (a). For input phase errors smaller than T/N, the proposed implementa-

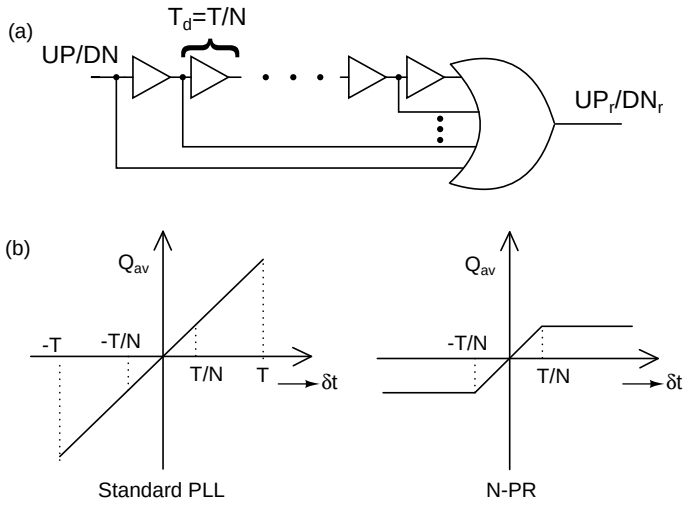

Figure 2.8: (a) Pulse repeater circuit, (b) Charge delivered per reference cycle vs phase error δt by the standard PFD+charge pump and N-PR+scaled charge pump.

tion of the N-PR technique behaves similar to a standard PLL (charge delivered per reference cycle is same for both the cases). For phase errors greater than T/N, the delayed UP/DN pulses overlap and the output of the OR-gate is always held high leading to gain saturation (charge delivered remains constant for errors $> T/N$) as shown in Fig. 3.14 (b), which increases the settling time of the PLL. In order not to affect the settling behaviour of the PLL, pulse repetition needs to be deactivated and the charge pump current scaled up by a factor N when the PLL is out of lock. This requires additional circuitry in the implementation.

2.4.3 Pulse position modulation with pulse repetition (PPM+PR)

Since PR removes the reference harmonics without redistributing it as noise, it may seem more attractive than random PPM. However, when the charge pump current is small (of the order of few micro amperes), dividing the current further by N may not be possible due to the restrictions imposed by the charge pump mismatch and leakage currents. Also charge pump switch sizes and mismatch may not scale with charge pump currents, leading to an increase in the net error current injected into the loop filter due to nonidealities. In that case as both PR and PPM offer the same spur rejection, the PR technique can perform poorly when compared to PPM in the presence of delay variations, since the magnitude of the inherent spur is larger.

A combination of PR and PPM results in a better performance. To achieve the same spur rejection of 8-PPM and 8-PR, we apply 4-PPM in conjunction with 2-PR, by passing the pulse through a 2-tap moving average filter $C_2(f)$ given by $C_2(f) = (1 + e^{-j\pi fT})/2$ and then randomizing the filtered pulse positions to four values spaced $T/8$ seconds apart (this ensures that all the 8 pulse positions are occupied). Fig. 2.10 (a) shows the UP/DN pulses before randomization and the possible positions occupied after applying the technique. The spectrum of the resulting signal is[4]

$$\frac{1}{T^2}\sum_k \delta(f - kf_r)|C(f)|^2|C_2(f)|^2 + \frac{1}{T}(1 - |C(f)|^2)|C_2(f)|^2$$

where $C(f)$ is the pseudo filter associated with the 4-PPM, $C(f) = 0.25\sum_{k=0}^{3} e^{-j\pi fkT/4}$. $C_2(f)$ has zeroes at odd harmonics of f_r and $C(f)$ has zeroes at even harmonics of f_r except at multiples of $8f_r$. We can easily verify that

$$C(f)\cdot C_2(f) = \frac{1}{8}\sum_{k=0}^{7} e^{-j\pi fkT/4} = C_8(f) \tag{2.14}$$

[4]The spectrum can be obtained by first deriving the spectrum of the signal for 4-PPM with $T_d = T/8$ using Eq. (2.10) and then multiplying the resulting spectrum by $|C_2(f)|^2$ (since 2-PR is equivalent to passing the signal through the filter $C_2(f)$).

which is equivalent to an 8-tap moving average filter. The spectrum of the signal reduces to

$$\frac{1}{T^2}\sum_k \delta(f - 8kf_r) + \frac{1}{T}(1 - |C(f)|^2)|C_2(f)|^2 \tag{2.15}$$

Eq. (2.15) shows that the spur rejection equals that of 8-PPM and 8-PR. The

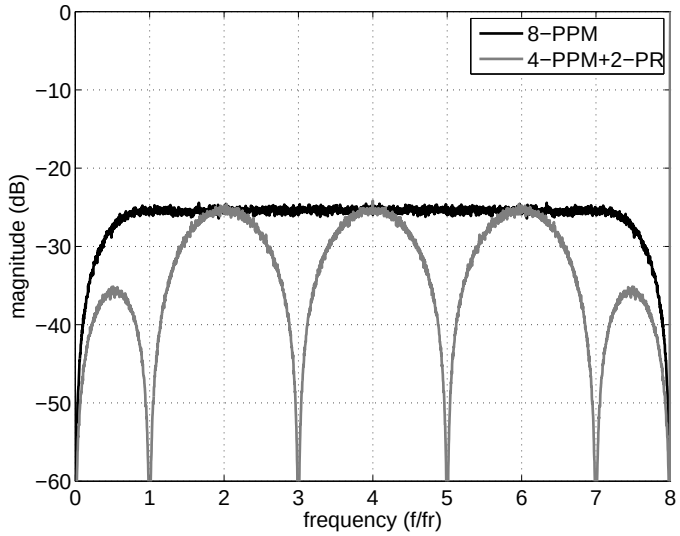

Figure 2.9: The spectrum of the 8-PPM signal overlaid with the 4-PPM+2-PR signal (PSD computed with a resolution binwidth of $f_r/512$).

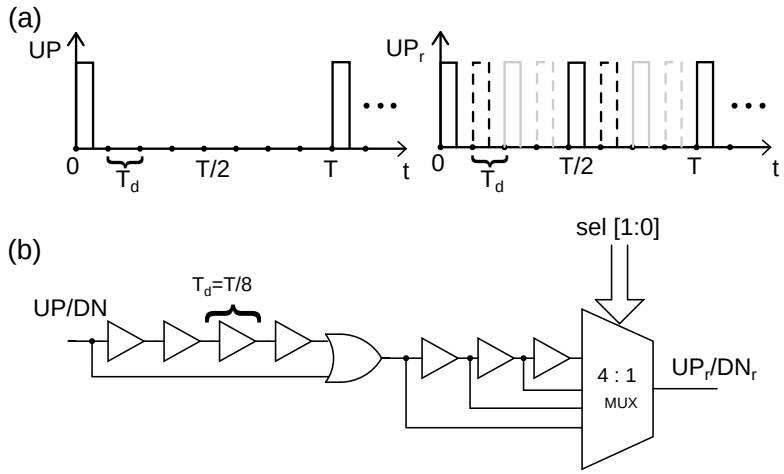

Figure 2.10: (a) The UP pulse before and after applying the technique, (b) Implementation details of combined 4-PPM+2-PR technique.

redistributed noise is lower compared to 8-PPM as it gets filtered by $C_2(f)$. One can intuitively see that the current pulse is passed through a 2-tap moving average filter (2-PR), which eliminates the odd harmonics of f_r and when 4-PPM

is applied, the power concentrated in the remaining even harmonics (other than harmonics of $8f_r$) are redistributed as noise. Since the total power in the reference harmonics is reduced after 2-PR, the redistributed noise in the 4-PPM+2-PR is smaller compared to 8-PPM.

Fig. 2.9 shows the simulated spectrum of the 4-PPM+2-PR signal overlaid with the spectrum of 8-PPM signal. We can see from the figure that the noise with the combined technique is lower than 8-PPM technique as expected. Fig. 2.10 (b) shows the implementation details of the 4-PPM+2-PR technique. The repeated UP/DN pulse is generated by first passing the pulse and a half cycle delayed version of the pulse to a two input OR gate and then pulse positions of the repeated pulse are randomly selected using a $4:1$ MUX based on a two bit control word sel$[1:0]$. The implementation complexity is also reduced compared to 8-PPM as the complexity of multiplexer and the logic generating the select signals is now reduced.

2.4.4 Shaped PPM+PR

When the magnitude of the spur is high, the redistributed noise floor is correspondingly high. The noise is then passed through the PLL transfer function which provides high gain for 'midband' frequencies ($f_r/100$ to $f_r/10$) inside the bandwidth of the PLL. In cases where the PLL has very low phase noise requirements the redistributed noise may form a lower bound on the noise floor in this region. To resolve this problem we can increase the order of noise shaping of the redistributed noise[5].

The PSD of the PPM signal modulated by an iid sequence a_i depends only on the probability distribution of a_i. When the samples of a_i are correlated, the resulting spectrum not only depends on its probability distribution but also on its correlation properties. The correlation properties of a_i can be exploited to control

[5] A similar approach albeit for a different purpose is proposed in [11].

the shape of the redistributed noise. The spectrum of PPM becomes too complex to compute analytically when a_i is correlated for the general case (for any N). Fortunately it is very easily tractable for $N = 2$. The spectrum $S_{rc}(f)$ of the shaped PPM (SPPM) signal when a_i takes on binary values (0 and 1) with equal probability ($p = 0.5$), is given by (Appendix A.1.3)

$$S_{rc}(f) = \frac{1}{T^2}|C_2(f)|^2 \sum_k \delta(f - kf_r) + \frac{4\sin^2(\pi fT/2)}{T} S_a(f) \tag{2.16}$$

where $S_a(f)$ is the PSD of a_k and $C_2(f)$ is the associated 2-tap pseudo moving average filter. Eq. (2.16) shows that the redistributed noise depends upon the PSD $S_a(f)$ of a_i. Thus the redistributed noise can be tailored to shape the noise further to higher frequencies by controlling the PSD of a_i. If the sequence a_i has a high-pass spectrum, from Eq. (2.16) the order of the high pass shaped redistributed noise is $G + 1$, where G is the high-pass order of $S_a(f)$.

One can realize an N-SPPM using an m-bit shaped sequence ($N = 2^m$) generated using m independent one bit shaped sequences[6].

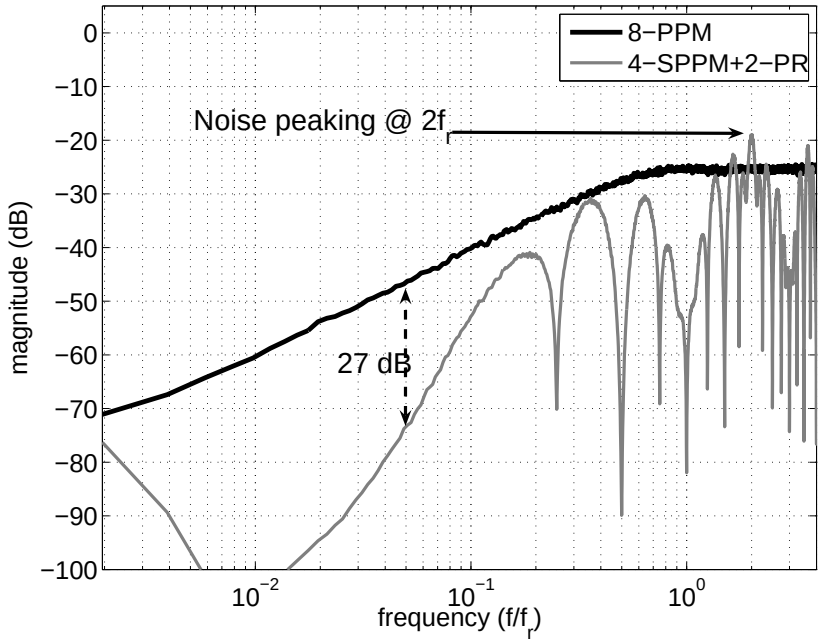

Figure 2.11: The spectrum of the 8-PPM signal overlaid with noise shaped 4-SPPM+2-PR signal shown on a log scale for noise comparisons (PSD computed with a resolution binwidth of $f_r/512$).

The shaped PPM will increase the high frequency noise floor and hence it has to be used in conjunction with PR technique to reduce high frequency noise. For $N = 8$, the two possible combinations are one bit SPPM with 4-PR (2-SPPM+4-PR) and two bit SPPM with 2-PR (4-SPPM+2-PR). Though using a 4-PR technique results in a lower high frequency noise, it suffers from the aforementioned problems of gain saturation and net increase in spur magnitude in the presence of nonidealities like 8-PR. Hence we go for 4-SPPM+2-PR technique.

A 4-SPPM+2-PR technique is the same as 4-PPM+2-PR except that the modulating sequence is a two bit higher order shaped sequence. In the current work we chose a third order shaped sequence to achieve low midband noise. The two bit shaped sequence was generated by combining two independent third order shaped one bit sequences (generated as described in later sections). The two bit sequence can be represented as $a_c[k] = 2a_1 + a_0$ where a_1 and a_0 are two one bit sequences with PSD given by $S_a(f) = |\sin(\pi fT)\sin(2\pi fT)\sin(4\pi fT)|^2$. The PSD of the two bit sequence is

$$S_{ac}(f) = 5|\sin(\pi fT)\sin(2\pi fT)\sin(4\pi fT)|^2$$

The PSD[7]of the 4-SPPM+2-PR signal is given by (Appendix A.1.4)

$$\frac{1}{T^2}\sum_k \delta(f - kf_r)|C(f)C_2(f)|^2 + \frac{2}{T}|C_2(f)|^2 S_a(f)\left(\sin^2(\pi fT_d) + \sin^2(3\pi fT_d)\right)$$

$$+\frac{4}{T}|C_2(f)|^2 S_{a2}(f)\left(2\sin^2(2\pi fT_d) + \sin^2(\pi fT_d) - \sin^2(3\pi fT_d)\right)$$

where $S_{a2}(f) = \sum_k \left(R_a(k)\right)^2 e^{-j2\pi fkT}$ The pseudo filter and the 2-tap moving average filter associated with this technique are similar to those in the 4-PPM+2-PR

[6]Extending the results presented in Appendix A.1.3, we can readily show that the redistributed noise depends up to m^{th} power of the autocorrelation function for m-bit case. This results in the noise not truly being $(G+1)^{th}$ order shaped due to the additional terms in the redistributed noise.

[7]The spectrum is derived in a similar manner as the 4-PPM+2-PR signal. First the spectrum of 4-SPPM is computed (Appendix A.1.4) and the resulting spectrum is passed through the filter $|C_2(f)|^2$

technique. This ensures that the reference spurs up to $8f_r$ are absent. The redistributed noise however depends on the PSD $S_a(f)$ of the one bit sequences a_i and the Fourier transform of its squared autocorrelation $(R_a(i))^2$ (proof given in Appendix A.1.4). Thus the noise is not truly third order shaped due to the additional component in the redistributed noise. Nevertheless it leads to a significant reduction in the noise in the midband frequency range. Fig. 2.11 shows the spectrum of the 4-SPPM+2-PR overlaid with 8-PPM. The high frequency noise is lower than the 8-PPM technique for most of the frequencies and peaks at some points which is expected in a shaped PPM. The midband noise is orders of magnitude less due to aggressive noise shaping of the SPPM technique.

The implementation of the 4-SPPM+2-PR is similar to the 4-PPM+2-PR technique as shown in Fig. 2.10, where the two bit control signal is the shaped two bit random sequence.

2.5 Delaying narrow UP/DN pulses

To obtain a delay of T_d, we need an infinite bandwidth system with transfer function e^{-sT_d}. An inverter is a delaying system with a finite bandwidth, which depends upon the device length and the technology. This restricts the minimum pulse width that a chain of inverters can delay reliably without attenuating it below the switching threshold. In a given technology, a maximum bandwidth digital delay line can be realised using a long chain of minimum length inverters. In a $0.18\,\mu m$ CMOS process with a 1.8 V supply to realize a maximum bandwidth delay line of delay 6.25 ns (T_d), the number of minimum length inverters necessary is close to 100 and the average current consumption is 31 μA. At the slowest process and temperature corners this chain can pass pulses of width > 200 ps without significant attenuation. This minimum delayable pulse width (MPW) reduces as technology scales down.

In a practical charge pump PLL, to improve the linearity of the PFD/CP and thus

avoid the problem of dead zone, a non-zero reset delay of T_{rst} seconds is introduced in the PFD reset path depending upon the size of the charge pump switches and tolerable spur level. This ensures that the UP/DN pulses are 'on' for at-least T_{rst} seconds even when the PLL is in lock condition. The value of T_{rst} can be close to a few hundred picoseconds ([6, 12]), well above the minimum delayable pulse width. Based on the value of T_{rst}, the delay line is designed by varying the length and supply voltage of the inverters used in the delay chain to obtain the desired delay.

In cases where the desired T_{rst} is close to the minimum delayable pulse width, the delay line needs to have a very high bandwidth. Hence a large number of

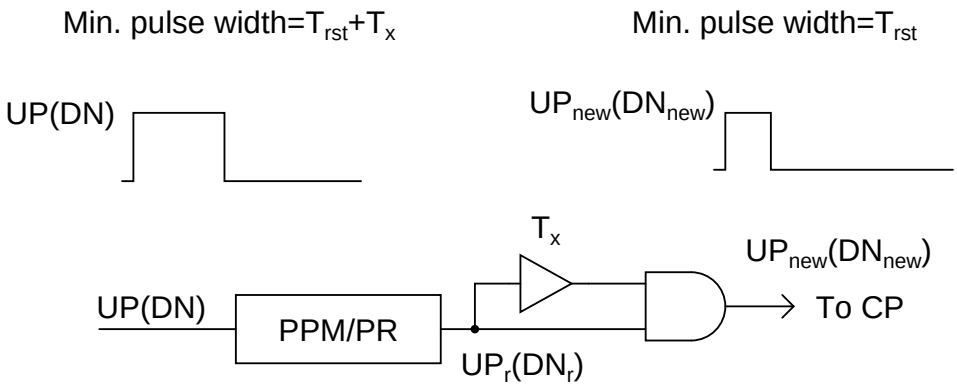

Figure 2.12: Implementation of the technique to tackle the narrow pulse problem.

minimum sized inverters are necessary to realize the desired delay. A straightforward approach to reduce the delay line bandwidth (hence its area and power) is to increase the reset delay more than the desired value (thus making the UP/DN pulses wider). But it leads to a proportional increase in spur level and noise contribution from the CP, when fed to the charge pump in the presence of charge pump nonidealities [6].

To resolve this problem, the width of the UP/DN pulses is first increased by T_x before feeding it to the delay line and then reduced by the same amount once it is out of the randomizing blocks, before being fed to the charge pump. Thus the delay line sees wider UP/DN pulses and the charge pump sees narrower pulses, relaxing the delay line bandwidth without compromising the spur level and noise.

Increasing the UP/DN pulse width by T_x can be accomplished by increasing the PFD reset delay to $T_{rst} + T_x$ and decreasing the pulse width at the output of the randomizing block can be accomplished using a two input AND gate and a delay T_x as shown in Fig. 2.12. Thus the minimum UP/DN pulse width seen by the delay line is $T_{rst} + T_x$ and the reset delay pulse width seen by the charge pump is T_{rst}. Even if T_{rst} is small, T_x can be adjusted such that $T_{rst} + T_x$ is wide enough for it to be transmitted through the delay line without increasing its area and power. For a T_{rst} of 500 ps, to realize a delay of 6.25 ns in a 0.18 μm technology, the number of inverters necessary is close to 60, with their length equal to 0.25 μm and an average current consumption of 18 μA. Using the aforementioned technique, with T_x=2.5 ns, the number of inverters necessary to realize the same delay across process and temperature variations is 6, with their length equal to 1.25 μm and an average current consumption of 4.3 μA. Hence the implementation of the delay cell is made simpler and independent of T_{rst}. The implementation techniques presented in section 2.4 can be used with this minor addition of an AND gate and delay T_x. In case of PR, the minimum time difference between two pulses is T_d seconds and hence the delayed pulse should not overlap with the next pulse. This restricts T_x to be less than $T_d/2$.

Another approach to implement the PPM/PR techniques is to place the delay line before the PFD [7], where the delay lines are driven by the ref and div signals instead of the UP/DN signals. Circuits for PPM, PR and PPM+PR with this modified architecture are shown in Fig. 2.13. In this method the width of the pulses is not a concern as the ref/div signals are much wider than the UP/DN signals and the bandwidth of the delay line can be lower (two inverters with their length equal to 3.3 μm is sufficient to realize a delay of 6.25 ns). Though placing the delay line before PFD might seem attractive due to their small area and power dissipation, a detailed comparison between the two methods (discussed in section 2.7) shows that the delay line after PFD has advantages like better delay mismatch insensitivity, reduced implementation complexity and relatively smaller delay line

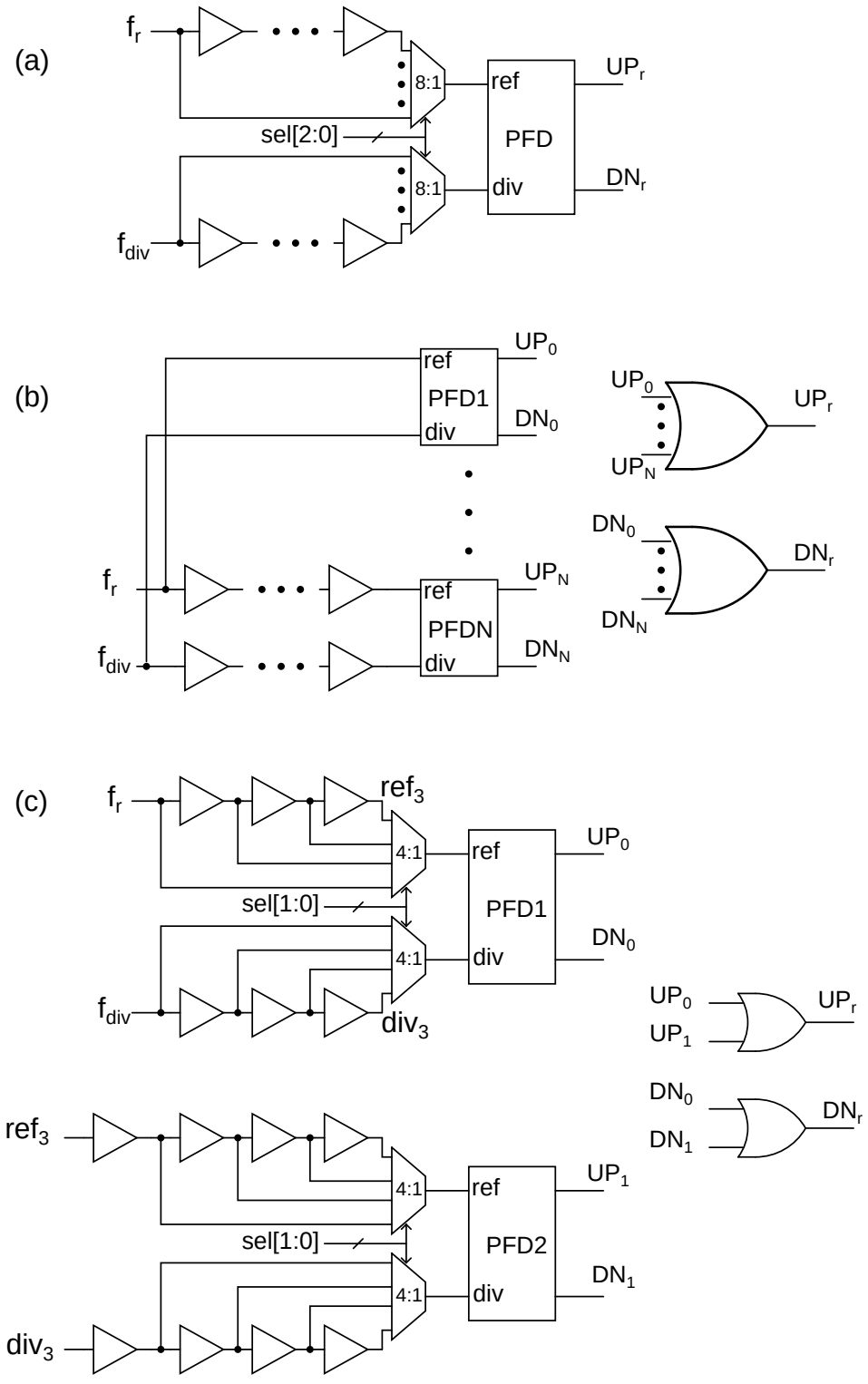

Figure 2.13: Alternative implementation with delay lines placed before the PFD: (a) PPM, (b) PR, (c) PPM+PR.

area (and current consumption) for the same jitter specification, compared to the former method.

2.6 Modulating sequence generation

In practice the modulating sequence a_k is generated using a pseudo random bit sequence (PRBS) generator. Sequences produced by the PRBS generator are deterministic and periodic [13]. Let a_k be a uniformly distributed periodic sequence with a period M. Since the modulating signal is periodic, the PPM signal also exhibits a periodic behaviour with a period $T_p = MT$. The PSD $S_{r,per}(f)$ of the periodic PPM signal is given by (derived in Appendix A.1.2)

$$S_{r,per}(f) = \frac{1}{T^2}\sum_k \delta(f - kNf_r) + \frac{(1 - |C_N(f)|^2)}{MT^2}\sum_k \delta(f - \frac{kf_r}{M})$$

The above equation shows that, in a periodic PPM, the noise shaping and the filtering nature of the random PPM are still preserved. But the redistributed noise has only discrete 'frequency slots' (or impulses) over which the noise is spread due to the modulating signal's periodicity (unlike the random case where the noise is spread continuously). This might seem intuitive since the PPM signal is periodic with a period T_p, its spectrum should have energy concentrated only at the harmonics of $1/T_p$. The harmonics of f_r are also the harmonics of $1/T_p = f_r/M$, hence the redistributed noise contains spur at kf_r, but reduced in magnitude. Since $C_N(kf_r) = 0$ for $k \in [1, N-1]$, for a N-tap moving average filter, we can compute the strength of the reference spurs kf_r to be

$$S_{r,per}(kf_r) = \frac{1}{MT^2}\delta(f - kf_r) \tag{2.17}$$

Comparing the above equation to the spectrum of an unmodulated impulse train, we can see that the strength of the reference harmonics is reduced by a factor

M. So increasing the periodicity reduces the redistributed noise level (by 3 dB for two fold increase in M). One can intuitively see that increasing the time period increases the number of frequency slots over which the redistributed power can be spread and hence the noise level goes down.

2.6.1 Practical considerations for PRBS generation

Linear feedback shift register (LFSR) is used to generate a PRBS. A sequence $a[i]$ constructed using the taps of a LFSR will tend to have a uniform distribution if sufficiently long lengths[8] are used (as frequency of ones and zeros in the PRBS sequence will approach 0.5). For a LFSR of length L, the periodicity of the sequence generated is $M = 2^L - 1$. Increasing L increases the period and hence reduces the noise level. Thus a long LFSR length not only ensures uniform distribution but also a lower redistributed noise floor. For an LFSR of length 15 ($M = 2^{15} - 1$), the spur is reduced by $10\log(M) = 45.2$ dB.

A three bit ($N = 8$) modulating sequence $a[i]$ can be generated using three taps of a single LFSR or by taking each bit from three LFSRs with different feedback configurations. In the latter case the sequence generated will have a 'white' spectrum as the samples of the sequence appear uncorrelated to each other. But the implementation complexity is increased as we will need three LFSRs. When the sequence is generated from a single LFSR, the samples of the sequence are correlated as the tap outputs ($z[i]$) of the single LFSR are just shifted versions of each other. For example taking the three consecutive tap outputs of a LFSR, the modulating sequence is given by $a_c[i] = \sum_{s=0}^{2} 2^s z[i-s]$. The sequence $a_c[i]$ possesses a low pass spectrum. For a low pass spectrum of the modulating sequence, the PPM signal will have higher noise at low frequencies than in the case when the modulating sequence is uncorrelated. Fig. 2.14 shows the 8-PPM spectrum when modulated by an uncorrelated sequence generated by combining three

[8]LFSR length refers to the number of shift registers.

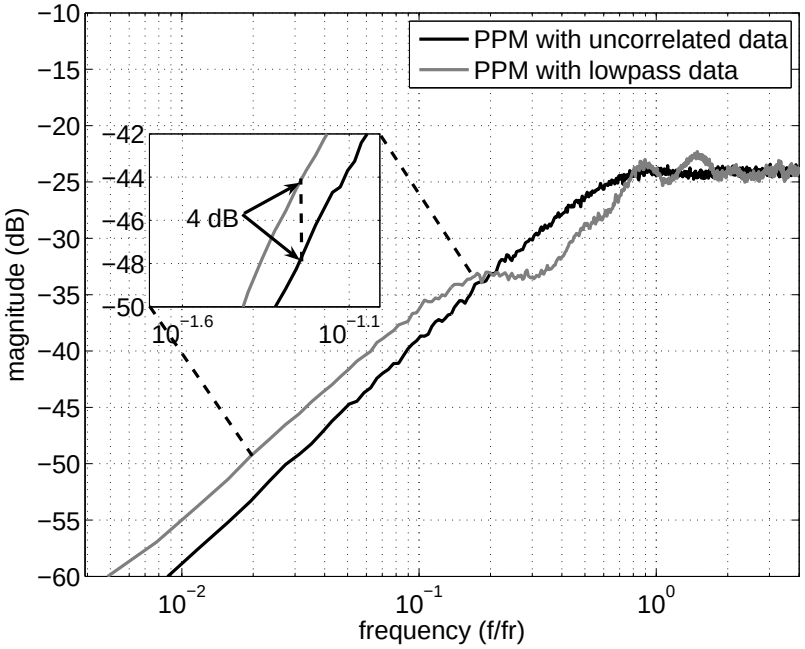

Figure 2.14: The spectra of the 8-PPM signal modulated by an uncorrelated (white) data and correlated (lowpass) data shown on log scale for noise comparisons (PSD computed with a resolution binwidth of $f_r/512$).

uncorrelated one bit data, overlaid with the 8-PPM spectrum when modulated by the correlated low pass sequence $a_c[i]$ in the above example. We can see that the spurs are absent in the correlated case as well, but the low frequency noise floor ($f_r/100 < f < f_r/10$) increases by 4 dB. Since the increase is marginal, it is not critical as the low frequency noise is dominated by the PFD and charge pump noise. Hence we can generate the three bit sequence from a single LFSR itself to reduce the implementation complexity.

2.6.2 Shaped data generation

One method of generating shaped binary data for SPPM is by feeding a uniformly distributed dither at the input of the quantizer of a one bit sigma delta modulator (SDM). This ensures that the output bits generated will have an uniform distribution (equal number of ones and zeroes) but the spectrum is high pass shaped by the noise transfer function (NTF [14]) of the SDM.

Another way of generating shaped binary random numbers with equal number of zeroes and ones is to use the Manchester encoding given in [15]. Manchester encoding maps a bit 1 to [10] and bit 0 to [01] from a random binary data stream, which provides a first order shaping [15]. Hence a third order shaped sequence can be generated by repeating the procedure three times. After the repeated encoding process, bit 1 is mapped to [10010110] and bit 0 is mapped to [01101001]. The magnitude spectrum of the shaped random binary stream (after removing the dc component) can be shown to be $|sin(\pi fT)sin(2\pi fT)sin(4\pi fT)|$. This method of generating shaped binary random numbers is very simple to implement because it requires a single LFSR running at $f_r/8$ and a few additional registers. Therefore we choose this method for generating the shaped sequence.

2.7 Effects of delay line nonidealities

The delays are implemented using CMOS inverters and are prone to process variations, random mismatch and device noise (thermal and flicker). The effect of process variations is discussed in section 2.3.2. The mismatch in the delay lines leads to a reference spur and the noise in the delay lines increases the noise floor at the VCO output. The detailed analysis is discussed in the remainder of the section.

2.7.1 Effect of mismatch

In the presence of mismatch, a delay of iT/N in the UP and DN signal paths, becomes $iT/N + \Delta T_{ui}$ and $iT/N + \Delta T_{di}$ respectively as shown in Fig. 2.15. To analyze its effect on the PLL performance, we split the delay variation into common mode and differential components. When these pulses are fed to a charge pump, the common mode component in the delay $iT/N + (\Delta T_{ui} + \Delta T_{di})/2$ leads to an additional time shift in the current pulse from its ideal position and the differential

component in the delay $\Delta T_{di} - \Delta T_{ui}$ produces a zero average current pulse whose width is equal to $\Delta T_{di} - \Delta T_{ui}$ as shown in Fig. 2.15. The narrow charge pump current pulses can be modeled as impulses spaced T_{rst} seconds apart[9] with weights given by the area under the pulses and delayed by the common mode component. Let ΔT be variation (due to device mismatch or random device noise) in the delay of single delay cell of value T/N (where ΔT is a zero mean gaussian random variable with variance ${\sigma_{\Delta T}}^2$). A delay of iT/N is obtained by passing the pulse through i identical delay cells of value T/N. Assuming that the variations in the delay cells are independent of each other, the variance associated with the delay iT/N is $i{\sigma_{\Delta T}}^2$. Thus the variance of random variables ΔT_{ui} and ΔT_{di} is $i{\sigma_{\Delta T}}^2$. Let $\Delta T_{cmi} = (\Delta T_{ui} + \Delta T_{di})/2$ and $\Delta T_i = \Delta T_{di} - \Delta T_{ui}$ be the common mode and differential variations in the delay iT/N. Then $\sigma_{\Delta T_{cmi}} = \sqrt{i/2}\sigma_{\Delta T}$ and $\sigma_{\Delta T_i} = \sqrt{2i}\sigma_{\Delta T}$. In the presence of common mode mismatch, the phase

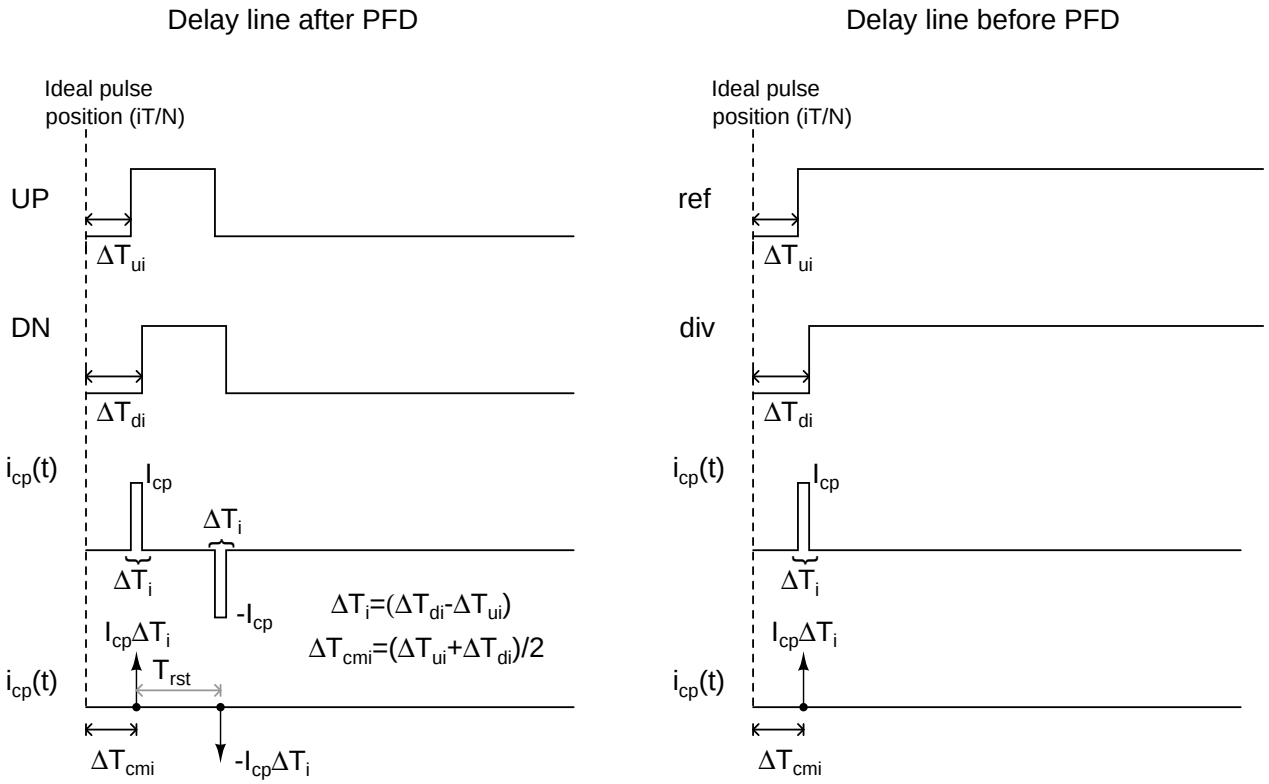

Figure 2.15: The UP/DN pulse waveforms and the charge pump current in the presence of delay variations corresponding to a delay of iT/N.

[9]In the analysis it is assumed that only the delay cell is the source of noise and hence the width of UP/DN pulses is equal to T_{rst} (the reset delay seen by the charge pump).

shift iT/N becomes $iT/N + \Delta T_{cmi}$, which leads to a change in the delays of the pseudo filter. When the delays vary, the location of the zeroes of the pseudo filter change ($f_z \neq k/T$) leading to a degradation in spur rejection. The maximum degradation occurs when there is maximum variation in the delays. Since ΔT_{cmi} is a gaussian random variable, the maximum variation in in the delay iT/N is considered to be $\approx 3\sigma_{\Delta T_{cmi}}$. The pseudo filter $C(f)$ for a worst case scenario can be written as

$$|C(f)| = \frac{1}{N}\left|\sum_{i=0}^{N-1} e^{-j2\pi f(iT/N+3\sqrt{i/2}\sigma_{\Delta T})}\right|$$

Fig. 2.16 shows the degradation in spur rejection in the presence of random mismatch. A point to note is that, in the absence of any delay trimming mechanisms the effect of these random mismatch errors will be dominated by the large systematic errors in the delay caused by temperature and process variations as explained in section 2.3.2. The degradation due to systematic errors ($\pm 10\,\%$) is overlaid with the random mismatch case in Fig. 2.16 to show its dominance.

The differential mismatch produces a zero average current pulse whose amplitude depends upon the delay value selected. The effect of differential mismatch on the PLL output spectrum can be easily understood in case of PR. When a delay of iT/N is selected, the error pulse injected can be expressed as $(I_{cp}\Delta T_i/N)p_d(t - iT/N)$, where $p_d(t) = \delta(t) - \delta(t - T_{rst})$. In PR, N delayed versions of the UP/DN signals appear per reference cycle, hence we have N mismatch current waveforms corresponding to the N delayed versions. So a periodic current is injected into the loop filter every reference cycle in the presence of differential mismatch between the delay lines. Thus differential mismatch is an additional source of reference spur. The worst case scenario occurs when the mismatches between the delays in the UP/DN delay lines add up in the same polarity and $\Delta T_i = 3\sqrt{2i}\sigma_{\Delta T}$. The periodic charge pump current injected per reference cycle due to the differential

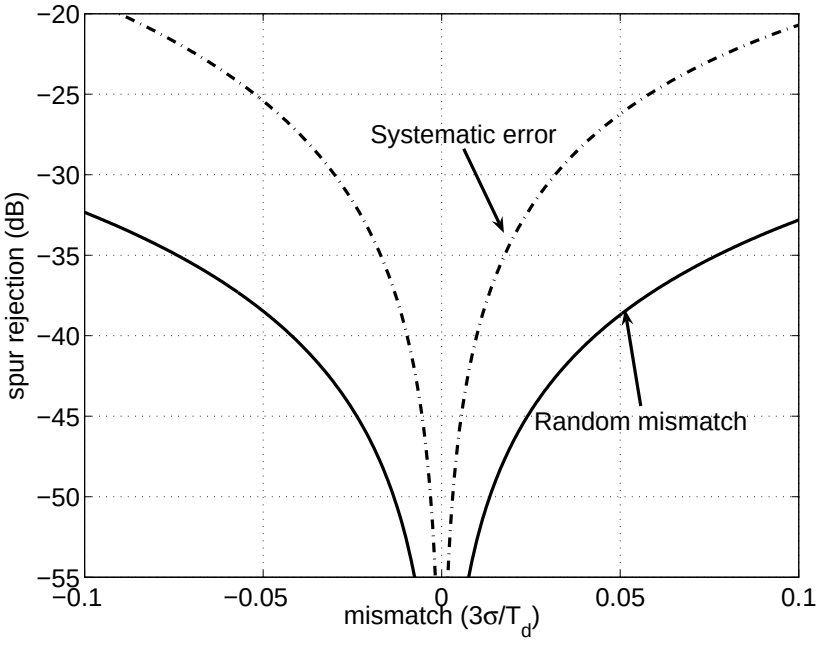

Figure 2.16: Spur rejection vs random delay mismatch.

mismatch can be expressed as

$$i_{ncp}(t) = \frac{\sqrt{2} I_{cp} 3\sigma_{\Delta T}}{N} \sum_{i=0}^{N-1} \sqrt{i} p_d(t - iT/N) \tag{2.18}$$

The magnitude of the spur (dBc) using Eq. (1.3) is given by

$$20 \log \left| P_d(f_r) \frac{Z(f_r)\, K_{vco}}{f_r} \frac{\sqrt{2} I_{cp} 3\sigma_{\Delta T}}{NT} \sum_{i=0}^{N-1} \sqrt{i} e^{-j2\pi i f_r T/N} \right|$$

$P_d(f) = 1 - e^{-j2\pi f T_{rst}}$ is the Fourier transform of the pulse $p_d(t)$ which is first order highpass shaped. In case of the PPM based techniques, on an average over a large number of reference cycles, all the error waveforms appear equal number of times (since a_i is uniformly distributed) within a reference cycle. Hence the average current waveform per reference cycle is the same as in PR and so is the magnitude of the reference spur. Thus all the techniques produce spurs of the same magnitude. The PPM based techniques additionally add redistributed noise at the PLL output. For a T_{rst} of 780 ps and a 5 % mismatch in a single delay cell ($3\sigma_{\Delta T} = 0.05T/N$), the reference spur introduced is -61.6 dBc. To remove this

component of spur, the UP and DN delay lines can be randomly interchanged based on an additional random signal. The noise added by this randomization will have insignificant contribution at dc due to the highpass nature of the pulse $p_d(t)$. However it adds to the implementation complexity of the logic.

When the delay lines are placed before the PFD, only the positive half of the error current (in Fig. 2.15) is injected into the loop filter in the presence of mismatch. The PLL responds in a way such that the average current injected into the loop filter every reference cycle is zero. Thus the per cycle error current waveform in case of PR can be represented as

$$i_{ncp}(t) = \frac{\sqrt{2} I_{cp} 3\sigma_{\Delta T}}{N} \sum_{i=0}^{N-1} (\sqrt{i} - \alpha)\delta(t - iT/N) \tag{2.19}$$

where $\alpha = (1/N)\sum_i \sqrt{i}$. The magnitude of the spur for the same mismatch as before can be computed to be -41.25 dBc. The magnitude of the spur is 20 dB higher than the former case, where there is a significant reduction in spur due to the highpass nature of the pulse $p_d(t)$. Randomizing the mismatch in this case will directly affect the inband noise as well due to the absence of pulse shaping. This is one major disadvantage of placing the delay line before PFD. Results from behavioral transient simulations show that the spur reduction when the delay lines were placed after PFD was 19.1 dB more than when they were placed before the PFD (close to the value predicted by analysis).

When the pulse narrowing circuits (Fig. 2.12) are used in the UP and DN paths, there will be mismatch between T_x values used in the two paths. This mismatch appears as a dc phase offset (as every pulse is passed through the circuit) and gets corrected by the PLL. Thus no additional spur is created due to the mismatch between the delays in the pulse narrowing circuits.

2.7.2 Effect of noise

In the presence of delay line noise, the rising and falling edges of the UP/DN pulses are corrupted by jitter at the output of the delay line. This leads to an injection of noise current at both these edges spaced T_{rst} seconds apart into the loop filter. The noise analysis can also be carried in a similar manner by splitting the error as common mode and differential components. Unlike the case of delay mismatch, the variations in the rising and falling edge are not the same due to uncorrelated nature of the noise. The common mode component of the delay line noise can be treated as a random variation in the delays of the pseudo filter. This leads to degradation in the spur rejection. But this effect will be negligible compared to the effect of mismatch due to its small magnitude and hence it can be ignored.

The differential component of the delay noise however is an additive noise at the charge pump output and hence degrades the output phase noise. The jitter in the rising and falling edges can be treated as uncorrelated and identical noise sources. If $S_n(f)$ is the noise current density due to the rising edge jitter, then the total noise current density is $2S_n(f)$ (the sum of two uncorrelated noise PSDs).

When the delay lines are placed before the PFD [7], the jitter of the delay line acts as an input phase error to the PLL and the PFD measures the phase difference between the rising edge of the ref and div signals. So only the error current corresponding to the rising edge is injected into the loop filter and the noise current spectral density is given by $S_n(f)$. Thus the noise added due to delay line jitter is 3 dB lower compared to the former case.

Fig. 2.17 shows the PLL output phase noise when the delay line is placed before and after the PFD. For the computations, each delay cell (of delay 6.25 ns) was modeled to have an rms jitter of 2.8 ps[10]. The inband noise as shown in the figure is -107 dBc/Hz and -104 dBc/Hz when the delay lines are placed before and after

[10]The jitter was computed using the phase noise analysis in 'spectre' on a delay line built using six CMOS inverters in 0.18 μm technology with an MPW > 3 ns ($T_{rst} + T_x = 3$ ns and $T_{rst} = 780$ ps) and their supply held at 1.8 V. Also the same delay line is used before and after PFD.

PFD in case of PR. Thus with the same delay line jitter before and after PFD, the output phase noise is 3 dB more for the latter.

Also the figure shows that the PR technique adds the least noise among all the proposed techniques. In PR the amplitude of each pulse is $1/N$ of that in PPM, resulting in a $1/N^2$ times noise power per pulse. Since there are N pulses per period in PR as opposed to a single pulse in PPM, the total noise power due to the delay line jitter in PR is $N/N^2 = 1/N$ of that of PPM (9 dB less for $N = 8$). Thus making PR desirable due to the low noise levels associated with it.

When the delay lines are placed before the PFD, fewer inverters of lower bandwidth can be used to realize a given delay compared to when the delay lines are placed after PFD. But to a first order, for a given delay and jitter specification, the

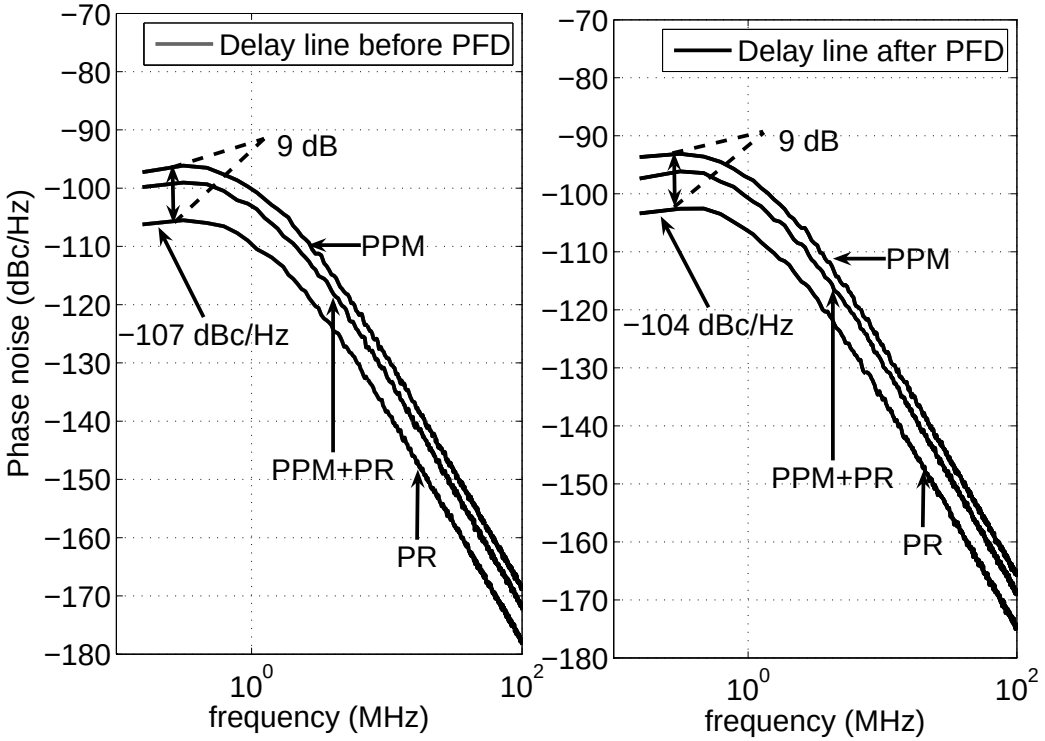

Figure 2.17: PLL output phase noise due to the delay line noise when delay line is placed after and before PFD.

power consumed by a short chain of low bandwidth inverters is the same as the long chain of high bandwidth inverters. Also simulations show that the gate area increases gradually as the delay line bandwidth reduces (or as device length increases). Therefore no significant benefit is gained in placing the delay line

before PFD, besides the 3 dB difference in noise mentioned above. This advantage has to be weighed against the significantly large spur due to mismatch between UP/DN delay lines as shown before, and, in case of PR, increased implementation complexity (multiple PFDs). In the author's opinion, it is preferable to place the delay line after the PFD and use the technique shown in Fig. 2.12 to increase the pulse width to a value that results in convenient bandwidth and the number of inverters in the delay line.

When the pulse narrowing circuits (Fig. 2.12) are used in the UP and DN paths, the jitter in the delay T_x directly contributes to the inband noise. But since the delay T_x is much smaller compared to the large delays of the delay lines in the randomizing blocks, its effect on the output phase noise is negligible compared to that of the latter. A detailed analysis of PPM was performed and several techniques based on the analysis were proposed to mitigate reference spurs. Owing to a strict time constraint we could only implement PPM and PR technique in the current work. The rest of the thesis explains the circuit details employed in implementing the techniques and present the simulation and measured results.

CHAPTER 3

Implementation Details

3.1 Introduction

The block diagram of the implemented PLL to test the proposed ideas of spur reduction is shown in Fig. 3.1. The parameters of the implemented PLL is shown

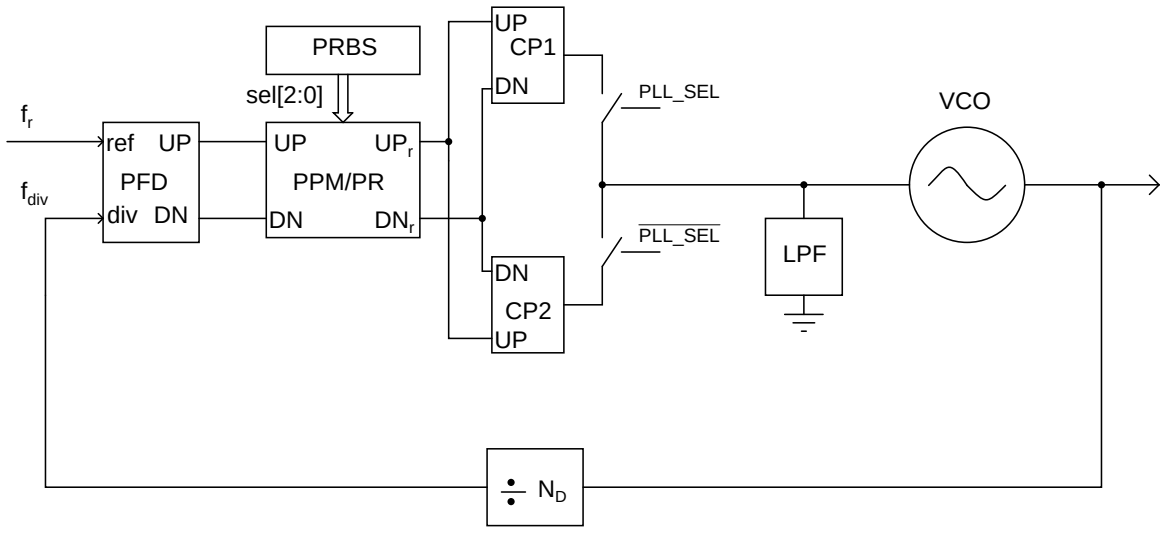

Figure 3.1: Block diagram of the implemented PLL.

in Table. 3.1. The UGB of the PLL was chosen to be $f_r/20 = 1\,MHz$. The circuit level implementation of the individual blocks are discussed in detail in the reminder of the chapter.

3.2 Phase frequency detector

A PLL is a feedback system that forces the divide phase to equal the reference phase. Any phase difference between the reference and divide signals is measured

Table 3.1: Implemented PLL parameters.

	Parameter
Input frequency	20 MHz
PFD	Tri-state PFD
Charge pump current	$I_{cp} = 56\,\mu$A
Loop filter	R = 21.7 kΩ, C_z = 37.25 pF, C_p = 1.99 pF
VCO	$f_{vco} = 1$ GHz, $K_{vco} = 300$ MHz/V
Divider	$N_D = 50$
unity gain bandwidth	$f_u = 1$ MHz
closed-loop 3dB bandwidth	$f_{3dB} = 1.9$ MHz
Phase margin	PM= 52.55^0

as an error signal by a phase frequency detector (PFD). Charge pump PLLs employ the classic tri-state PFD for its linear phase to voltage characteristics and zero static power dissipation in the steady state [1].

The schematic of the tri-state PFD used in the design is shown in Fig. 3.2. The reset path shown here has an 'AND' gate and a buffer which introduces a delay of 1.2 ns (in the nominal case) to address the problem of dead zone [1]. The D-flip

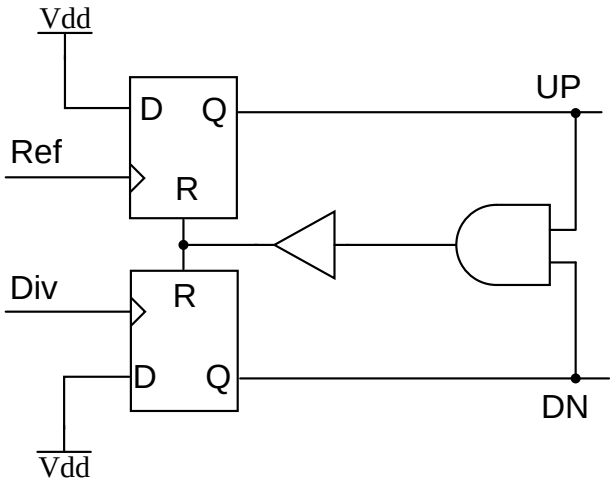

Figure 3.2: Tri-state PFD.

flop used in the design is a standard architecture built using high speed master and slave latches. The schematic of the D-flip flop is shown in Fig. 3.3. The flip-flop also has an asynchronous reset incorporated into it. The reset is performed by the MOS devices M_{nr} and M_{pr} as shown in the figure.

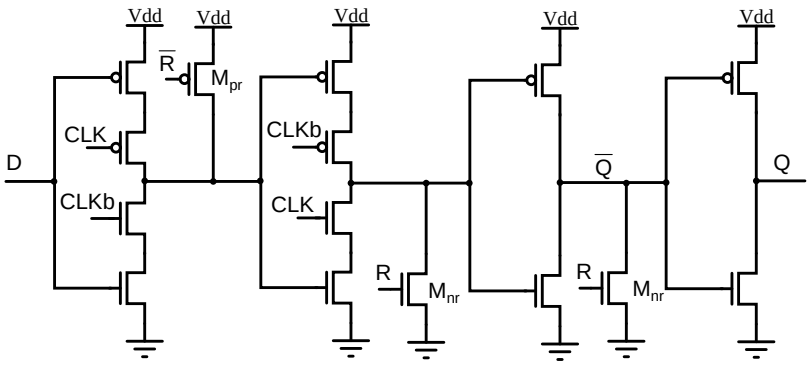

Figure 3.3: DFF used in the PFD.

3.3 Charge pump

Charge pump is the interface between the PFD and the loop filter. The UP/DN pulses contain the phase error information between the reference and divide signals in their pulse widths. Since the VCO needs a voltage for its control, a simple way to convert the error information in pulse widths to a voltage is to generate current pulses whose widths are proportional to the phase error and inject it into an impedance with lowpass characteristic.

3.3.1 Charge pump implementation

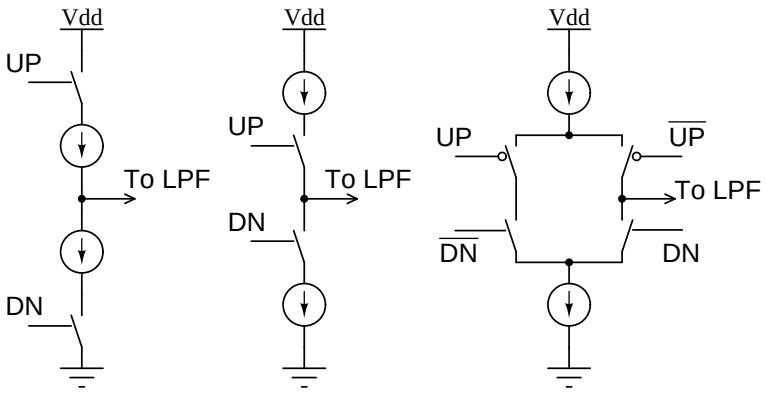

Figure 3.4: Charge pump switch arrangements.

To convert the phase error information in UP/DN signals to current pulses, the UP/DN pulses turn two current sources on and off as shown in Fig. 3.4. When both the UP and DN signals are high, the output current is zero. That is the charge pump does not respond to common mode changes in the UP/DN signals.

For positive phase errors the UP pulse goes high and a positive current pulse is generated by the charge pump. For negative phase errors the DN pulse goes high and a negative current pulse is injected into the loop filter.

The current pulses can be generated in in three ways as shown in Fig. 3.4. In the first two ways shown in Fig. 3.4(a) & (b), the current source is fully turned off when the UP/DN signals are zero. When any of the signals goes high, the current has to fully turn on to produce a current pulse proportional to the phase error. Thus the current pulses produced by the first two methods contain large current spikes in the current output as the current source has to fully turn on from an off state. The architecture shown in Fig. 3.4 c) 'steers' the current when the UP/DN signals are zero into a different path. Thus the current source is never fully turned off leading to a low feed through current injection into the loop filter when the UP/DN changes their levels. The charge pump implemented in our design is illustrated

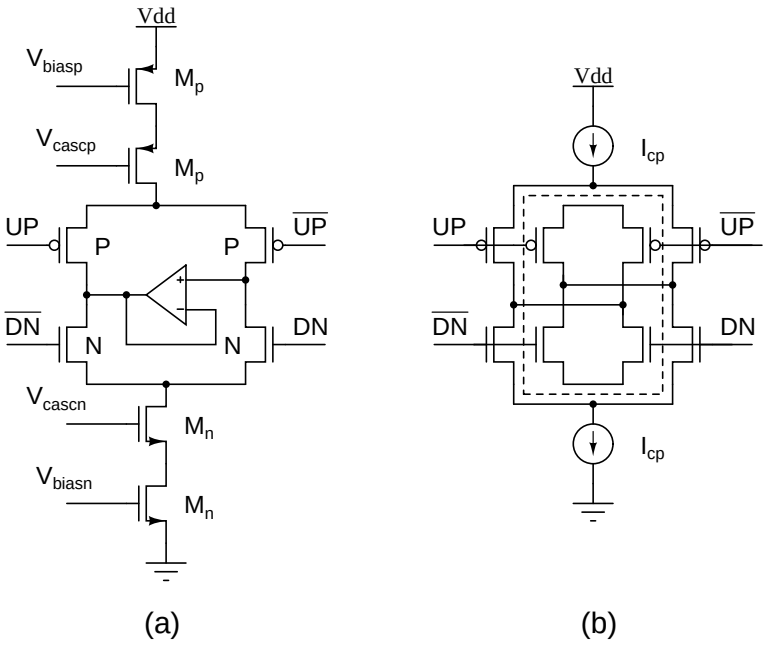

Figure 3.5: Charge pump implementation.

in the Fig. 3.5.(a), showing the bias devices and the switch configuration. The devices M_p, M_n are the bias devices that generate the desired UP and DN currents. The bias voltages that set the currents are derived using a bias generation circuit explained in the following section. Dummy devices are added to the switches

as shown in Fig. 3.5.(b) to reduce the feed through current injected during the transitions in the UP/DN signals. The unity gain follower shown in the Fig. 3.5 is used to maintain the same drain voltages of the switching NMOS and PMOS devices used for current steering. This reduces the errors injected due to drain voltage mismatch of the current steering devices. The schematic of the unity gain follower amplifier implemented as a two stage amplifier with miller compensation is shown in Fig. 3.6. The open loop gain and phase response of the amplifier is

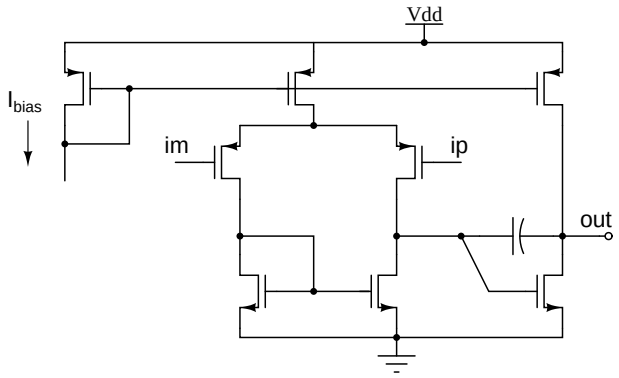

Figure 3.6: Amplifier used in the charge pump.

shown in Fig. 3.7. The UGB of the amplifier is 13.7 MHz and the phase margin is 84 degrees. The wide swing operation of the amplifier is tested by applying a

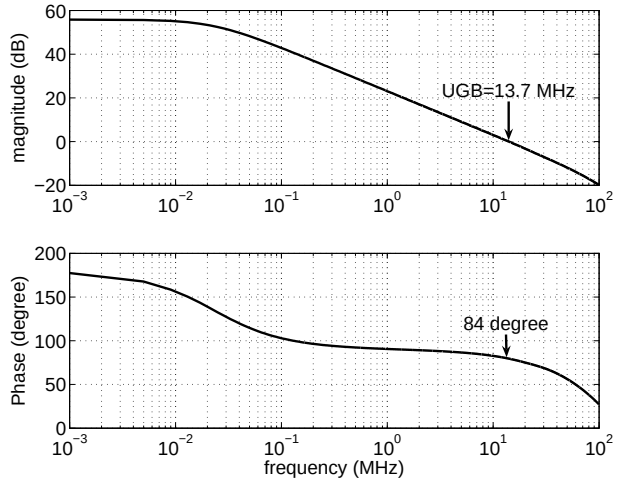

Figure 3.7: Magnitude and phase response of the unity gain amplifier used in the charge pump.

voltage ramp of slope 1.8 V/10 μs. As shown in the Fig. 3.8, the amplifier tracks the input for a range of 0 to 1.4 V. The saturation in the gain at high input voltages

occurs due to the PMOS input pair of the amplifier entering into the cut-off region. An important point to note is that the input pair enters cutoff region as the input voltage increases above $V_{dd} - |V_{D,sat}| - |V_{Tp}|$ and this results in the devices entering sub threshold region and for further increase in the input voltage to cutoff region[1]. From simulations without any mismatch in the input pair it was found that the input voltage tracks for a voltage range of 0 - 1.4 V as shown in Fig. 3.8.

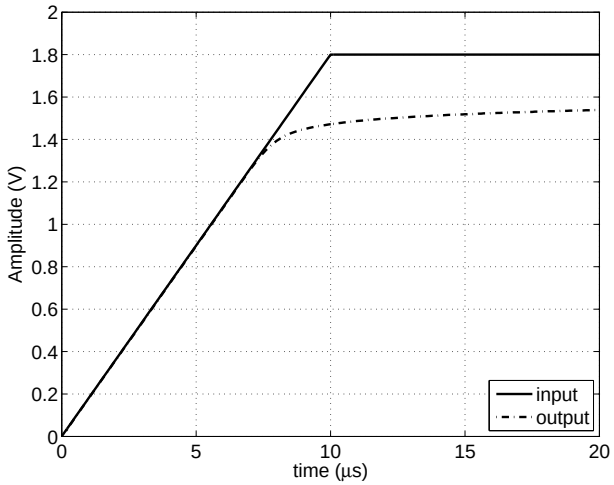

Figure 3.8: Transient simulation showing the wide swing operation of the amplifier.

3.3.2 Charge pump bias generation

An external voltage source ($V_r = 0.9$) is used to generate the UP current by using an amplifier in feedback as shown in Fig. 3.9. The generated UP current is $I_{up} = V_r/R = 56\mu A$. The UP current source, is then used to generate the DN current by a replica feedback mechanism as shown in Fig. 3.9, thus ensuring that the UP and DN currents are equal. The amplifiers used in the bias generation circuit are single stage differential to single ended converters with PMOS inputs.

The bias devices are sized with large lengths and hence proportionally larger width for a given G_m ($W = L = 2\mu$ for PMOS and $W = L = 4\mu$ for NMOS) to

[1]Though the gain and bandwidth reduce with increasing voltage level, the follower functionality does not have a significant impact on the PLL performance for such small variations between the input and output voltage.

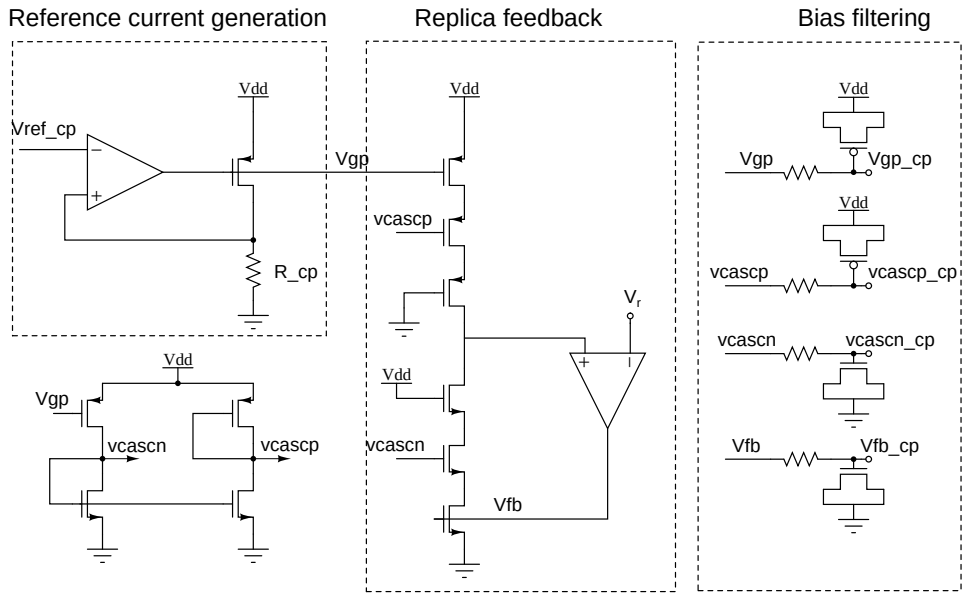

Figure 3.9: Charge pump bias generation circuit.

achieve the following benefits. Large area devices reduce the flicker noise contribution of the individual devices of the charge pump and also leads to a smaller V_T and $V_{ds}\,(\lambda)$ mismatch. Additionally it adds to the supply bypass capacitor that filters the supply noise and the noise from current mirroring devices.

3.4 Loop filter

The loop filter used in the PLL is the standard architecture with a proportional and integral path provided by a resistor (R) and capacitor (C_z) as shown in Fig. 3.10. The capacitor C_p is to reduce the fluctuations on the control voltage or to reduce the magnitude of the reference spur at the PLL output. The values of the resistor and capacitors are chosen based on the loop dynamics as explained in Chapter 1.

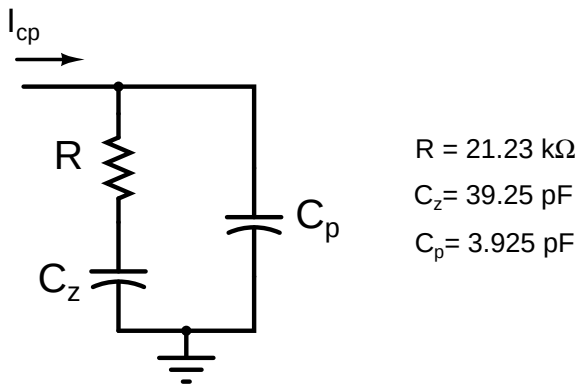

Figure 3.10: Loop filter architecture.

3.5 Pulse position randomizer and pulse repetition circuit

3.5.1 Randomization

The charge pump pulse position is randomized to spread the energy in the reference harmonics to all frequencies as described in Chapter 2. This randomization can be achieved by randomizing the UP/DN pulses that are fed as an input to the charge pump. The pulse position randomization is done in two steps.

- First the different delayed versions of the UP/DN pulses are generated using a chain of delay cells
- Next one of the delayed versions is chosen using a 8:1 multiplexer based on a 3-bit control word

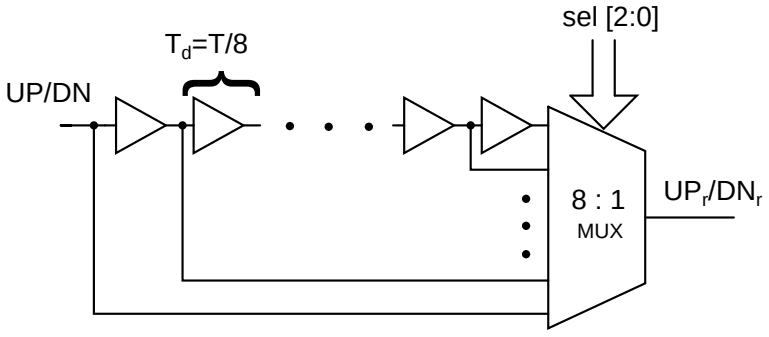

Figure 3.11: Pulse position randomizer.

Fig. 3.11 shows the pulse position randomizing circuit at a block level.

3.5.2 Delay cell

The delay cell is implemented as a chain of CMOS inverters. The desired delay is controlled by varying the supply voltage of the CMOS inverter. Fig. 3.12 shows

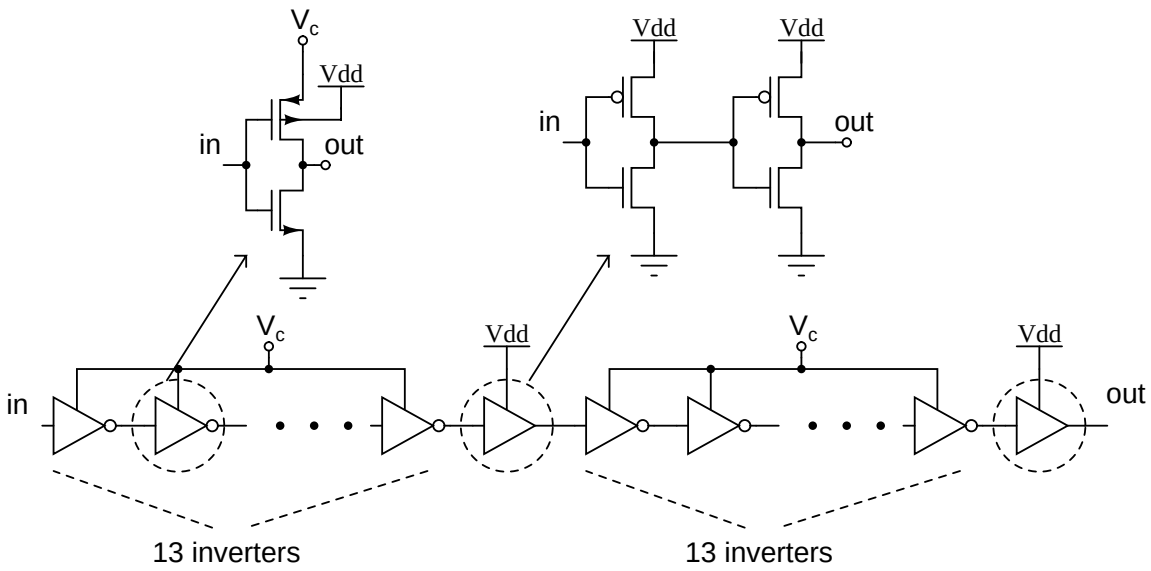

Figure 3.12: Delay cell implementation.

the schematic of the delay cell. The delay cells should be able to delay very narrow pulses of width ≈ 1 ns, which is the reset delay of the PFD. So the lengths of the delaying inverters should be chosen to ensure not only that the desired delay is met but also the narrow pulses should pass through them without being filtered out by the low pass nature of the delay cells. In the current work the length and widths were chosen through simulations such that they were able to allow narrow pulses of worst case width close to 0.8 ns. High speed buffers are inserted after the 13 cells to restore the pulses to a nearly rectangular shape.

3.5.3 8:1 Multiplexer

The 8:1 MUX is implemented by using 2:1 MUXs as shown in Fig. 3.13. Each 2:1 MUX is a set of switches with a driving inverter. The pass switches are implemented as transmission gate switches. The 2:1 MUX output is driven by an inverter, to reduce the load seen by the input to the 2:1 MUX.

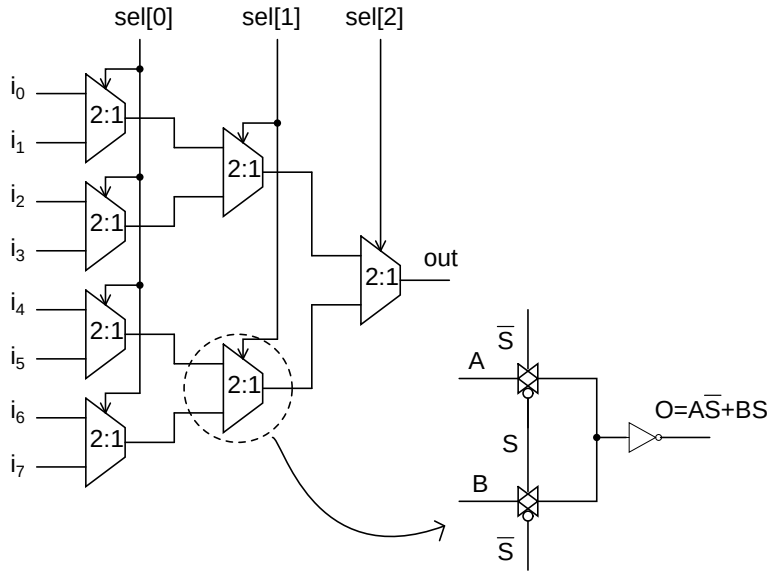

Figure 3.13: 8:1 Multiplexer.

3.5.4 Pulse repeating circuit

The pulse repetition is accomplished by passing delayed versions of the UP/DN signals through an 8-input OR gate as discussed in Chapter 2. The conceptual

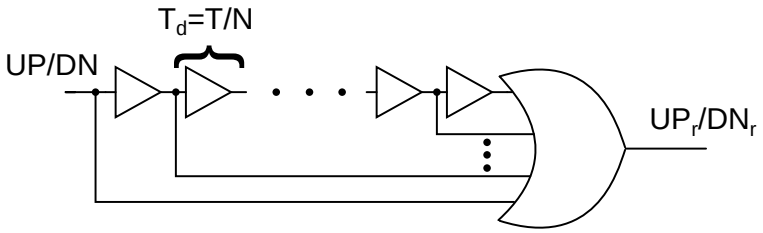

Figure 3.14: Pulse repeater.

schematic of the idea is shown in Fig. 3.14 for $N = 8$. To implement the 8-input OR gate for the pulse repetition technique, a pseudo NMOS logic is chosen over CMOS logic. In a CMOS implementation the PMOS devices form a series stack for the OR gate implementation and the NMOS devices are connected in parallel. Hence the discharging path of the output node is same for the different delayed pulses but the charging times are different for the different delayed versions. This generates a varying output pulse width for different delayed versions, introducing a periodic behaviour in the repeated pulse every reference cycle. Hence reference spurs appear at the output. A pseudo NMOS implementation ensures that the

charging and discharging paths are identical for all the delayed versions of the pulses and hence leads to a perfect pulse repetition. The schematic of the 8-input OR gate is shown in Fig. 3.15.

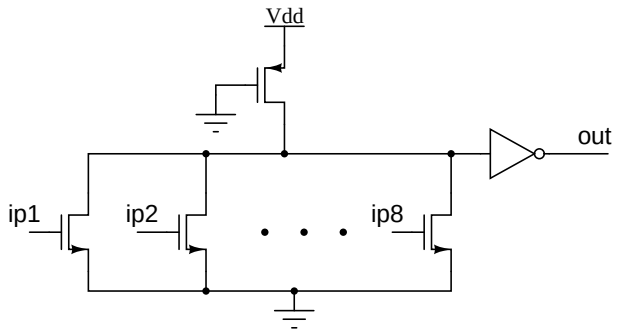

Figure 3.15: 8-input OR gate schematic.

3.6 Modulating sequence generation

For $N = 8$ we need a three bit random number to control the 8:1 MUX. For a PRBS of length L with an Linear feedback shift register (LFSR) structure, maximum length sequences can be generated by many combinations of taps which are summed and fed back to the first stage [13]. Once the length of the PRBS is chosen, the number of possible configurations (the taps whose outputs are summed and fed back to the first stage), varies with the length and all these configurations leads to a maximum length sequence. Simulations showed that the sequences generated by these different configurations were uncorrelated to each other and hence a binary summing of the output of three such maximum length sequence implementations produces three bit binary stream with a white spectrum. The different configurations of LFSR of length 15 used for the three bit random number is shown in Fig. 3.16. The PRBS is custom designed using CMOS logic.

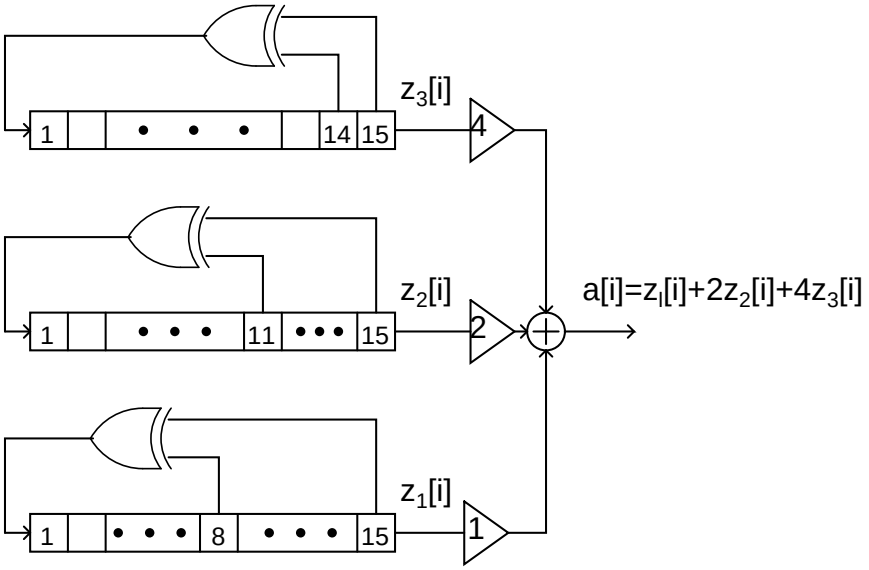

Figure 3.16: 3-bit random number generation.

3.7 Timing analysis for clocking the modulating signal

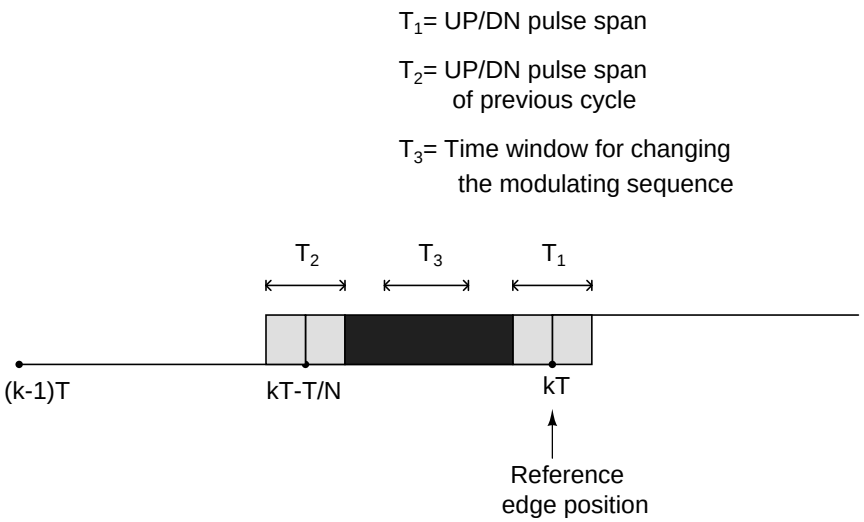

Figure 3.17: Figure showing the timing for the PRBS and the PLL.

The modulating sequence is changed every reference cycle and needs to be clocked appropriately to avoid any timing clashes with the UP/DN signals. In the steady state the UP/DN pulses appear close to the reference edge. If the divider edge leads the reference edge, the DN pulse appears before the reference edge and vice versa. The span of the UP/DN pulses is shown as T_1 in Fig. 3.17. In the previous cycle when a delay of $7T/N$ is selected, the UP/DN pulse can appear at $kT - T/N$

in the previous cycle. The span of the UP/DN pulses around $kT - T/N$ is shown as T_2 in the figure. Hence the modulating signal for the k^{th} reference cycle has to be changed in the time window between kT and $kT - T/N$ as shown in Fig. 3.17. This ensures that the change in the select signal for the k^{th} cycle does not conflict with the timing of the UP/DN pulses of the current and previous cycle. So the reference clock is fed to the PRBS first and a delayed version (delayed by 2.5 ns) is fed to the PFD in the PLL.

3.8 Voltage controlled oscillator

Ring oscillators are known for their easy integration and wide tuning range in CMOS processes. LC oscillators are known for very good phase noise performance, but the inductors occupy very large area and need extensive additional work to model, design and layout them. Thus a ring oscillator based VCO is chosen for implementation in the current work.

A n-stage ring oscillator is formed by a cascade of n single pole amplifiers with the final output negatively fed back to the input of the first stage amplifier. For a given frequency of oscillation and a phase noise specification, the area and the power dissipated is independent of the number of stages in the oscillator (explained in Appendix B). A three stage ring oscillator is chosen in the current work for implementation for simplicity.

3.8.1 Delay cell

A fully differential three stage ring oscillator is chosen as the VCO for the PLL due to its immunity to common mode noise sources like the supply noise. The differential delay cell has NMOS inputs and a diode connected PMOS load as shown in Fig. 3.18. The minimum supply voltage necessary for the operation of

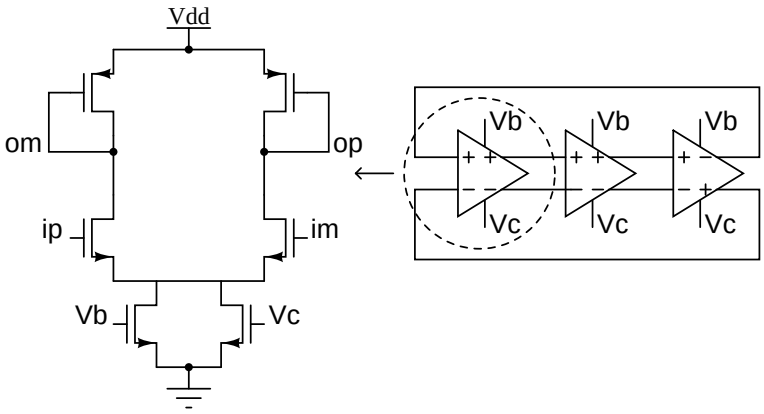

Figure 3.18: Basic VCO cell.

the delay cell is

$$V_{dd,min} = V_{ovp} + V_{ovn} + V_{Tn} + |V_{Tp}| + V_{ovt}$$

where V_{ovp}, V_{ovn} and V_{ovt} are the overdrive voltages of the PMOS load, NMOS input and the NMOS tail transistors of the delay cell. The lengths of the devices are chosen to meet the desired range of frequency of oscillation.

Having a large overdrive improves the phase noise performance of the VCO as it reduces the noise contributed by the individual devices. To achieve a good phase noise, the overdrives of the devices used in the delay cell and the tail current sources needs to be higher but it demands a large supply voltage. In order to resolve this we can go for a delay cell with linear region MOS resistor loads, where the drop across the device can be reduced significantly as it operates in linear region. But this method would need an additional bias generation circuit to set the desired gate voltage for the linear region MOS load, which adds additional phase noise to the VCO. Hence we traded the linear region load with a diode connected load operating at a supply voltage of 2.2 V, to reduce the phase noise and the implementation complexity of the delay cell.

3.8.2 Tuning circuit

The tuning of the VCO is accomplished by changing the current I_{vco} of the delay cell proportional to the control voltage of the VCO. The functional diagram of the tuning circuit is shown in Fig. 3.19. The VCO current of a single delay cell is

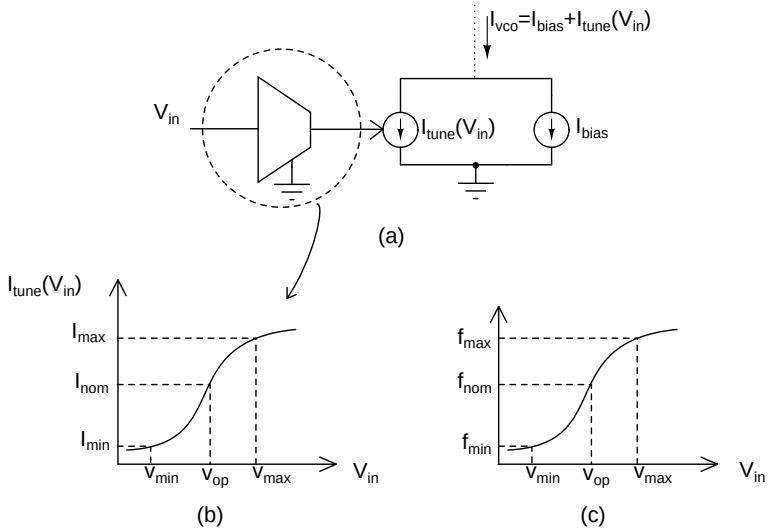

Figure 3.19: (a) VCO tuning circuit, (b) I-V characteristics of the V-I converter, (c) The resulting f-V characteristics of the VCO.

given by

$$I_{vco} = I_{bias} + I_{tune}(V_{in})$$

The tuning current and the bias current are selected to get the desired VCO characteristics. The tuning current is given by

$$I_{tune}(V_{in}) = G_m V_{in}$$

Since we need to generate a tuning current proportional to the control voltage, the tuning circuit is nothing but a trans-conductor. To achieve a wide tuning range, we need a linear transconductor operating over a wide input range. The VCO needs to have a tuning range of 0.3 - 1.5 V, which implies that the transconductors should have an operating range of 1.2 V (symmetric about 0.9 V). Assuming a simple NMOS or PMOS differential pair the linear range (range over which the current

fully switches to another pair) is approximately

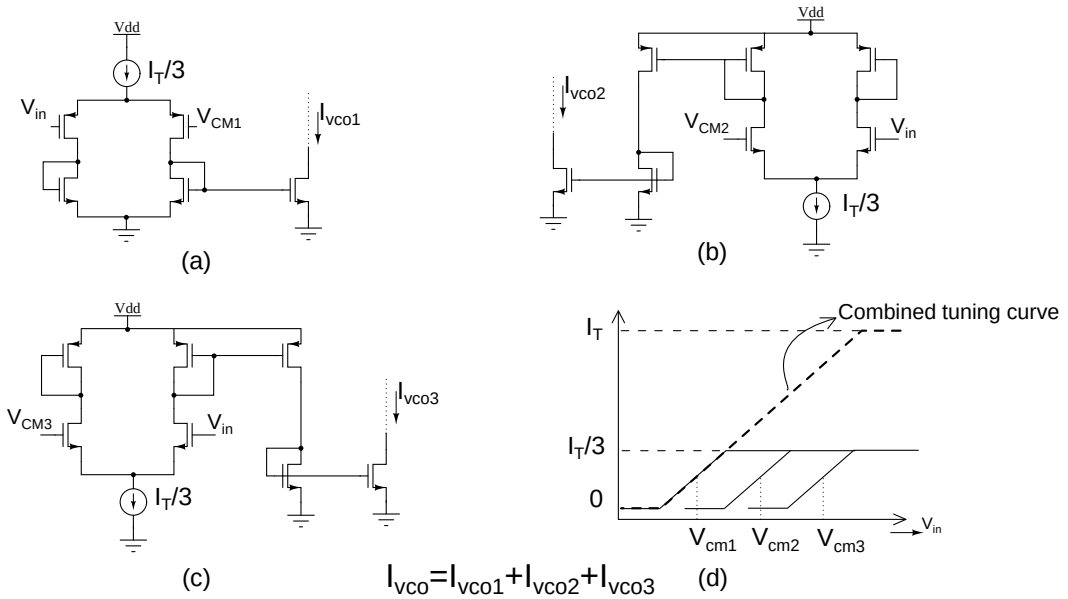

Figure 3.20: Stagger tuned VCO. Transconductance cells active in the range (a) 0.3 - 0.7 V, (b) 0.7 - 1.1 V, (c) 1.1 - 1.5 V, (d) Staggered transconductor I-V characteristics.

$$V_{rg} = 2\sqrt{2}(V_{gs} - V_T)$$

where $V_{gs} - V_T$ is the overdrive of the input pair in the quiescent condition. Since the linear range requirement is 1.2 V, we have

$$(V_{gs} - V_T) \geq 0.43V$$

So to have a wide tuning range, a single transconductor should have an overdrive of at least 0.43 V for the input pair and hence a V_{gs} of approximately 0.85 volts (for a worst case V_T of 400 mV in 0.18 μm CMOS process). Since we want the characteristics to be symmetric around 0.9 V, the transconductor will not be able to provide a wide tuning range and linearity due to voltage headroom problems.
To resolve this we use a staggered transconductor whose I-V characteristic is shown in Fig. 3.20 (d). The three transconductors are staggered at 0.5 V, 0.9 V and 1.3 V, with a range of 0.4 V per transconductor cell. The overdrives per stage of the staggered transconductors are reduced to 0.141 V, relaxing the headroom requirement

of the transconductors. Thus it covers the entire VCO tuning range of 0.3 V to 1.5 V and provides high linearity. The first transconductor with a 0.5 V common mode uses a PMOS input pair for voltage headroom reasons and the other two transconductors have NMOS inputs with common mode voltages of 0.9 V and 1.3 V as shown in Fig. 3.20.(a), (b), (c). The simulated tuning characteristic of the staggered G_m cell is shown across corners at a temperature of 27^0C in Fig. 3.21. The VCO does not have any amplitude control loop, as the amplitude variation

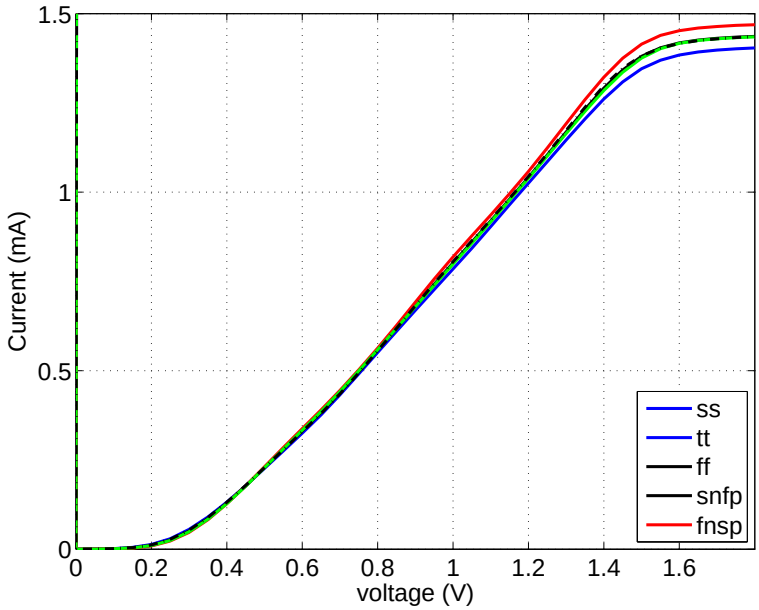

Figure 3.21: Tuning current vs input voltage.

across corners was less than 20 %. The nominal value of the maximum tuning current I_T per cell is 1.44 mA and the bias current for a nominal setting is 1.2 mA. The VCO is simulated at a transistor level with extracted layout parasitics in the nominal corner. Figure 3.22 shows the VCO tuning characteristics. The gain of the VCO is $\approx$ 300 MHz/V.

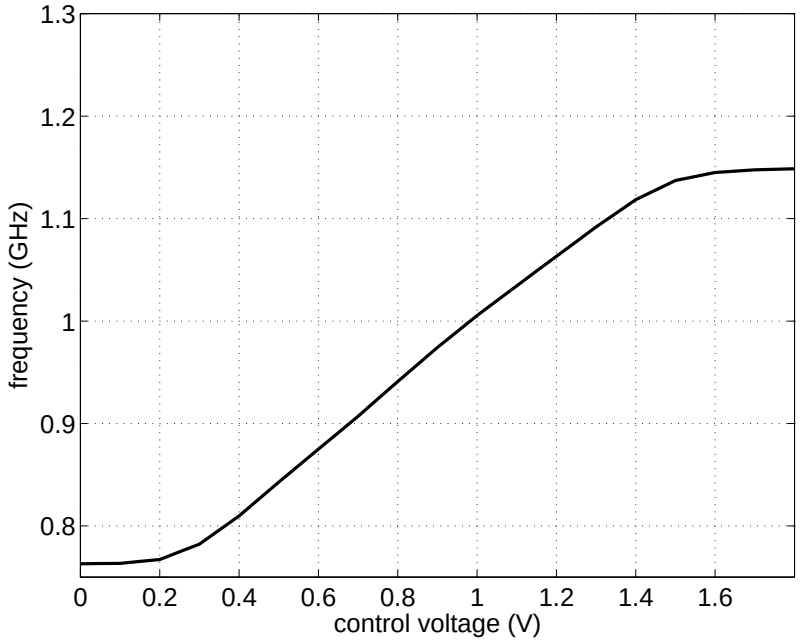

Figure 3.22: VCO characteristics measured at the nominal corner.

3.9 Frequency divider

3.9.1 Multi-modulus dividers

Multi-modulus dividers form the basic building block for the frequency synthesizers which require programmable divide value. A promising architecture for implementing multi-modulus dividers is to use a cascade of 2/3 modulus dividers as shown in Fig. 3.23. This type of dividers built using 2/3 modulus dividers are known for their modular nature and wide-range programmability without any feedback loops around large chain of flip-flops [16]. Owing to their asynchronous nature they are also more power efficient. Thus they have become the de-facto choice for programmable frequency division in PLLs and frequency synthesizers. The programmable divide value is selected using the l-bit select signal $[P_0 : P_{l-1}]$. The 2/3 dual modulus dividers divide the input signal frequency by two or three based on the select signal and the *mod* signal fed to every stage from the preceding stage as shown in Fig. 3.23. The cascaded 2/3 architecture generates a *mod* signal which propagates from the last stage to the first stage as shown in Fig. 3.23. For

every output clock cycle of the divider, the *mod* signals of all the stages goes high once. The ON-time of the *mod* pulse of the i^{th} stage in the divider is equal to the time period of the i^{th} divider's output. For instance the ON-time of the last stage *mod* signal is one divider output clock cycle (hence it is always ON every cycle), the stage before that has a *mod* value of 1 for half the output clock cycle and so on till the first stage which has an ON time for the mod_0 signal to be 1 clock cycle of its output (which is VCO output divided by 2, $2T_{vco}$). When both the select signal P_i and the *mod* signal are simultaneously high, the 2/3 modulus divider counts three cycles of the input signal, otherwise it counts two cycles of the input signal. Thus when all the P_i are logic high, all the 2/3 cells count three input cycles once per divider output period. The final divide value (total number of counted cycles) at the output is given by

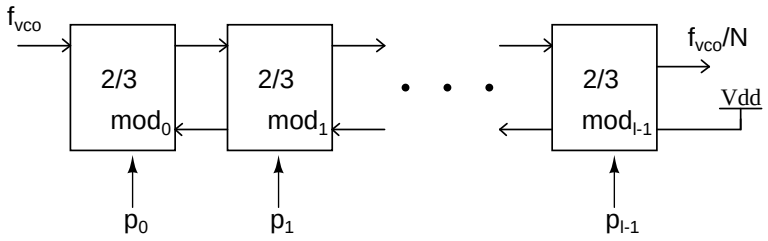

Figure 3.23: A multi-modulus divider formed using 2/3 modulus dividers.

$$N = 2^l + [P_0 + 2P_1 + ... + 2^{l-1}P_{l-1}] \tag{3.1}$$

$$N = 2^l + \sum_{i=0}^{l-1} 2^i P_i \tag{3.2}$$

Thus for a l stage dual modulus divider the divide value is in the range $[2^l, 2^{l+1} - 1]$. The nominal VCO output frequency is 1 GHz and the reference frequency is 20 MHz. Thus the nominal divide value is 50. To achieve this we need at least five 2/3 modulus divider stages. With five stages, the division ratio lies in the range $[32, 63]$.

The 2/3 modulus divider architecture used in the divider is shown in Fig. 3.24. The input to the divider is the VCO output running at a frequency of 1 GHz. It is

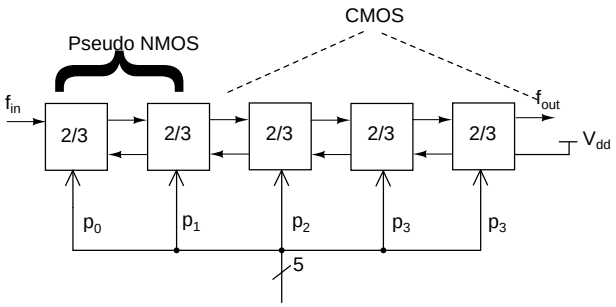

Figure 3.24: Divider architecture.

well known that in a given CMOS technology pseudo NMOS logic is always faster than CMOS logic. Thus we opted to use pseudo NMOS logic for the first two stages that operate at 1-1.5 GHz even if it is not power optimal (A current mode logic (CML) could have been used for the initial stages to save power, however the CML logic has a large number of devices stacked from supply to ground demanding a large supply voltage for a low input sensitivity[2] or wide output swing. Hence we chose pseudo NMOS for the initial stages). The rest of the logic in the divide chain is CMOS. The divide by 2/3 section of the multi-modulus divider is shown

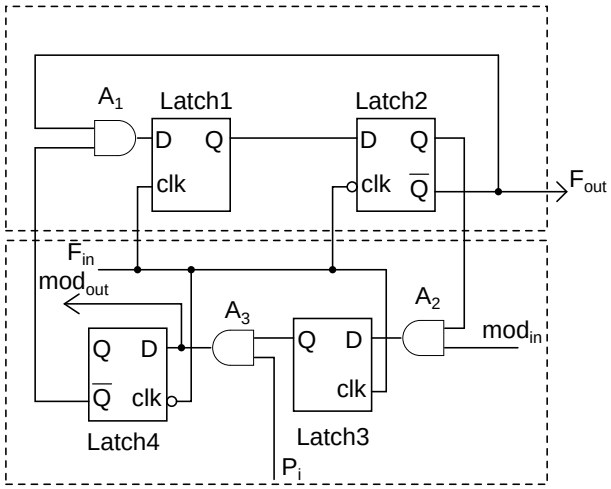

Figure 3.25: Divide by 2/3 section shown at gate level

at a gate level in Fig. 3.25. When either mod_{in} or P_i signal is low, one of the input to the AND gate A1 is always high and hence the 2/3 section behaves as a divide

[2]A low input sensitivity here means the smallest input signal that can be applied to the divider. A smaller input signal demands a larger gain for the sampling stage in the divider, which in turn implies a larger G_m or load resistor. In order not to increase the noise, to increase the gain, the G_m is increased fixing the resistor which leads to an increased drop across the resistor and demands a larger supply voltage

by 2 circuit. When both mod_{in} and P_i signals are high, the 2/3 section behaves as a divide by 3 circuit [16].

The latches in the 2/3 section are implemented in a fully differential pseudo

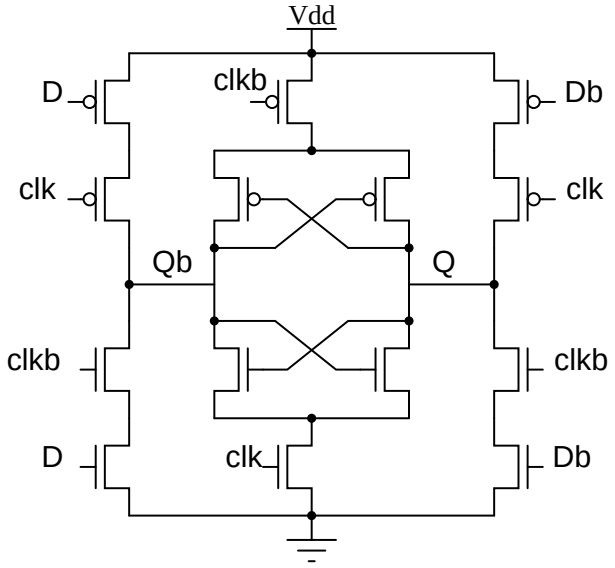

Figure 3.26: CMOS latch.

NMOS logic for the first two stages as they operate at the highest frequency in the divide chain. The 2/3 section consists of D-latches and 'AND' gates. The latch is implemented as a positive level triggered latch which samples on clkb and holds (latches) it on clk. The latches which have an ANDed input can be combined

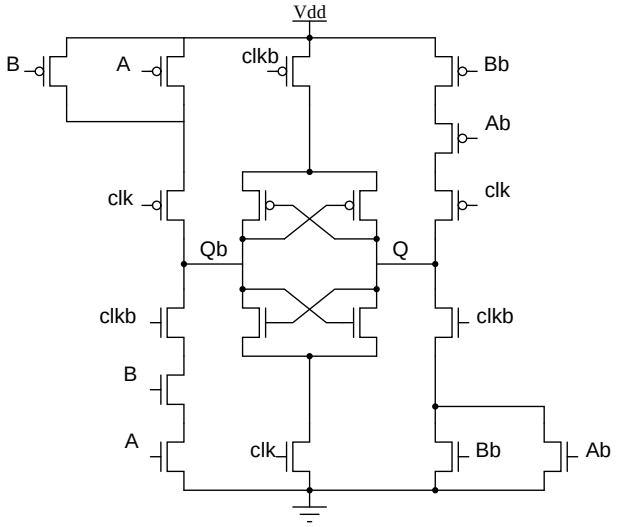

Figure 3.27: CMOS latch with AND functionality combined.

into a single stage latch with AND functionality merged into it. Fig. 3.26 shows the

architecture of the differential CMOS latch used in the design. The CMOS Latch combined with the AND gate functionality is shown in Fig. 3.27. The architecture of the pseudo NMOS logic latch of the first two stages is also similar to the CMOS latch except the complementary PMOS load is replaced by a simple PMOS linear region load. The schematic of the pseudo NMOS latch and the ANDed pseudo NMOS latch are shown in Fig. 3.28.

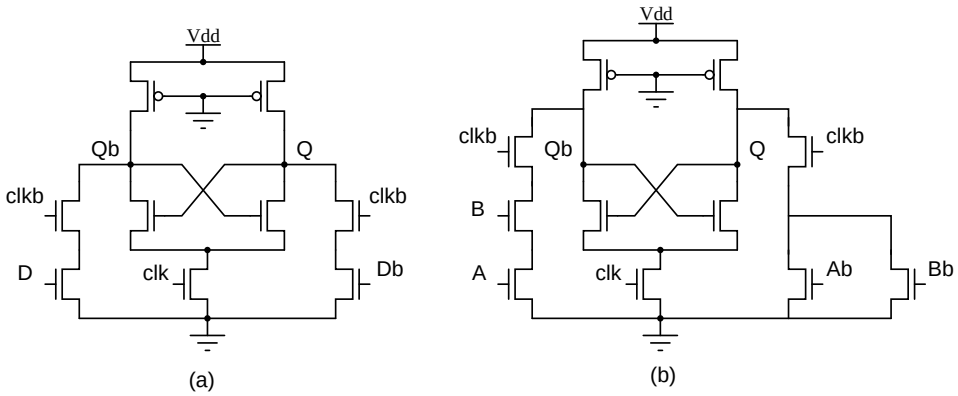

Figure 3.28: (a) Pseudo NMOS latch and (b) ANDed pseudo NMOS latch shown at a transistor level.

3.9.2 Programmable divide value

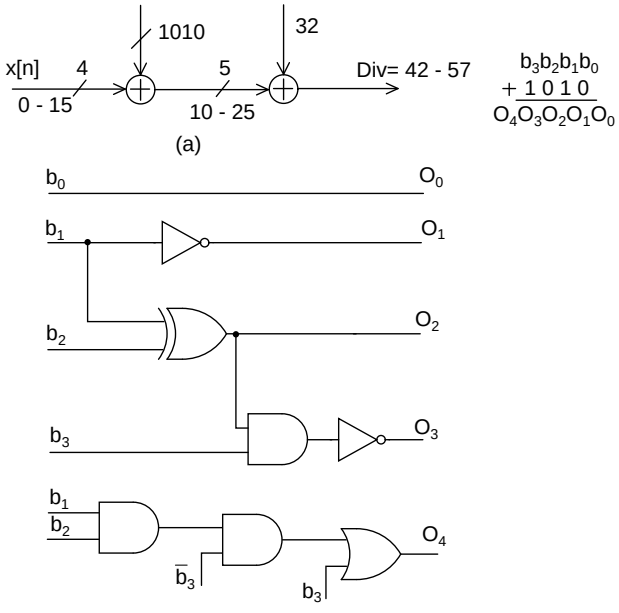

Figure 3.29: Divider encoder logic.

The VCO has a tuning range of 1.2 V, which corresponds to a frequency range of $1.2K_{vco} = 360\,MHz = 18f_r$. Since it is an integer N PLL, to cover the entire range of the VCO we need a divide value that is programmable up to 18 values in steps of one. Though the implemented divider provides a five bit control (32 values), only 18 values is necessary to get the desired divide value. Using a five bit control results in a large division range being unused, hence the programmability range was reduced to 16 values and a four bit control was used[3]. Maintaining the divide value of 50 corresponding to the nominal output frequency of 1 GHz as the center, the desired division ratio is in the range 42 - 57.

To obtain the desired divide value, the 5-stage dual modulus divider needs a five bit control signal in the range 10 - 25. To the external four bit control word, 1010 is added using a four bit full adder with carry. This results in a five bit control word between 10 and 25, necessary to control the programmable divider.

Since the one of inputs to the adder is always constant (1010 in our case), we use this to minimize the complexity of the adder. Let $b_3b_2b_1b_0$ be the input data stream and $O_4O_3O_2O_1O_0$ be the five bit output of the adder as shown in Fig. 3.29. Then with some simple Boolean algebra we arrive at

$$O_0 = b_0$$

$$O_1 = \overline{b_1}$$

$$O_2 = b_1 \oplus b_2$$

$$O_3 = \overline{b_3 \oplus (b_1 b_2)}$$

$$O_4 = b_3 + b_1 b_2 \overline{b_3}$$

The encoder used for the division ration selection is given in Fig. 3.29.

Simulations were carried out on the extracted view of the divider in the slow corner[4]. The simulated waveforms of the divider for an input of 1 GHz (1 ns time

[3]This results in a reduction of the VCO output frequency range by $(18 - 16)f_r = 2{\cdot}f_r = 40\,MHz$.

[4]The simulations are performed in slow corner, since the divider is prone to malfunction at this corner due to slower speeds of the initial stage dividers. Ensuring an accurate operation at

period) of peak-to-peak amplitude 200 mV and a select value for the divider to be $b_0b_1d_2b_3 = 1111$ (which corresponds to a divide value of 57) are shown in Fig. 3.30.

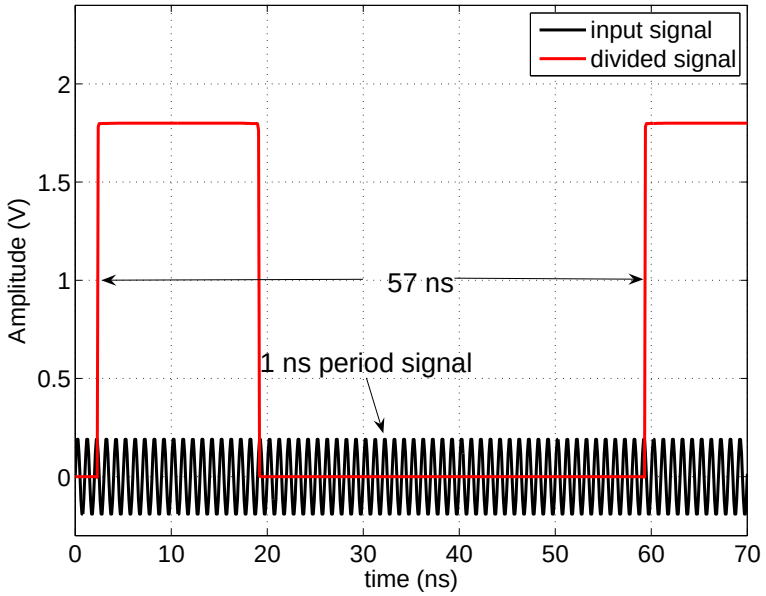

Figure 3.30: Divider waveforms overlaid with the VCO waveform.

3.10 Buffers

3.10.1 Control voltage buffer

The control voltage output is probed to study the settling performance of the PLL. To minimize the noise introduced on the control voltage by the probing path, we use a unity gain follower to buffer and shield the control voltage from the external noise sources. The buffer needs to have wide input operating range from 0.3 V to 1.5 V and unity gain bandwidth $>$ 1 MHz. A simple way to accomplish a wide swing operation is to connect a differential to single ended amplifier with PMOS input pair in parallel with a differential to single ended amplifier with NMOS inputs as shown in Fig. 3.31. For lower input voltages ($v_{in} < 0.5\,V$) the

this corner would automatically ensure the correct operations at other corners as well.

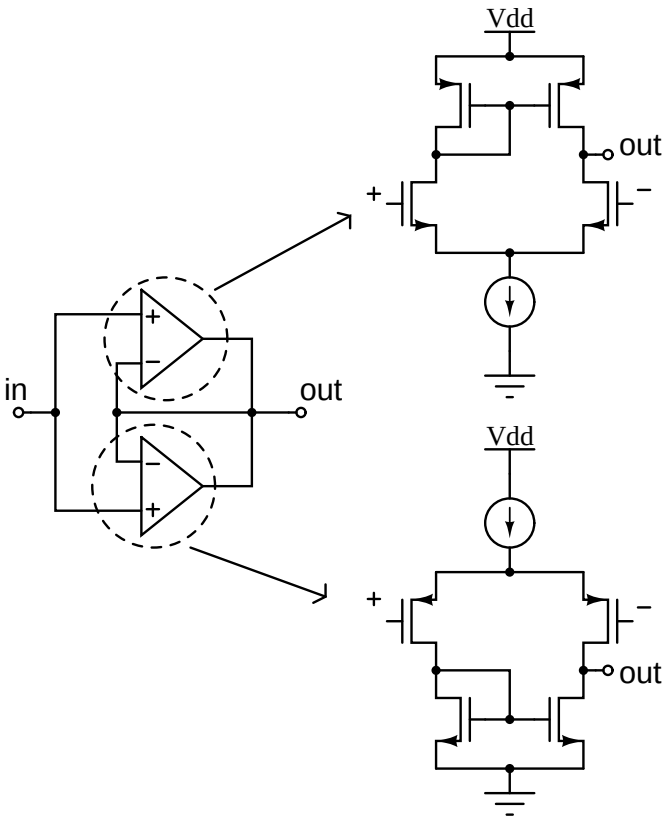

Figure 3.31: Control voltage buffer schematic.

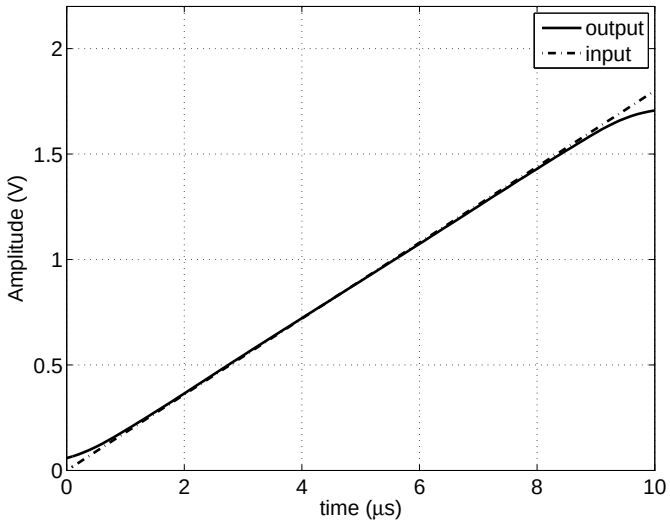

Figure 3.32: Transient response of the control voltage buffer.

amplifier with PMOS inputs is active and for input voltages greater than 1.2 V the amplifier with the NMOS input pair is active. For voltages near the common mode voltage (0.9 V), both the amplifiers are active and the gain is maximum as devices in both the amplifiers are in the active region of operation. The transient response of the amplifier for a slow voltage ramp with a slope of 1.8 V/μs.

3.10.2 VCO buffer

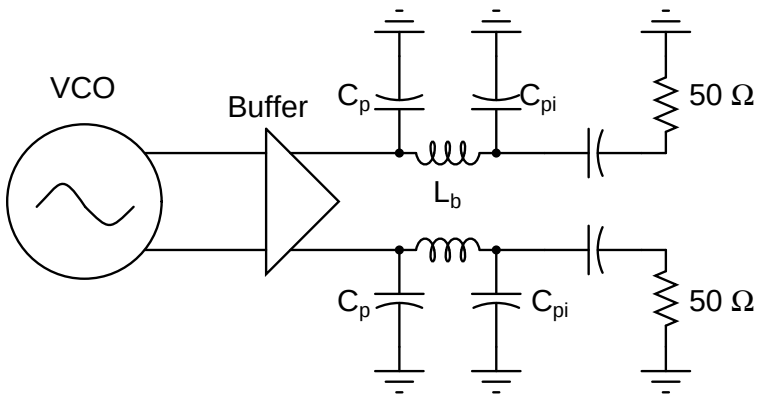

Figure 3.33: Buffered VCO output driving the bond pad, pin and a 50 Ω resistor.

The VCO buffer serves as an interface to bring the VCO output on chip to the external world for phase noise measurements. The circuit model of the VCO buffer being taken out for measurement to a 50 Ω resistor load is shown in Fig. 3.33. The figure shows the VCO buffer driving the bond pad modeled as a capacitor C_p, bond wire modeled as an inductor L_b, the output pin modeled as a capacitor C_{pi}. The output pin is capacitively coupled to a measuring device (Spectrum analyzer) modeled as a 50 Ω load resistor. The VCO buffer is implemented in current mode logic (CML) with resistive loads as a tapered buffer architecture shown in Fig. 3.34. The total power consumed by the VCO buffer is 10.8 mA. For a bond pad capacitor value of 1.5 pF, bond wire inductance of 2 nH and a pin capacitor of 3 pF, the simulated peak to peak differential output voltage delivered to the 50 Ω load resistor is 450 mV.

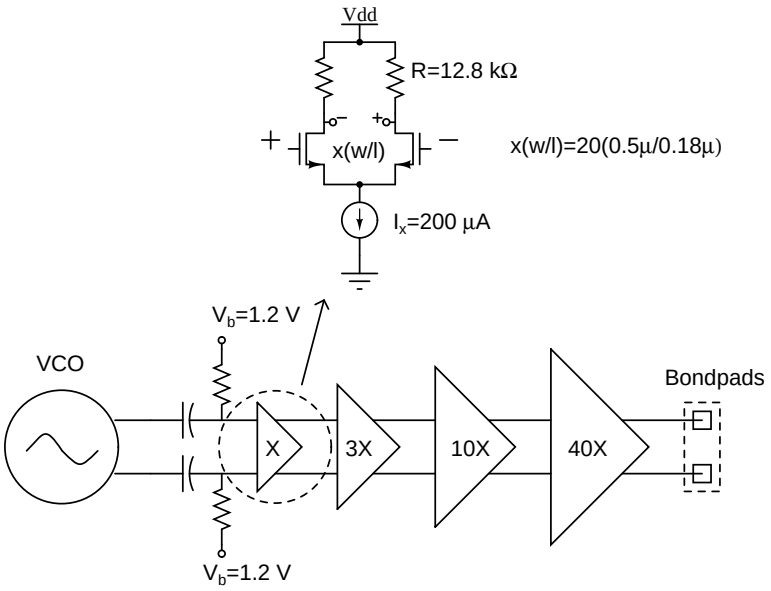

Figure 3.34: VCO buffer schematic.

3.11 Lock detector circuit

A lock detector is implemented to detect and disable[5] the randomization logic when the phase errors exceed $\delta T > T/N = 6.25\,\text{ns}$. The phase lock detection circuit was implemented by exploiting the fact that the inverters behave as a low pass filter. The phase error is first generated by feeding the UP and DN signal to an XOR gate. This produces a pulse whose width is proportional to the magnitude of the phase error between the reference and divide clocks. The resulting error pulse is passed through a series of inverters with long device lengths followed by a high speed inverter. This is equivalent to passing the pulse through a lowpass filter followed by a slicer as shown in Fig. 3.35.(a). So when the pulse widths are larger than a threshold value, the pulse is passed through the inverters and it appears at the slicer output, and for small pulse widths the lowpass filter attenuates its amplitude and the slicer detects it as a zero. The inverter lengths are chosen such that they allow pulses of width greater than $9\,ns$ (in the nominal corner) which is a condition indicating the PLL is out of lock.

[5]Though not implemented in the current design, the lock detector can also be used to disable the PR technique when the phase errors are large enough to affect the PLL dynamics.

When the pulse appears at the slicer output we set the 'lock det' signal high.

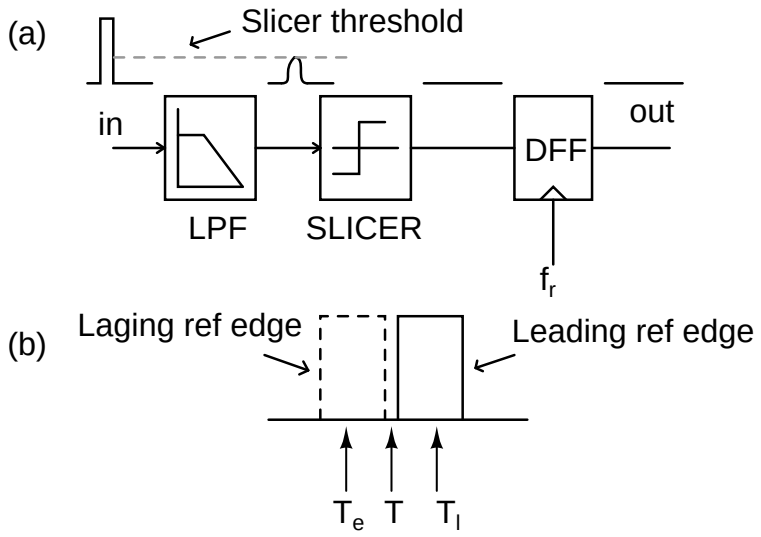

Figure 3.35: (a) Idea behind the 'Phase lock' detector implementation, (b) Figure showing the sampling instants T_e and T_l w.r to the rising edge of the reference clock.

This can be accomplished by sampling the output of the slicer using the reference clock signal. If the reference clock leads the divide clock, the pulse would appear after the reference edge and when the divide edge leads the reference edge, the pulse would appear before the reference edge. So to sample the pulse we use an 'early-late sampling'. We use a delayed version of the reference clock to sample the pulse when the reference clock leads the divide clock and an advanced (early) version of the reference clock when it lags the divide clock. The sampling instants of the delayed (T_l) and the early (T_e) clocks are shown in Fig. 3.35.(b) along with the possible error pulses.

The gate level schematic of the lock detector is shown in Fig. 3.36 with the dimensions of the inverters used for lowpass filtering and slicer operations. The D-Flip flops are implemented in a master and slave configuration using level triggered CMOS latches. The transfer characteristics of the implemented lock detector (simulated on the extracted view) is shown in Fig. 3.37.

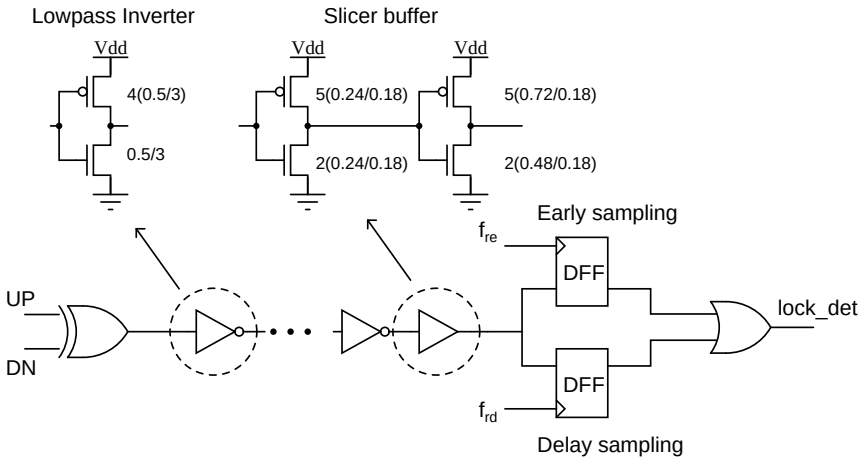

Figure 3.36: 'Phase lock' detector schematic.

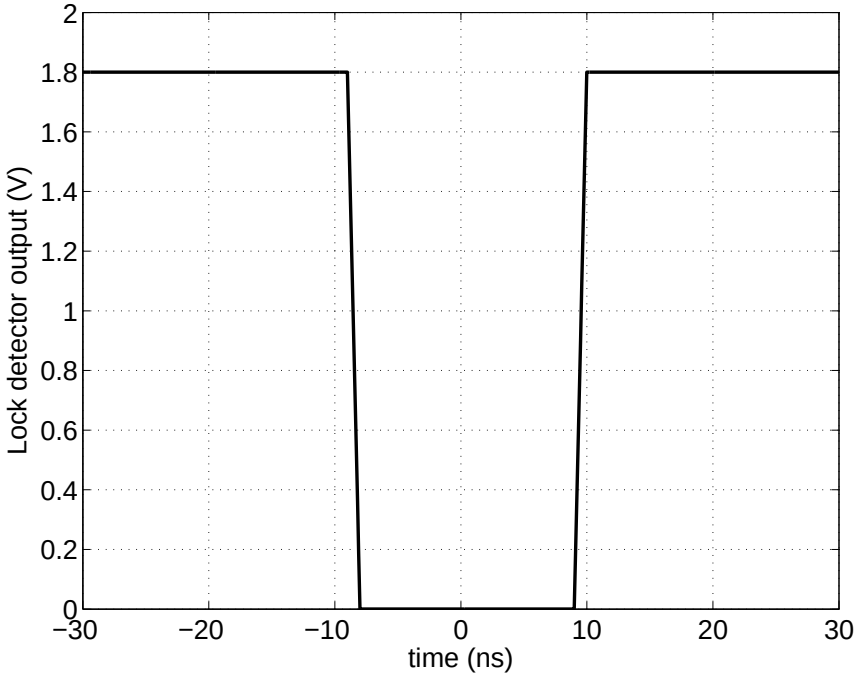

Figure 3.37: 'Phase lock' detector characteristics.

CHAPTER 4

Delay tuning PLL

The delays are implemented using CMOS inverters and are prone to process and temperature variations. One straightforward approach to counter the delay variations is to use a replica delay locked loop (DLL), where a voltage controlled delay line is used in a feedback loop which ensures that the delay is equal to one reference clock period. However there are two problems associated with this approach. First, in the presence of nonidealities like charge pump feedthrough and mismatch, the DLL will finally settle such that there is a finite phase offset between the DLL output and the input clock, which implies that the delay attained is not exactly one reference period. Second, the DLL has the problem of locking to integer multiples of reference period in the steady state.

An alternative is to configure (one half of) the delay line as a voltage controlled ring oscillator and tune its oscillating frequency to a fixed reference frequency using a PLL. Though there may be finite phase offsets between the VCO output and the input reference clock, the frequency is perfectly tracked. Hence the time period of the VCO is exactly equal to the reference clock period, $T_{vco} = T_i$. T_i is the time period of the input reference clock. When the inverter chain in the ring oscillator is used a delay line, the delay value generated is exactly tuned to the desired value without the afore-mentioned problems associated with the DLL based tuning. Therefore a PLL based delay tuning is chosen for delay tracking across process and temperature corners.

4.1 Delay tuning PLL dynamics

Fig. 4.1 shows the schematic of the PLL used for delay tuning. The PLL employs a dual path for phase error, the first proportional path [1] is provided by the resistor R and charge pump CP1 with current I_{cp1} and the second proportional path is provided by charge pump CP2 with current I_{cp2} as shown in the figure. The

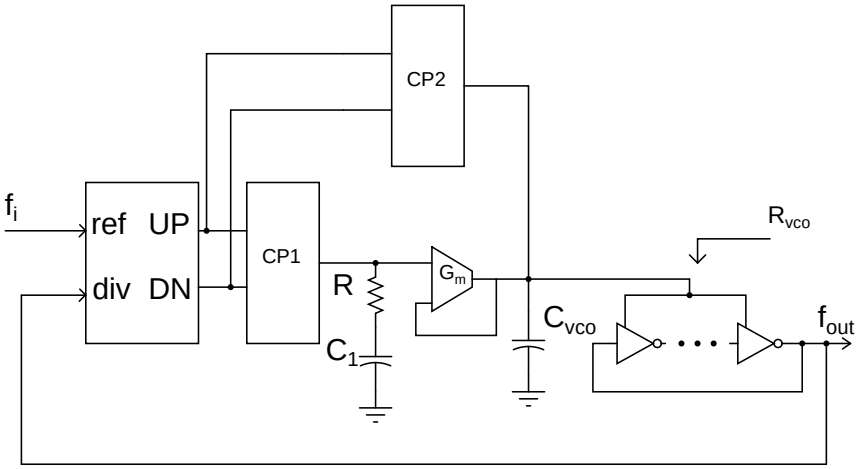

Figure 4.1: Supply regulated PLL for Delay tuning

integral path for the error is provided by the capacitor C_1. The PLL employs a ring oscillator as its VCO and in the steady state the VCO time period will be equal to the input reference period and the delay cells used in the VCO behave as a delay line with delay equal to $T_i/2$. These delay cells are replicated and used in the design to get the desired delays required for spur elimination. The loop gain $LG(s)$ of the PLL is given by

$$LG(s) = \frac{I_{cp1}K_{gm}K_{vco}(1+\frac{s}{\omega_z})}{s^2C_1(1+\frac{s}{\omega_p})} \tag{4.1}$$

$$\begin{aligned} \omega_z &= \frac{G_m}{(a_1+G_mR)C_1} \\ \omega_p &= \frac{G_m+G_{vco}}{C_{vco}} \end{aligned}$$

where $K_{gm} = \dfrac{G_m R_{vco}}{1 + G_m R_{vco}}$, $a_1 = I_{cp2}/I_{cp1}$. The transconductance amplifier G_m has to drive the ring oscillator and hence needs to provide the current required by the oscillator. The bias current of the transconductor has to be much higher than the current drawn by the ring oscillator and hence a simple differential to single ended amplifier cannot be used a transconductor due to voltage headroom requirements despite its good supply rejection characteristics [17]. This mandates a two stage amplifier which needs to be miller compensated for stability requirements as the second stage sees a large load capacitor C_{vco} chosen for better supply noise rejection. Adding a two stage amplifier for the transconductor introduces additional pole within the PLL loop and thereby affects the stability margin. We can also see from the above equations of loop dynamics, that the G_m of the transconductor not only determines the pole location, but also the loop gain (K_{gm}). In order to decouple the dual functions of providing the DC gain and the VCO current, we use the technique of current assistance for the transconductor.

The conceptual schematic of the current assisted transconductor is shown in Fig. 4.2. A pre-estimated current (I_{vco}) is injected into the VCO as shown in

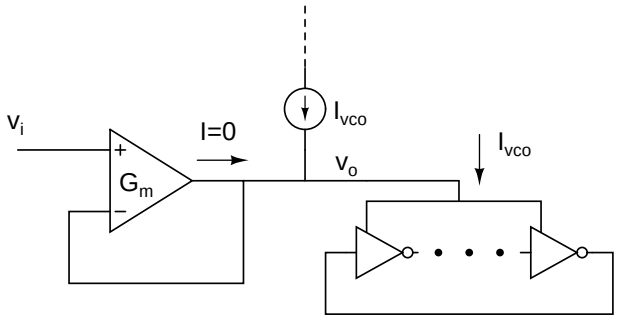

Figure 4.2: Transconductor with Current Assistance

the figure. This relaxes the transconductor current specifications as it has to supply zero current to the VCO and thus only maintain $v_i = v_o$ by its feedback action. The current can be estimated and pumped into the VCO in two different ways. The first method is named as the feedback method and the second as the feedforward method.

4.1.1 Feedback compensation

Illustrated in the figure 4.3 is the feedback method. A replica VCO (main VCO scaled down by n) is separately driven by an amplifier and the current that is fed by the PMOS pass transistor is multiplied by n and mirrored to the VCO. The advantage can be seen by the fact that the current estimating loop sees a lower capacitor at its second stage due to the load scaling operation. The equations that

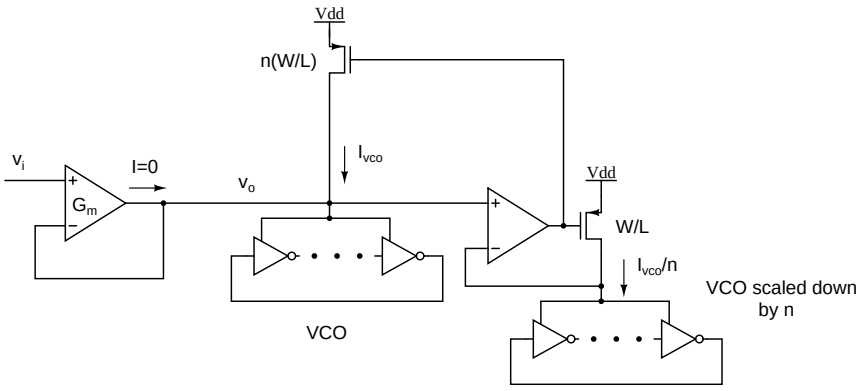

Figure 4.3: The proposed idea to make the G_m independent of the VCO load by feedback replica current injection.

represent the dynamics in the feedback compensation are

$$G_m.v_i(t) = G_m.v_o(t) + v_o(t)[G_{vco}(t) - G_{fb}(t)] + C_{vco}\frac{dv_o(t)}{dt} \tag{4.2}$$

Since the VCO draws a time varying periodic current, the load offered by the VCO is modeled as a time varying transconductance $G_{vco}(t)$. $G_{fb}(t)$ is the estimated time varying feedback current injected into the VCO. When $G_{fb}(t) = G_{vco}(t)$, we have

$$v_i(t) = v_o(t) + \frac{C_{vco}}{G_m}\frac{dv_o(t)}{dt} \tag{4.3}$$

Applying the Laplace transform to Eq. 4.3, we get

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{1 + \frac{sC_{vco}}{G_m}}$$

The above equation shows that the DC gain is 1 (independent of G_m) and the pole is located at G_m/C_{vco}.

4.1.2 Feedforward compensation

Another method is to use a feed forward current injection as shown in Fig. 4.4. The VCO current is estimated in a similar manner by using the input voltage as shown in the figure. The equation for the dynamics of the PLL in the feed-forward

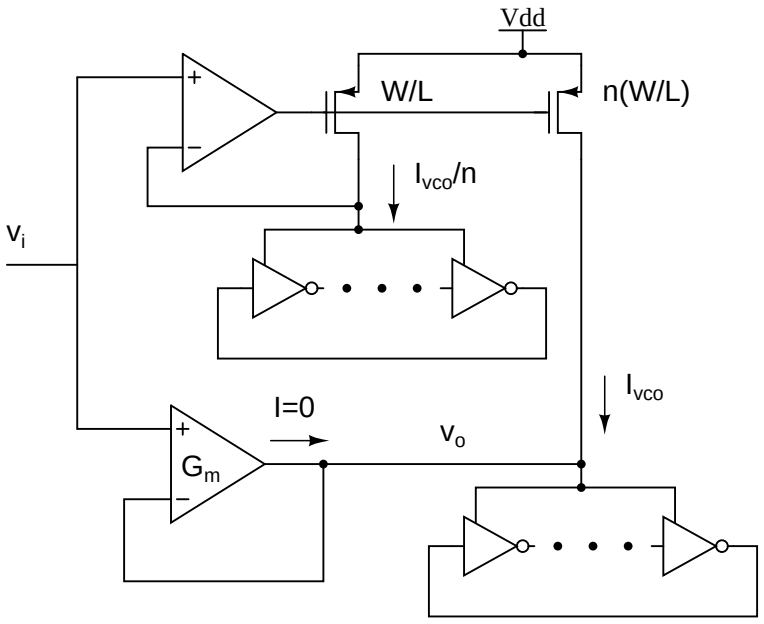

Figure 4.4: Feedforward replica current injection

current injection case is given by

$$v_i(t)[G_m + G_{ff}(t)] = v_o(t)[G_m + G_{vco}(t)] + C_{vco}\frac{dv_o}{dt} \tag{4.4}$$

when $G_{ff}(t) = G_{vco}(t)$

$$v_i(t) = v_o(t) + \frac{C_{vco}}{G_m + G_{vco}(t)}\frac{dv_o}{dt} \tag{4.5}$$

The VCO current can be seen as a dc current plus a zero average periodic current riding over it. As the number of stages increase the current drawn from the VCO

control voltage will tend to a DC current[1]. In the current design to meet the requirement of delaying narrow UP/DN pulses, the replica ring oscillator chain consists of a large number of high speed inverters. Thus the DC current is much larger than the transient variations in the current and its effect can be ignored. Hence the time varying load $G_{vco}(t)$ can be approximated to its average value G_{vco}. Applying the Laplace transform to Eq. 4.5, we get

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{1 + \frac{sC_{vco}}{G_m + G_{vco}}}$$

The above equation shows that the DC gain is 1 (independent of G_m) and the pole is located at $(G_m + G_{vco})/C_{vco}$.

It can be inferred from the preceding analysis that the two techniques ensure a unity DC gain and are identical complexity wise. Even the supply noise rejection[2] of the PLL remains same for both the techniques as shown in Fig. 4.5.

However the positive feedback method has a drawback when there is a mismatch between the actual VCO load and the replica load. If

$$G_{fb} > G_{vco}$$

then at the DC we have

$$\frac{v_o}{v_i} = \frac{1}{1 - \frac{\Delta G}{G_m}} \tag{4.6}$$

[1]As the number of stages increase for a given frequency of oscillation, the rise and fall times of the oscillator output will reduce and the output will tend to be nearly rectangular in shape. The high frequency current drawn from the supply will have frequency of nf_{vco}, where n is the number of stages. This is because the n-stages in a VCO draw current from the supply when they are undergoing transitions in a single VCO period offset in phase by π/n. As n increases the phase difference between the successive outputs of the inverters in the oscillator chain will become smaller and the current drawn from the supply will appear like a DC when n tends to ∞.

[2]The supply noise rejection of the PLL is measured by injecting noise at the supply voltage of the buffer driving the VCO and computing the phase noise at the VCO output. In the current analysis the PLL was replaced with its linear model with the buffer driving the VCO alone at schematic level. The noise was injected at the supply of the buffers and the phase noise was computed at the linear VCO phase-domain model.

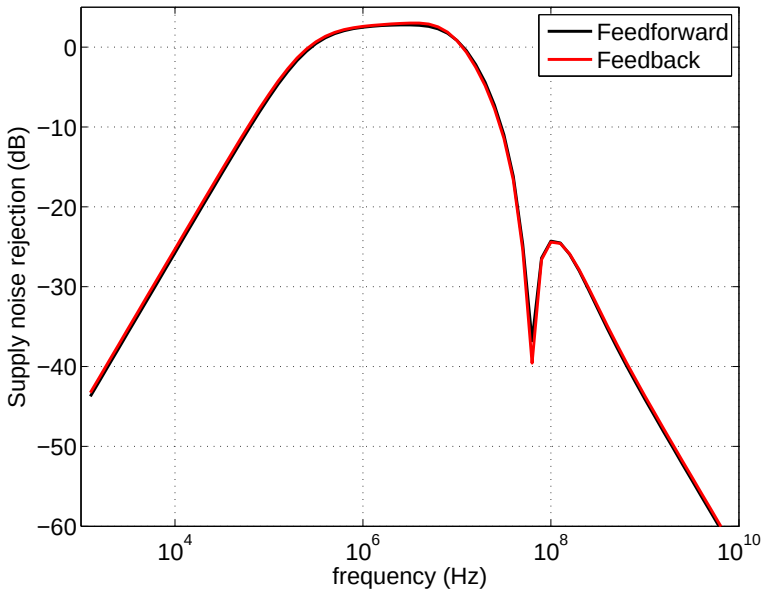

Figure 4.5: Supply noise rejection of the two techniques when applied to the PLL.

where $\Delta G = G_{fb} - G_{vco}$ Here we can see that when $\Delta G > G_m$ the gain is negative and the loop becomes unstable. This might be true in cases where $G_{vco} \gg G_m$.

In the feedforward method of providing the load current, the gain at dc is given by

$$\frac{v_o}{v_i} = 1 + \frac{\Delta G}{G_m + G_{vco}} \tag{4.7}$$

And it is less sensitive to variations in G_{ff}. So the feedforward method is chosen for implementation. The loop gain $LG(s)$ of the PLL after applying the technique is given by

$$LG(s) = \frac{I_{cp1} K_{vco} (1 + \frac{s}{\omega_z})}{s^2 C_1 (1 + \frac{s}{\omega_p})} \tag{4.8}$$

where

$$\begin{aligned} \omega_z &= \frac{G_m + G_{vco}}{(a_1 + (G_m + G_{vco})R)C_1} \\ \omega_p &= \frac{G_m + G_{vco}}{C_{vco}} \end{aligned}$$

The VCO load is modeled as a linear load $R_{vco} = 1/G_{vco}$ for loop dynamics simulations. Fig. 4.6 shows the step response of the PLL for a control voltage step

of 0.1 V. Also shown in the figure is the step response of the PLL when the VCO load is time varying. The linear resistive model of the VCO is replaced by the VCO running at the desired frequency of oscillation. The close match between the two step response validates the assumption made in modeling the load of the VCO as a resistor R_{vco}. The parameters of the delay tuning PLL are listed in 4.1.

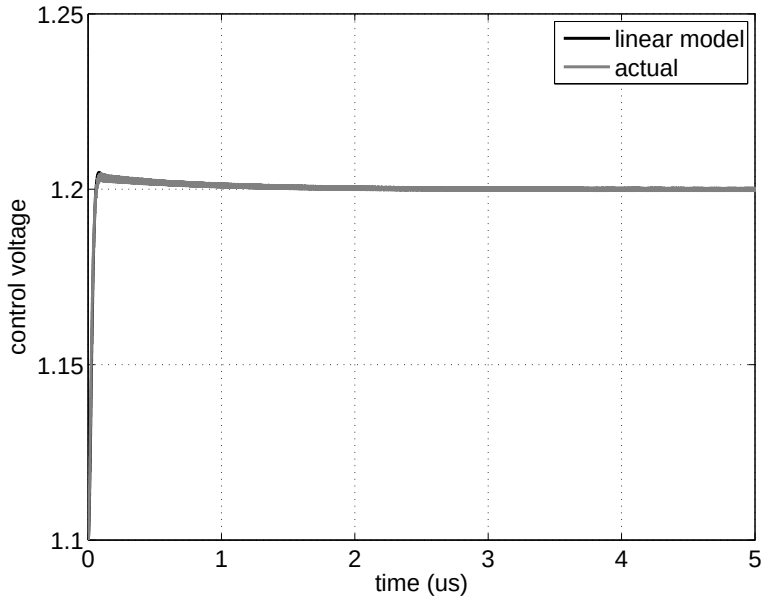

Figure 4.6: Step response of the PLL with the VCO impedance modeled as resistor overlaid with the actual VCO timevarying load.

Table 4.1: Delay tuning PLL parameters

	Parameters
Input frequency	160 MHz
PFD	Tri-state PFD
charge pump currents	$I_{cp1} = 5\,\mu$A, $I_{cp2} = 50\,\mu$A
Resistor and capacitors	$\mathrm{R} = 5.2\,\mathrm{K}\ \Omega, \mathrm{C}_1 = 41.4$ pF, $\mathrm{C}_{\mathrm{vco}} = 9.1$ pF
VCO	$f_{vco} = 160$ MHz, $K_{vco} = 344.25$ MHz/V
unity gain bandwidth	$f_u = 4$ MHz
closed-loop 3dB bandwidth	$f_{3dB} = 5.9$ MHz
Phase margin	PM$\approx$ 72 degree

4.1.3 Choice of input frequency

The inverter chain used in the VCO (in the steady state) provides a delay of $T_i/2$ and is used as delay cell in the randomization logic of the actual PLL. If the input frequency of the delay tuning PLL is 20 MHz, the control voltage of the PLL will have spurs at 20 MHz and when it is used to drive the replicated delay cell in the actual PLL with randomization it introduces noise at f_r degrading the spur performance. To overcome this problem we use an input frequency of Nf_r and thus the spurs introduced by the delay tuning PLL occur at Nf_r. Thus the input frequency of the DPLL is chosen to be $8f_r = 160$ MHz.

4.1.4 Inverter chain based VCO

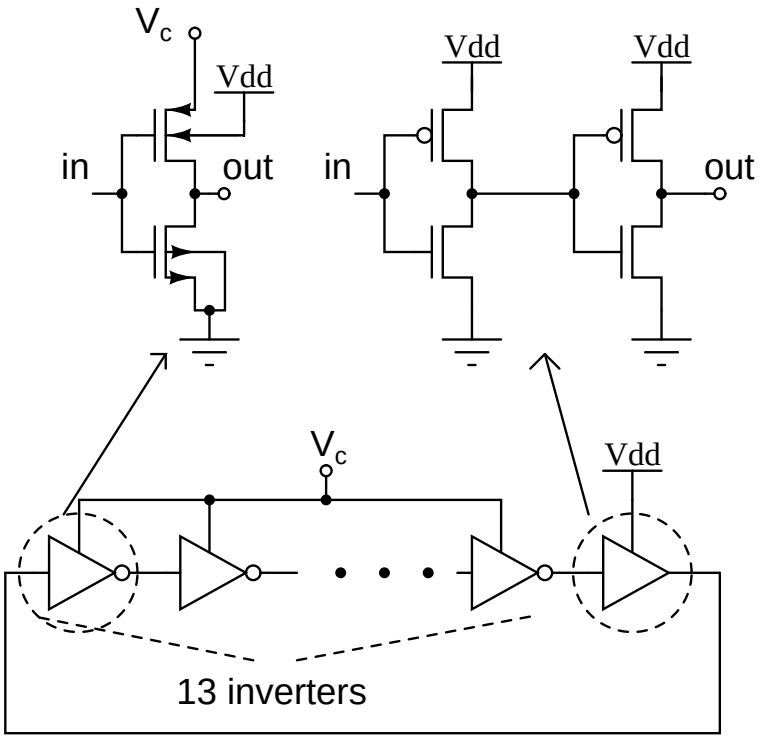

Figure 4.7: VCO schematic.

The VCO of the delay tuning PLL is a chain of inverters with a slicer buffer as shown in the Fig. 4.7. The slicer buffer is added keeping in mind the fact that the chain of inverters would be replicated in the delay cell of the actual PLL

and a long chain would narrow the UP/DN pulses as they propagate through the chain. Thus repeater buffers should be added in between the inverter chains to restore the rise and fall times of the propagating pulse. The added repeater buffers will introduce additional delay in the delay line which leads to degradation in the spur performance (due to the increase in the delay of the individual cell). So the repeater buffer is included in the VCO itself and the delay of the chain with the buffer is tuned to $T/2$ in the steady state. The tuning characteristics of the inverter chain VCO is shown in Fig. 4.8. The inverter chain of the VCO provides

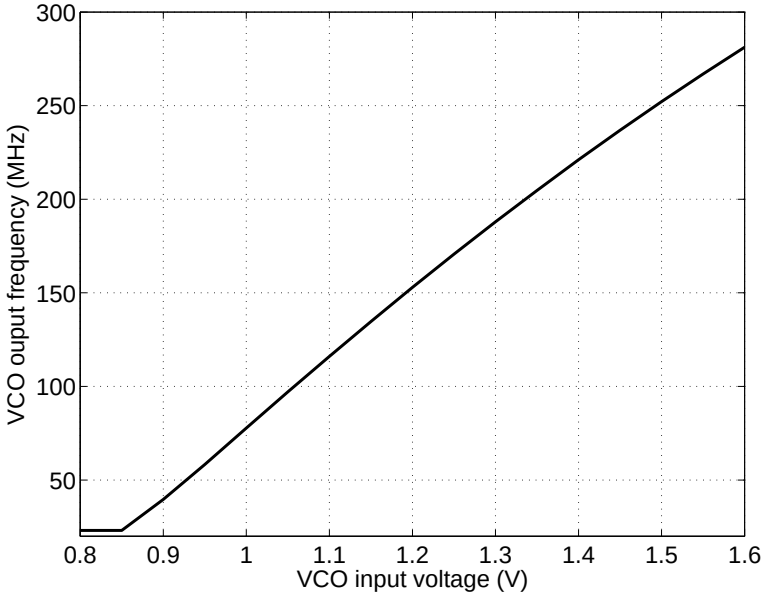

Figure 4.8: VCO tuning characteristics.

a delay of $T/2N$ and a cascade of two such invert chains provides a delay of T/N. Thus a cascade of two such VCO inverter chains is used a single unit delay cell of delay T/N in the randomization logic of the PLL. The schematic of the unit delay cell is shown in Fig. 4.9.

4.1.5 Schematic of the PFD and charge pump

The schematics of the PFD and two charge pumps are similar to the ones used in the actual PLL explained in chapter 3.

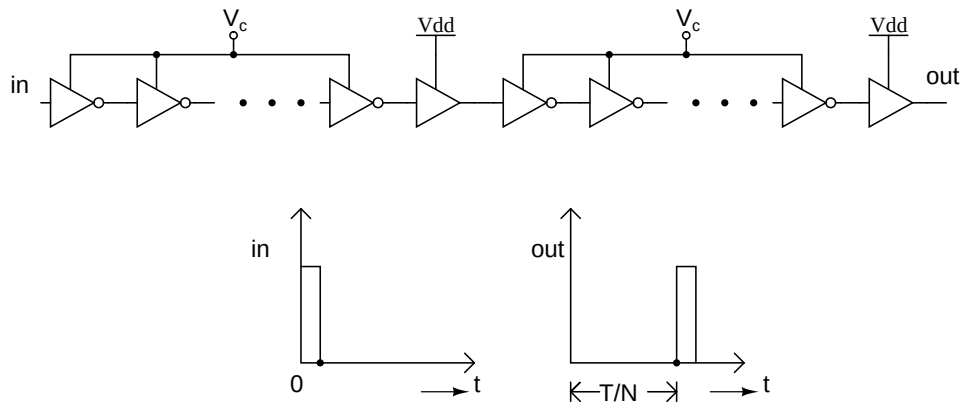

Figure 4.9: Delay cell schematic showing the cascade of inverter chains used in the VCO.

4.1.6 DLL buffer

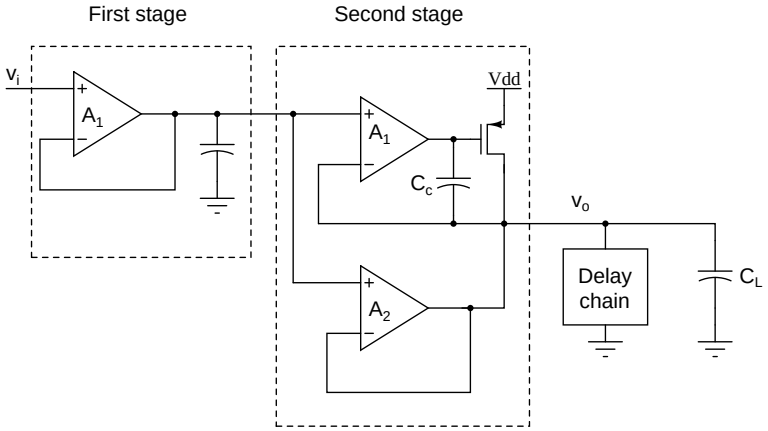

Figure 4.10: Delay cell buffer.

The control voltage of the delay tuning PLL has to drive a low impedance load (the replicated delay cells with supply voltage control) which draws switching current. The VCO control node cannot be directly used to drive the delay chain as the load will affect the stability of the delay tuning PLL. Hence a buffer is necessary to isolate the load from the control voltage node. The buffer is divided into two stages, the first stage is a low capacitance input stage with a very low bandwidth to filter out all the high frequency noise on the control voltage. The second stage is the driver stage which drives the load of the delay cell. The delay cell offers a low resistive impedance[3] $\approx R_{vco}/14$ and a large load capacitor C_L is connected

[3]A cascade of two identical VCO chains form a single delay cell and hence if R_{vco} is the

at the output node for better supply noise rejection and to minimize the voltage fluctuations at that node due to switching currents drawn by the inverters. The low impedance output node demands a two stage amplifier for the second stage buffer to meet the gain requirements. But it leads to two closely spaced poles for a two stage amplifier (due a large resistance and small capacitance at the high gain first stage). To compensate this a large compensating capacitor is needed, which results in a low bandwidth for the buffer. So a feedforward compensation path is used from the input to the output that bypasses the two stage amplifier at high frequencies as shown in Fig. 4.10. This simultaneously provides the high gain (gain of a two stage amplifier) at DC and a large bandwidth (equivalent to an uncompensated single stage amplifier).

The amplifiers A_1 and A_2 are single stage differential to single ended amplifiers

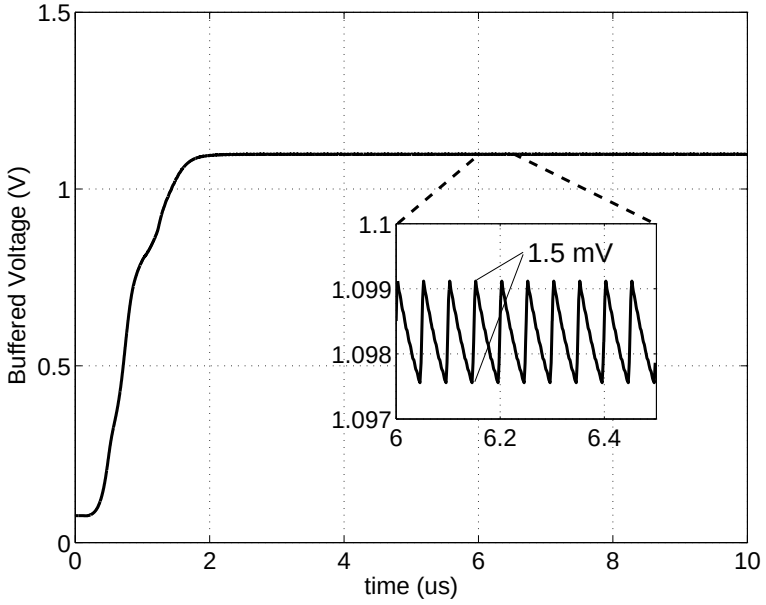

Figure 4.11: Buffer step response.

with NMOS inputs and PMOS current mirror load. A_1 is a low bandwidth amplifier with a current consumption of $10\,\mu$A and A_2 is the high bandwidth amplifier with a current consumption of $400\,\mu$A. The amplifiers are chosen with NMOS

impedance looking into the supply voltage of the VCO chain, then $R_{vco}/2$ is the impedance of a single delay cell. Since 7 such delay cells are needed for the entire delay generating block, the impedance looking into the supply of the entire delay chain is $R_{vco}/14$.

input pairs since the variation of the control voltage is always above 0.9 V across process and temperature variations.

A transient simulation is performed to test the performance of the buffer feeding the bias to the delay line. The buffer is made to drive a time varying load which is simulated by exciting the delay cell with a periodic signal of time period $T = 50\,ns$ and a pulse width of 1 ns[4]. The buffer delivers a voltage of 1.1 V to the simulated time varying load. The step response of the buffer simulated at a schematic level is shown in Fig. 4.11.

[4]This is done to emulate the actual load in the lock condition where the pulse widths of the UP/DN signals is of the order of 1 ns.

CHAPTER 5

Simulation Results

5.1 Block level simulations

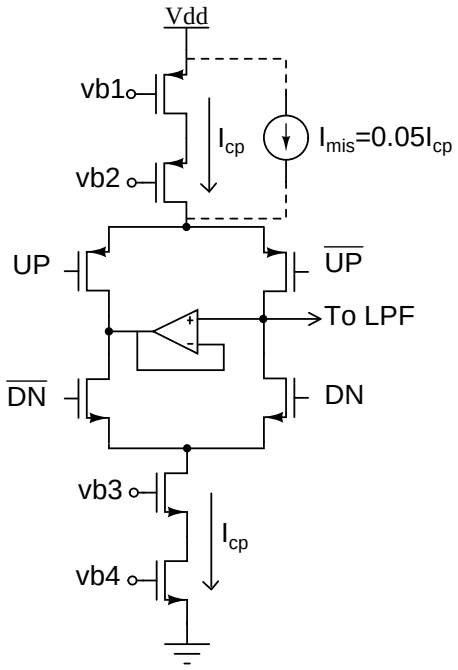

Figure 5.1: Transistor level charge pump schematic showing the source of mismatch added for simulations.

Reference spurs arise due to nonidealities in the PFD, charge pump and loop-filter. To reduce the simulation time, the VCO, divider and the digital logic for randomization are modeled behaviorally as they have no effect on the generation of reference spur. The PFD, charge pump and loop filter are simulated at transistor level. The VCO, divider and the randomization logic are noiseless and the source of noise is only deterministic, contributed by the charge pump and PFD. To model the effect of charge pump mismatch, a constant current source of value $0.05I_{cp}$ (5 % mismatch) is connected in parallel with the upper current source as shown in

Fig. 5.1. The feed through is inherent with the circuit of the implemented charge pump.

The simulated[1] phase noise of the 8-PPM and 8-PR techniques overlaid with the

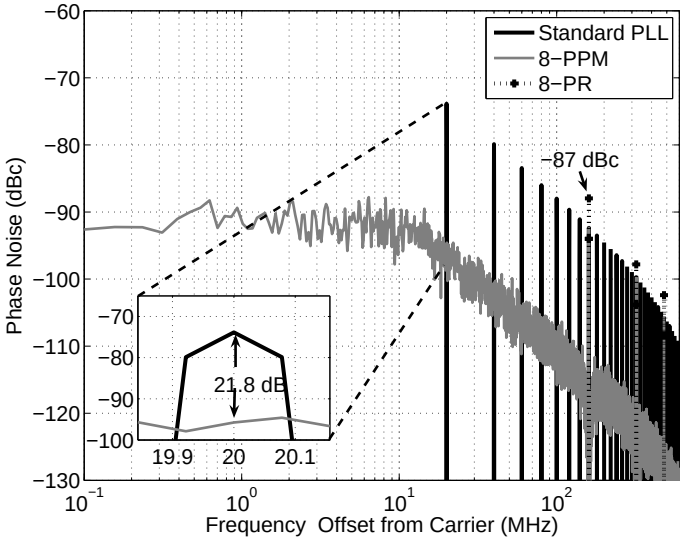

Figure 5.2: Phase noise of the PLL output comparing the the performance of the 8-PPM and 8-PR techniques with the standard PLL (The resolution bandwidth used for PSD computation is 78.125 kHz).

standard PLL is shown in Fig. 5.2. The figure shows the absence of reference spur in both the 8-PPM and 8-PR techniques. The spur is converted to noise in 8-PPM technique and the noise level is 21.8 dB below the reference spur (measured at a resolution bin-width of 78.125 kHz). The 8-PR technique has only spurs at $8f_r$ without adding any redistributed noise as expected. Additionally it can be observed that the spur at $8f_r$ in case of 8-PR is higher than the PPM. This is attributed to the net increase in the injected spur current into the loop filter as the feed through current does not exactly scale with the scaled switch sizes.

The randomization techniques (8-PPM and 4-PPM+2-PR) spread the energy in the harmonics to all the frequencies and hence raise the noise floor at the PLL output. To study the effect of the techniques on the output phase noise we compare the phase noise contribution of the VCO, loop filter resistor and charge pump to

[1]The phase noise of the PLL is obtained by computing the PSD of the output VCO phase, which is obtained by running a transient simulation of the PLL and integrating the zero mean control voltage ($v_c(t)$) after settling, $\phi_{out} = 2\pi K_{vco} \int v_c(t)dt$.

the noise introduced by 8-PPM and 4-PPM+2-PR techniques. Fig. 5.3 shows the phase noise due to the randomization overlaid with the PLL noise at the output. (The phase noise model of the open loop VCO assumes a phase noise specification of -120 dBc/Hz at 1 MHz offset and a $1/f^3$ corner of 200 kHz as shown in Fig. 5.3[2]). The phase noise contributed to the PLL output by the VCO

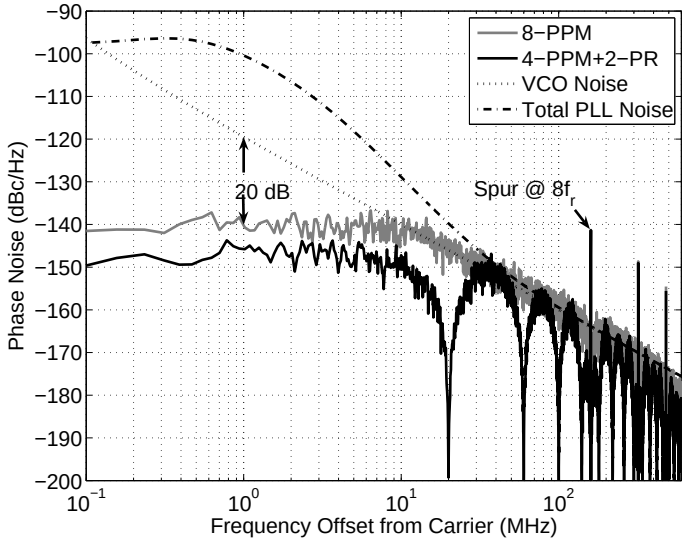

Figure 5.3: Phase noise at the PLL output due to the resistor, VCO and charge pump compared with the redistributed noise added by 8-PPM and 4-PPM+2-PR techniques.

and resistor is dominant near the bandwidth of the PLL and at high frequencies. The plot shows that the noise added by the randomization techniques is 40 dB lower than these two contributions at frequencies close to the bandwidth of the PLL and it becomes dominant only at frequencies greater than f_r (20 MHz in the simulated PLL). We can also see from Fig. 5.3 that the combined 4-PPM+2-PR technique has lower redistributed noise due to the additional filtering offered by 2-PR as explained before.

Fig. 5.4 shows the spectrum of the 4-SPPM+2-PR technique when applied to the implemented PLL and compared with the 8-PPM technique. We can clearly see the shaping of the noise for low frequencies, leading to orders of magnitude

[2]A point to note is that the actual VCO implemented in the PLL is not as stringent. The purpose here is to emphasize that the noise introduced by these techniques are smaller compared to such a stringent VCO specification.

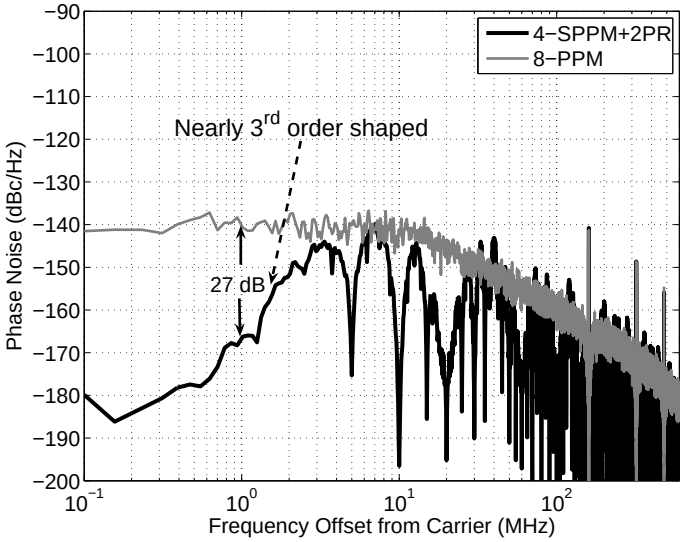

Figure 5.4: The phase noise contribution of the 8-PPM overlaid with the phase noise due to 4-SPPM+2-PR technique.

reduction in the 'midband' region. The simulated PLL shows a reduction in the noise level by 27 dB near the PLL bandwidth ($f_r/20$) compared to the 8-PPM technique.

5.1.1 Transient simulation

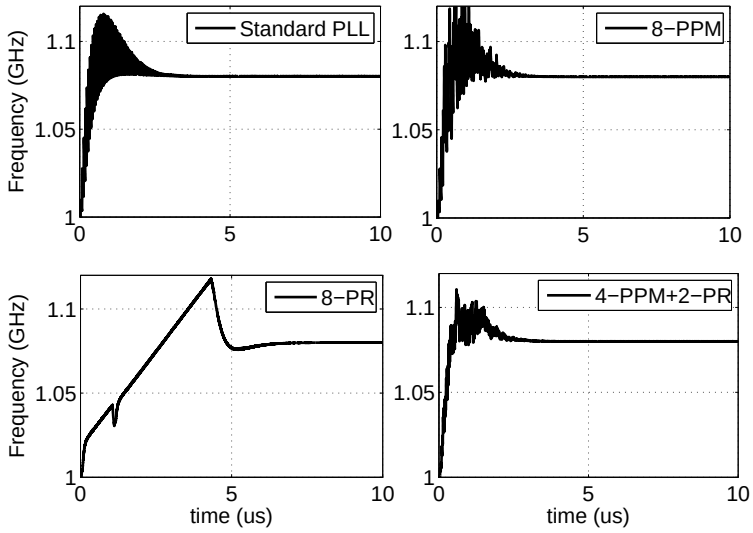

Figure 5.5: Settling behavior of the PLL for different techniques for a frequency step of 80 MHz (from 1 GHz to 1.08 GHz).

As mentioned earlier in Section 2.4.2, the 8-PR technique has the problem of

gain saturation for large phase/frequency errors which leads to an increased settling time. So to compare the large-signal settling of the PLL when the different techniques are applied, we give a step of 4 in the divide value (50 to 54) which corresponds to an output frequency step of $4f_r = 80$ MHz from 1 GHz to 1.08 GHz. Fig. 5.5 shows the simulated response of the PLL to a frequency step when different techniques were applied. The figure shows that the settling behavior of 8-PPM and 4-PPM+2-PR techniques is similar to the standard PLL. The PR technique shows a slewing behavior due to the gain saturation for nearly 4.5 μs and then settles to the desired value after 8 μs (approximately twice as much as in the other techniques).

5.2 Noise computations

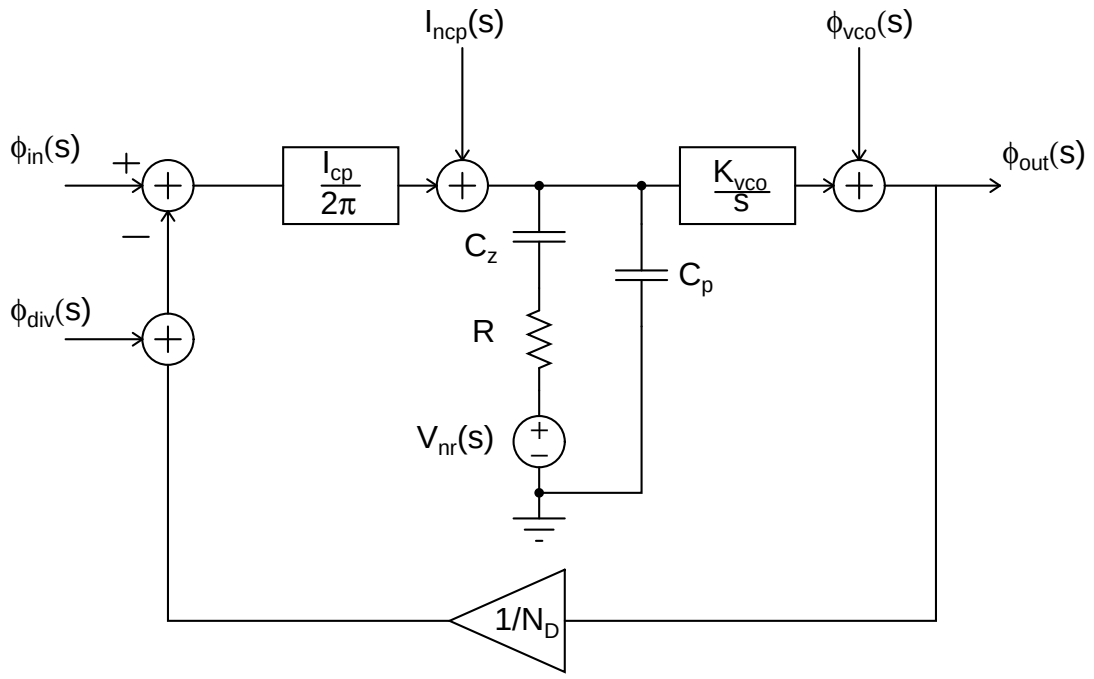

Figure 5.6: Linear PLL model showing the various noise sources contributing to the output phase noise.

The phase noise of the VCO simulated at 1.18 GHz is shown in Fig. 5.7. The phase noise is close to -98.5 dBc/Hz @ 1 MHz offset from the carrier. The simulated noise current density of the charge pump output current is shown in Fig. 5.8. To

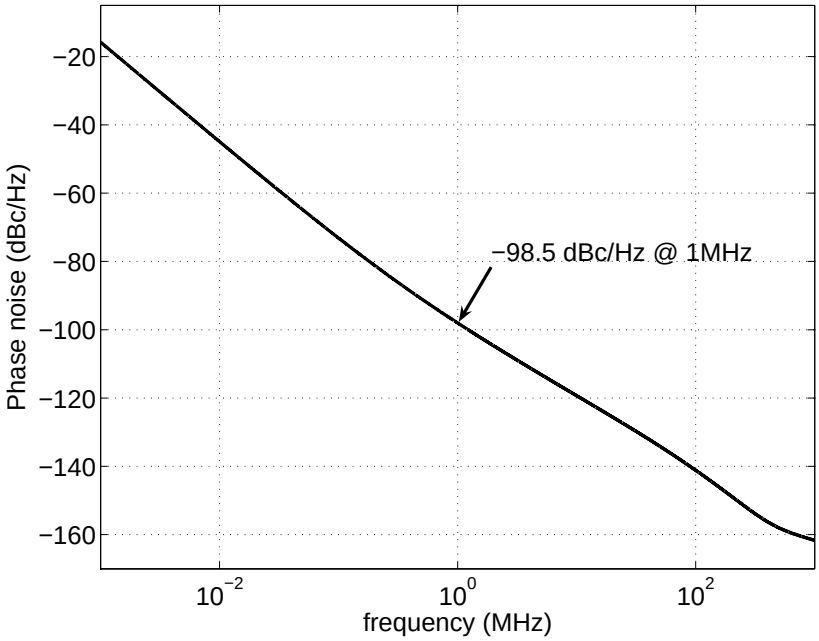

Figure 5.7: VCO phase noise measured at 1.18 GHz.

obtain the current noise spectral density, the output node of the charge pump is connected to a constant DC voltage source (0.9 V in the nominal case) and the noise current is measured through the voltage source after performing an AC noise analysis. In the steady state, the UP/DN pulses are on for at least T_{rst} seconds. Assuming a white current noise spectral density, the total noise current power injected into the loop filter reduces by a factor of T_{rst}/T. Hence we scale the noise current density obtained from the noise analysis by a factor T_{rst}/T to obtain the actual noise current density injected into the loop filter [18]. For a worst case noise analysis T_{rst} is chosen to be 2 ns[3]. The total PLL output noise overlaid with the individual contributions is shown in Fig. 5.9. The total PLL noise is overlaid with the noise added by the randomization techniques to compare their performance. The randomization noise is significantly lower than the noise contribution of the PLL. The VCO noise used for noise computations is the noise of the implemented VCO and not the ideal VCO noise profile assumed previously in Fig. 5.3.

[3]The nominal value is 1.2 ns.

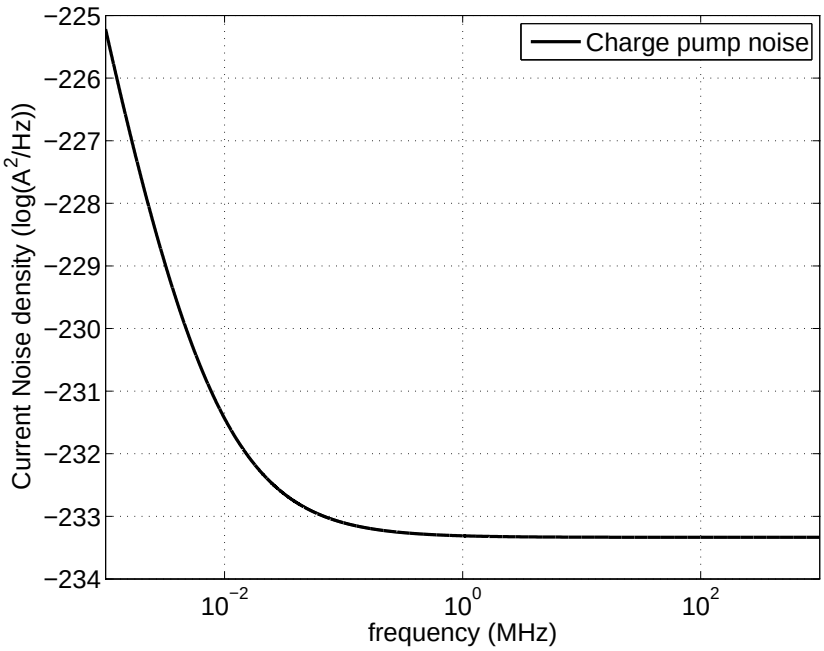

Figure 5.8: Charge pump noise current density.

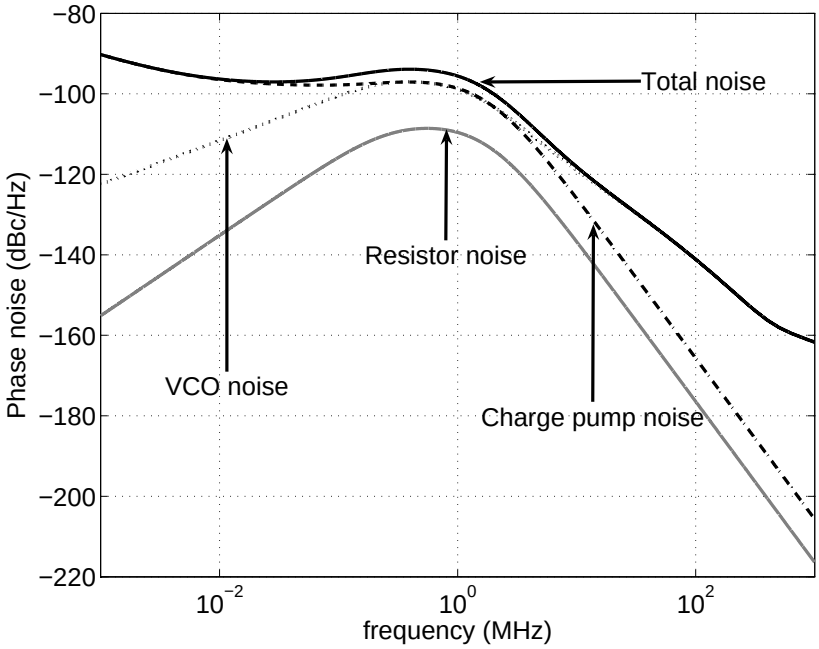

Figure 5.9: Total PLL output noise.

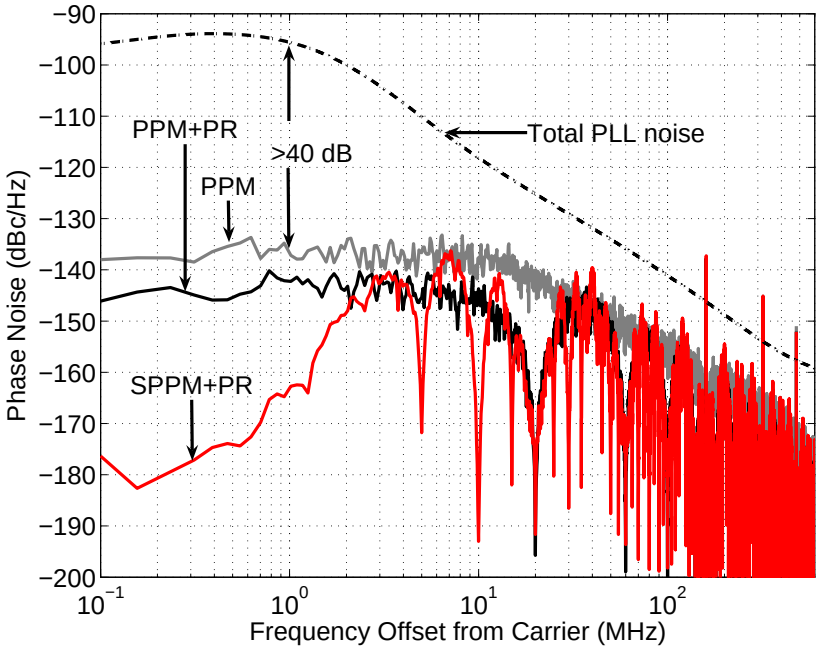

Figure 5.10: Total PLL output noise overlaid with the noise added by the randomization techniques.

5.2.1 Power consumption

The total current consumption of the PLL is listed in Table. 5.1.

Table 5.1: PLL power consumption

Block	**Current consumption**
PFD	0.462 mA
Charge pump	0.18 mA
Randomization Logic	0.5 mA
VCO (nominal setting)	6.7 mA
Divider	8.7 mA
Delay tuning PLL	1.32 mA
Total	16.54 mA (without Delay tuning PLL)
Total	17.86 mA (with Delay tuning PLL)

CHAPTER 6

Testing

6.1 Floor plan of test chip

The layout floor plan of the test chip fabricated to verify the ideas presented in the previous chapters is shown in Fig. 6.1. Empty area is filled up with supply bypass capacitors.

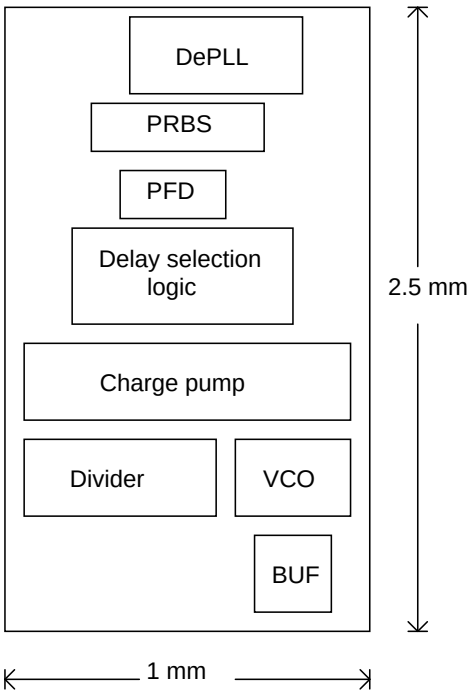

Figure 6.1: Floor plan of the designed PLL.

The snapshot of the layout of the chip is shown in Fig. 6.2. The area of the individual blocks are given in Table 6.1

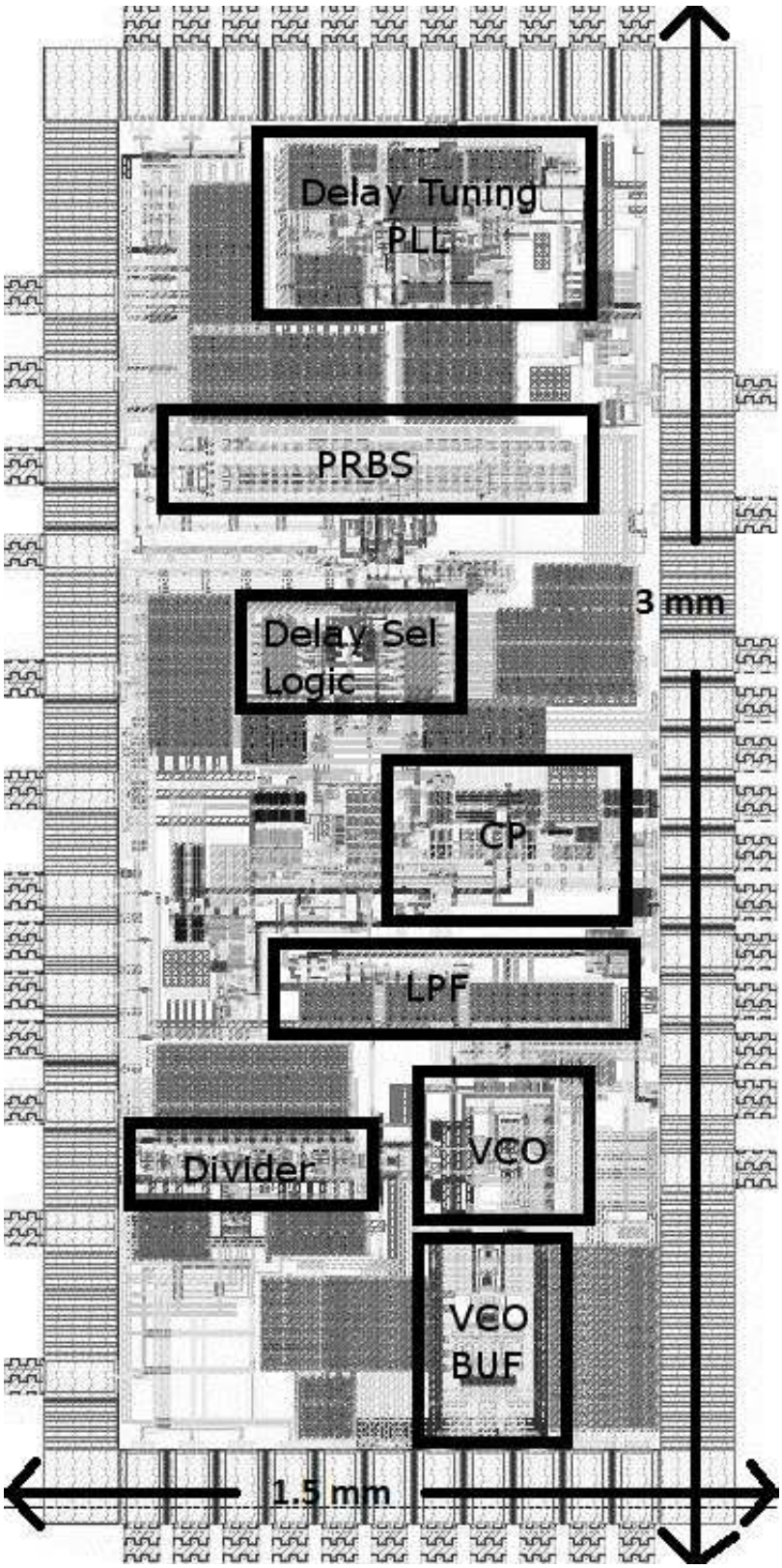

Figure 6.2: Snapshot of the layout of the designed PLL

Table 6.1: Areas of individual blocks.

Block	**Area** (mm^2)
PFD	0.00075
Charge pump (both PPM and PR, including by pass caps)	0.1524
LPF	0.084
VCO	0.055
Divider	0.03
Delay selection logic	0.048
PRBS	0.1125
Delay tuning PLL	0.245

6.2 Measurement setup

The test setup for measuring the phase noise of the PLL is shown in Fig. 6.3. A Rhode and Schwarz spectrum analyzer with a measurement frequency range of 200 kHz to 13 GHz was used for measuring the phase noise. The PLL output from the chip is differential and the spectrum analyzer is single ended. Hence a Balun was used to convert the differential signal to a single ended output before feeding it to the spectrum analyzer as shown in Fig. 6.3.

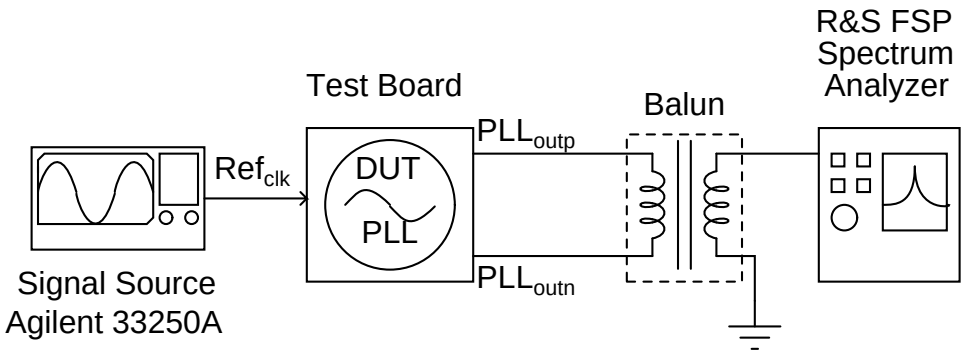

Figure 6.3: Test setup for measuring the phase noise of the PLL chip.

6.3 Measured results

The phase noise of the measured PLL is shown in Fig. 6.4. The measured spur at $f_{vco} + f_r$ is -65 dBc and $f_{vco} - f_r$ is -64 dBc below the carrier power. Fig. 6.5

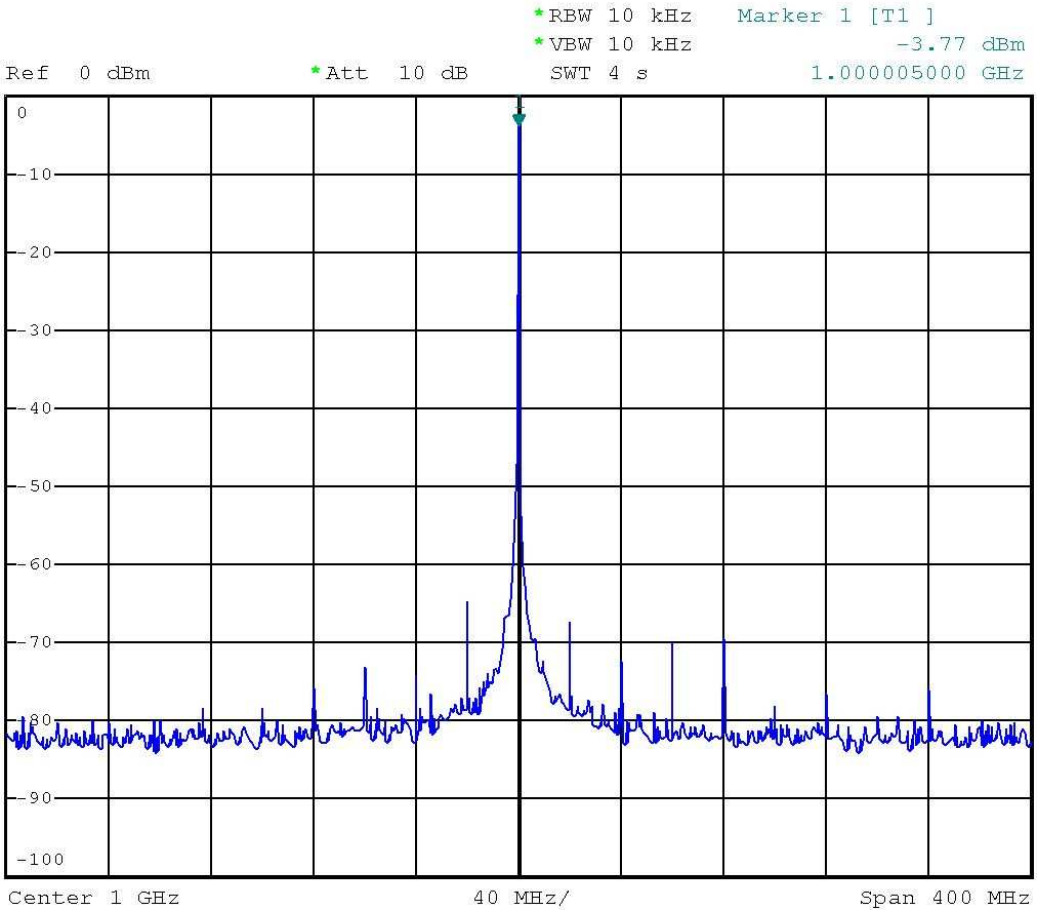

Figure 6.4: Measured results showing the PLL output spectrum.

shows the measured phase noise of the PLL when PR is enabled. The reduction in the spur level at $f_{vco} \pm f_r$ can be clearly seen. The spur level at $f_{vco} - f_r$ is -73 dBc (9 dB reduction in spur). Fig. 6.6 shows the phase noise of the PLL when PPM is enabled. Even in this case the reduction in the spurs can be clearly seen. The spur level at $f_{vco} - f_r$ is -72 dBc (8 dB reduction in spur). Fig. 6.7 shows the phase noise of the PLL when different techniques are applied. It can be seen that the in band noise of the PLL remains unaffected when PR is tuned on. This is due the fact that the in band delay line noise which is dominated by the flicker noise of the delay line, gets first order shaped as discussed in Chapter 2. Hence the in

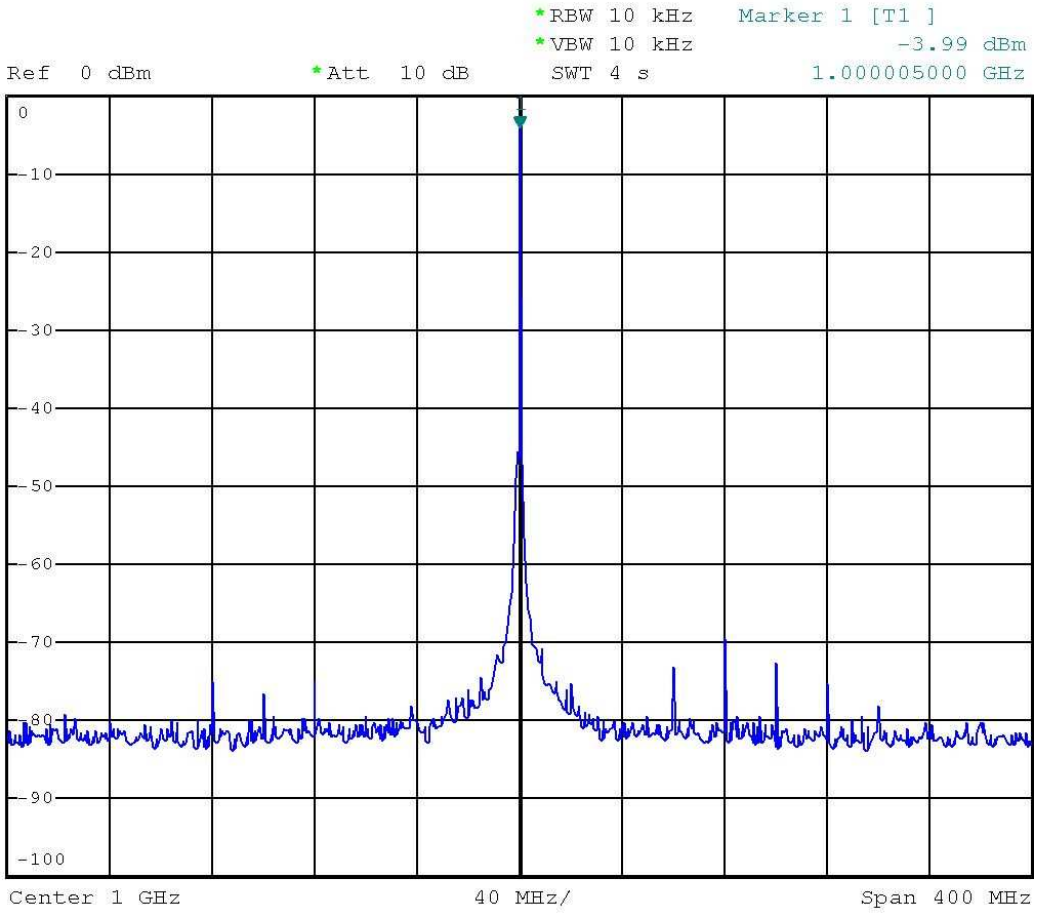

Figure 6.5: Measured results showing the PLL output spectrum when PR is turned on.

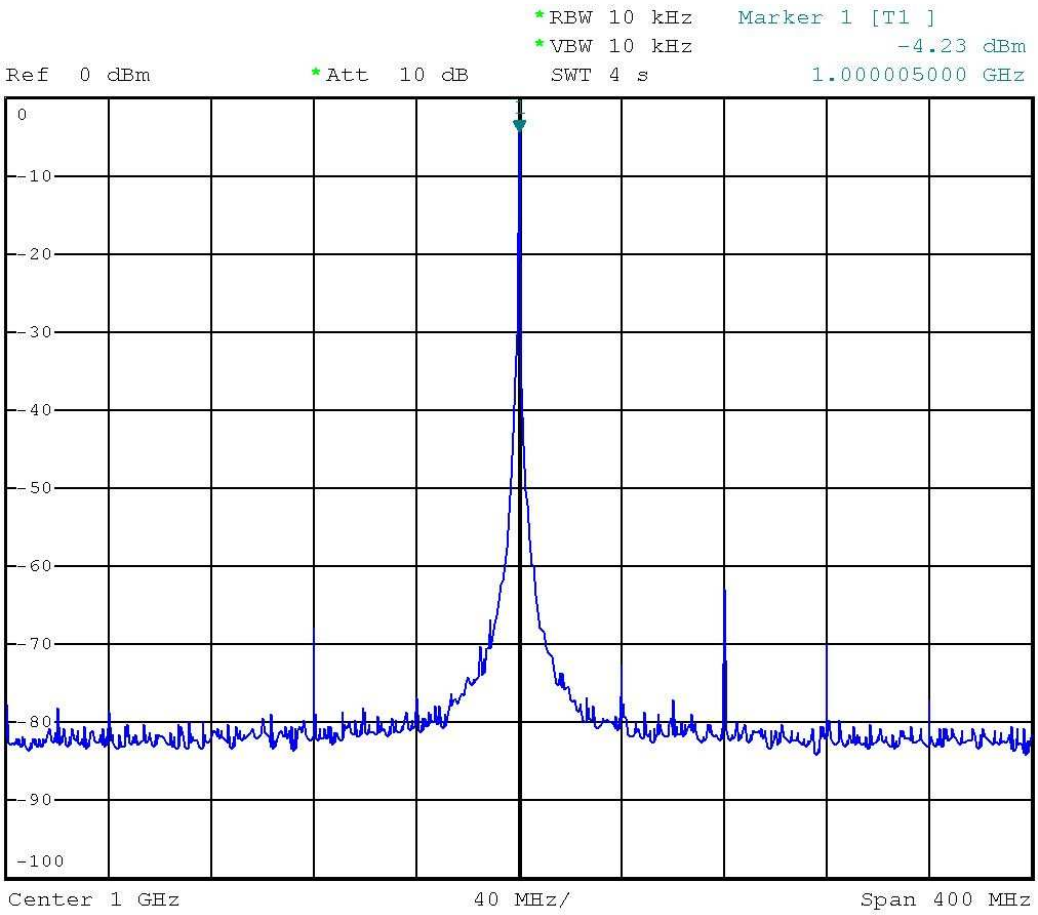

Figure 6.6: Measured results showing the PLL output spectrum when PPM is turned on.

band noise addition due to PR is insignificant. The noise of the PLL when PPM is enabled increases significantly due to the high gain provided by the PLL loop filter at low frequencies for the redistributed noise. The result is a clear indication that PPM with a iid sequence is not an attractive solution from a noise perspective. Though not implemented in the current work, one can use a noise shaped PPM and apply PR (SPPM+PR) in conjunction with it to reduce the in band noise contribution as suggested in Chapter 2.

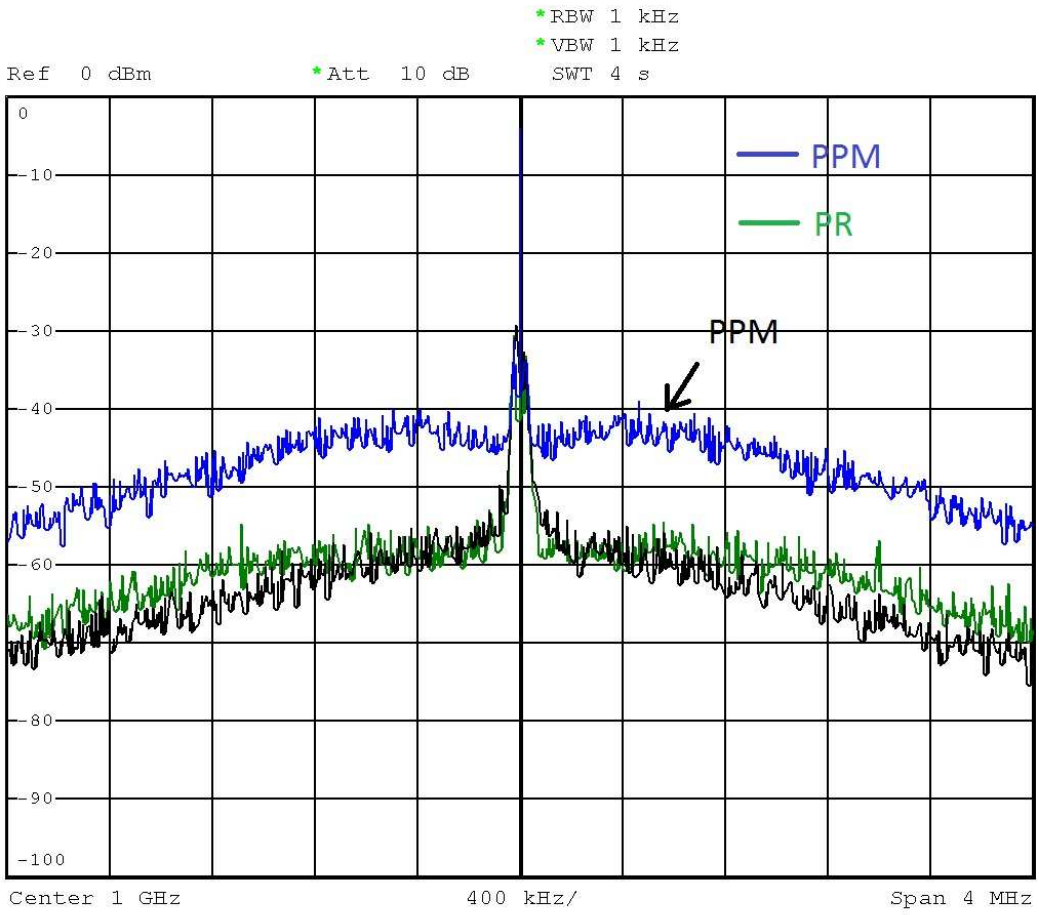

Figure 6.7: Measured results showing the PLL output noise. The measured in band noise spectrum of the PPM, PR and normal PLL are shown in blue, green and black colors.

The spur levels in the output spectrum of the measured PLL are listed in Table. 6.2.

Table 6.2: Measured spur levels for different techniques

Spur (offset from carrier)	**Spur level in dBc (Normal)**	**Spur level in dBc (PR)**	**Spur level in dBc (PPM)**
$+f_r$	-65	-69	-79
$+2f_r$	-68	-81	-69
$+3f_r$	-66	-69	-73
$+4f_r$	-64.6	-65.15	-59.6
$+5f_r$	-85	-76	-84.4
$+6f_r$	-75	-75	-65
$+7f_r$	-74.6	-77.5	-81.5
$+8f_r$	-75	-76	-76
$-f_r$	-64	-73	-72
$-2f_r$	-70	-81	-69
$-3f_r$	-71	-76.5	-83
$-4f_r$	-70.6	-72	-64.5
$-5f_r$	-81	-82.5	-89
$-6f_r$	-78	-70.2	-81
$-7f_r$	-78	-86	-83
$-8f_r$	-77	-78	-76

6.4 Discussions on measured results

6.4.1 Spurs at $\pm 4f_r$

Large spurs at $f_{vco} \pm 4f_r$ were observed in the measured results in all the cases. The magnitude of these spurs did not change with the changes in the delay values or by changing the switch voltage levels of the charge pump. This is an indication that the source of the these spurs are not due to nonidealities in delay cells, PFD and charge pump. Though the exact source of these spurs could not be traced due to time constraints of the work, it is clear that it is due to external sources like coupling from the switching currents in the divider and on board coupling.

6.4.2 Higher even order harmonics in PPM

When the PPM is enabled higher even order harmonics were observed (harmonics at $2f_r$ and $4f_r$ were larger in magnitude compared to PR). This is attributed to

the switching noise induced by the PRBS operation. This hypothesis was verified by turning on the PRBS alone and enabling the PR technique. Ideally this should have no effect on the PR technique as the multiplexer in the PPM is bypassed in this mode. When the PR technique was enabled without enabling the PRBS, the second harmonic spurs were lower in magnitude and when the PRBS was turned ON the second harmonic terms increased to the levels as seen in PPM.

6.4.3 Asymmetric spurs at $f_{vco} \pm k f_r$

The spurs measured at the PLL output exhibit asymmetry about the center frequency. That is the spurs at $f_{vco} + k f_r$ and $f_{vco} - k f_r$ are unequal in magnitude. The spurs are an effect of frequency modulation of the VCO output due to a periodic charge injection at the control voltage every reference cycle. If it was purely frequency modulation then the spurs about the VCO frequency should be identical in magnitude (explained in Appendix C). Similarly in case of a sinusoidal amplitude modulation, the spectrum of the amplitude modulated signal contains equal magnitude spurs at $\pm f_r$ offset from the carrier. The only difference between an AM signal and narrow band FM signal is that the phase of the sidebands are of opposite polarity in case of narrow band FM and same polarity in case of AM. Thus when an AM signal is added to an FM signal (both modulated with the same base band signal with different amplitudes), the resulting signal will have asymmetric tones at the modulating frequency (shown in Appendix C). Thus in the author's opinion the possible source of the asymmetric spurs is due to the amplitude modulation of the VCO output (which is already frequency modulated at f_r) at f_r.

The VCO output is taken to the pads through a CML buffer and then passed through a Balun on board before being fed to the spectrum analyzer. The bias current of the CML buffer is externally supplied through a pin. The source of amplitude modulation is the modulation of the bias current (at the reference fre-

quency) due to stray coupling on board. It is well known [19] that modulating the bias current of a CML buffer is nothing but mixing (multiplying) the input signal with the bias current modulating signal. This is nothing but an amplitude modulation of the input fed to the buffer. Fig. 6.8 illustrates the source of the amplitude modulating noise in the CML buffer. Thus the output of the buffer is a combination of AM and FM and hence the output sidebands are asymmetric. The signal at the output of the buffer can be modeled as

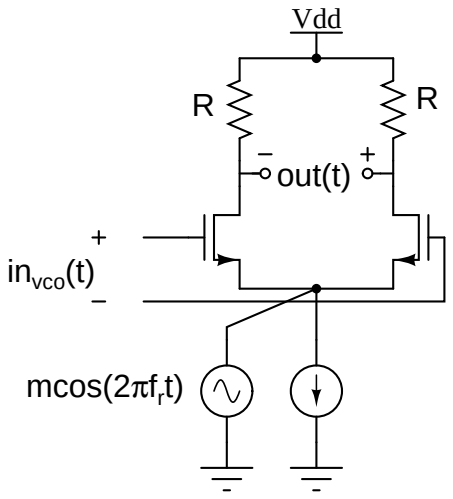

Figure 6.8: AM due to the modulation on the bias current.

$$x_{out}(t) = A\cos(2\pi f_{vco}t + m_2\sin(2\pi f_r t))(1 + m_1\cos(2\pi f_r t))$$

Using the results in Appendix C, it can be readily shown that the above signal will indeed have asymmetric spurs at $f_{vco} \pm f_r$.

CHAPTER 7

Conclusion and Future Work

A major contribution of this thesis is the spectral analysis and interpretation of PPM signals. A detailed analytical study of PPM was presented and noise shaping characteristics of several PPM based techniques were analyzed and discussed. PPM of charge pump current pulses by a uniformly distributed sequence behaves as a moving average filter and converts the filtered out harmonics to first order shaped wideband noise. The noise added is insignificant at frequencies close to dc. Therefore it does not affect the long term jitter of the PLL. Another spur reduction technique called pulse repetition (PR) (proposed in [7]) eliminates the spurs completely without redistributing it as noise. This technique is analysed and compared to PPM.

Different spur reduction techniques based on PPM and PR are discussed. Simpler implementation ideas are proposed to implement the techniques. Methods of increasing the order of noise shaping in PPM to further reduce the midband noise contributed by random PPM are discussed. The performance degradation of the techniques in the presence of delay variations, random mismatch in the delays and modulating sequence periodicity are discussed in detail. Simulation results confirm the correctness of the derived results, reduction in spur levels and low noise levels added by the PPM techniques.

The divider used in the design consumes high power due to the use of pseudo NMOS logic for the initial stages. Better power optimization techniques like using CML for the initial stages could be explored to reduce the power consumed by the divider.

Since the major focus of the work is on the analysis of PPM based techniques, the PLL was not optimized for random noise. The noise specification for which the

PLL was designed can be further tightened. For a given bandwidth, the charge pump current can be increased and the loop filter resistor can be reduced to improve the inband noise performance. The choice of ring oscillator for the VCO was made due to the lack of better models of the inductors in the current technology and time constraint to complete the work. However with an accurate inductor model the VCO noise can be further reduced employing LC oscillators.

A replica delay tuning PLL was used to tune the delay across process and temperature corners. This method however leads to an increased implementation complexity. Better circuit design techniques can be explored to reduce the delay variations in the delay line without increasing the implementation complexity.

APPENDIX A

Spectral Analysis of PPM signals

A.1 Autocorrelation function of the PPM signals

The pulse position and amplitude modulated signal $r_p(t)$ is given by

$$r_p(t) = \sum_k x_k p(t - kT - a_k T_d)$$

It can be expressed as $r_p(t) = r(t) * p(t)$ where

$$r(t) = \sum_{k=-\infty}^{\infty} x_k \delta(t - kT - a_k T_d) \tag{A.1}$$

$r(t)$ is an impulse train whose amplitude is modulated by the sequence x_k, and the impulse positions are modulated by a_k. Let x_k and a_k be stationary random processes[1], such that a_k is a integer valued sequence $\in [0, N-1]$. Let $R_x(k)$ be the autocorrelation function of x_k and $S_x(f)$ its power spectral density given by $S_x(f) = \sum_k R_x(k) e^{-j2\pi fkT}$. For a cyclostationary random process [20] of period T, the autocorrelation can be computed as a time average of the ensemble autocorrelation function.

$$R_r(\tau) = \lim_{L\to\infty} \frac{1}{LT} \int_{-LT/2}^{LT/2} E[r(t)r(t-\tau)]\, dt \tag{A.2}$$

[1]Though we have assumed x_k and a_k to be stationary, wide sense stationarity [20] is sufficient for the derivations given in this work.

$E[r(t)r(t-\tau)] = R_r(t,\tau)$ is the ensemble autocorrelation function given by

$$R_r(t,\tau) = E\left[\sum_i \sum_j x_i x_j \delta(t - iT - a_i T_d)\delta(t - \tau - jT - a_j T_d)\right]$$

Since x_k and a_k are independent, and $f(t)\delta(t-t_0) = f(t_0)\delta(t-t_0)$, and $E[x_i x_j] = R_x(i-j)$, making the substitution $i - j = k$, we get

$$R_r(t,\tau) = \sum_k \sum_i R_x(k) E\left[\delta(t - iT - a_i T_d)\delta(\tau - kT - (a_i - a_{i-k})T_d)\right]$$

The above equation shows that the ensemble autocorrelation is a function of time. It can be easily verified that it is also periodic, with a period T. Thus $r(t)$ is a cyclostationary random process [10]. Using Eq. (A.2) we get

$$R_r(\tau) = \sum_k R_x(k) \lim_{L\to\infty} \frac{1}{LT} \sum_{i=-L/2}^{L/2}$$

$$\int_{iT}^{iT+T} E\left[\delta(t - iT - a_i T_d)\delta(\tau - kT - (a_i - a_{i-k})T_d)\right] dt \tag{A.3}$$

we define $b_k = a_i - a_{i-k}$, as a new sequence. since the sequence a_k is stationary, the statistics of b_k is independent of time origin i and depends only on time difference k. Taking the integration inside the expectation operator and after some manipulations we obtain

$$R_r(\tau) = \frac{1}{T} \sum_k R_x(k) E\left[\delta(\tau - kT - b_k T_d)\right] \tag{A.4}$$

Let $P_A(a)$ be the probability mass function of the random variable a, and $P_{Bk}(b)$ be the probability mass function of the random variable b_k. Then

$$E\left[\delta(\tau - kT - b_k T_d)\right] = \sum_{b\in B} P_{Bk}(b)\left[\delta(\tau - kT - bT_d)\right] = P_{Bk}\left(\frac{\tau - kT}{T_d}\right)$$

Using the above result in Eq. (A.4) we have

$$R_r(\tau) = \frac{1}{T}\sum_k R_x(k) P_{Bk}\left(\frac{\tau - kT}{T_d}\right) \tag{A.5}$$

$P_{Bk}\left(\frac{\tau - kT}{T_d}\right)$ is a set of impulses spaced T_d apart centered around kT. The amplitude of the impulses is the probability mass function[2] of b_k. Eq. (A.5) can be re-written as

$$R_r(\tau) = \frac{1}{T}\sum_k R_x(k)\delta(\tau - kT) * P_{Bk}(\frac{\tau}{T_d}) \tag{A.6}$$

Then the spectrum of the PPAM signal is obtained by taking the Fourier transform of Eq. (A.6). To compute the autocorrelation function we need to compute $P_{Bk}(b)$ for all k. The expressions of the spectrum is derived for different cases of the modulating sequence by computing $P_{Bk}(b)$ for all these cases, in the reminder of the section.

A.1.1 PPM by an iid sequence

If the sample values of the sequence a_k are iid, then a_i and a_{i-k} are independent. The probability mass function $P_{Bk}(b)$ of b_k is the same for all non-zero values of k and is given by the convolution of the $P_A(a)$ and $P_A(-a)$ [10].

$$P_{Bk}(b) = \begin{cases} P_A(a) * P_A(-a) = P_B(b) & \text{for } k \neq 0 \\ \delta(b) & \text{for } k = 0 \end{cases} \tag{A.7}$$

where $P_B(b)$ is the time independent probability distribution of the sequence b_k. Using the above conditions we obtain the expression for $R_r(\tau)$ from Eq. (A.6) to

[2]Though we have assumed a_k to have discrete probability distribution, the expressions are same even for continuous distributions. If b_k is a continuous random variable then $P_{Bk}\left(\frac{\tau - kT}{T_d}\right)$ is a continuous symmetric pulse centered at kT, whose area is 1 (since it is a pdf).

be

$$\left(\frac{1}{T}\sum_{k} R_x(k)\delta(\tau - kT)\right) * P_B(\frac{\tau}{T_d}) + \frac{R_x(0)}{T}[\delta(\tau) - P_B(\frac{\tau}{T_d})]$$

The PSD $S_r(f)$ of the signal $r(t)$ is obtained by taking the Fourier transform of the above result. Since $P_A(\tau/T_d)$ is real. If $C(f)$ is the Fourier transform of $P_A(\tau/T_d)$, then the Fourier transform of $P_A(-\tau/T_d)$ is $C^*(f)$. Using Eq. (A.7) the Fourier transform $C_b(f)$ of $P_B(\tau/T_d)$ is given by

$$C_b(f) = C(f)\cdot C^*(f) = |C(f)|^2 \tag{A.8}$$

Using these results we obtain the spectrum of PPAM signal $r(t)$ modulated by an iid sequence as

$$S_r(f) = \frac{1}{T}S_x(f)|C(f)|^2 + \frac{R_x(0)}{T}(1 - |C(f)|^2) \tag{A.9}$$

For any arbitrary pulse shape $r_p(t) = r(t) * p(t)$. The power spectral density $(S_{rp}(f))$ of of the PPAM signal $r_p(t)$ is given by $S_{rp}(f) = S_r(f)|P(f)|^2$, where $P(f)$ is the Fourier transform of the pulse $p(t)$. The spectrum $S_{xp}(f)$ of the PAM signal $x_p(t)$ is well known [10] and given by $S_{xp}(f) = |P(f)|^2 S_x(f)/T$. Using this we can reduce the spectrum of PPAM to

$$S_{rp}(f) = S_{xp}(f)|C(f)|^2 + \frac{R_x(0)}{T}(1 - |C(f)|^2)|P(f)|^2 \tag{A.10}$$

One can readily show that for a deterministic sequence x_k, we obtain the same results as derived above. An important point to observe is that the spectrum of a PAM signal is completely determined by the autocorrelation of the samples of the amplitude modulating sequence alone, but in a PPAM signal, the spectrum depends on the probability distribution of the modulating signal a_k as well.

A.1.2 PPM by a pseudo random sequence

In practice the modulating sequence a_k is generated using a PRBS generator. PRBS sequences are pseudo random and the sequence repeats itself with a period M, $a_i = a_{i+M}$. The sequence $b_k = a_i - a_{i+k}$ is also periodic with a period M and $b_k = 0$ for $k = \cdots -M, 0, M, 2M \cdots$. For all other values of k, the sequence is the same as the uncorrelated case.

$$P_{Bk}(b) = \begin{cases} P_A(a) * P_A(-a) = P_B(b) & \text{for } |k| \neq 0, M, 2M \cdots \\ \delta(b) & \text{for } |k| = 0, M, 2M \cdots \end{cases}$$

Using these constraints in Eq. (A.6) and taking its Fourier transform we obtain the spectrum $S_{r,per}(f)$ of the PPAM signal modulated by a pseudo random sequence with period M as

$$S_{r,per}(f) = \frac{1}{T} S_x(f)|C(f)|^2 + \frac{(1 - |C(f)|^2)}{T} S_x(\frac{f}{M}) \tag{A.11}$$

where $S_x(f/M) = \sum_k R_x(kM) e^{-j2\pi fkMT}$. When the impulse amplitudes are not modulated $R_x(k) = 1$, the spectrum reduces to

$$\frac{1}{T^2}|C(f)|^2 \sum_k \delta(f - kf_r) + \frac{(1 - |C(f)|^2)}{MT^2} \sum_k \delta(f - \frac{kf_r}{M}) \tag{A.12}$$

A.1.3 PPM by a binary correlated sequence

When the samples of a_k are not iid $P_{Bk}(b)$ is not constant and the spectrum of the PPAM signal cannot be expressed in terms of the probability distribution of sequence a_k alone. We need to compute $P_{Bk}(b)$ for all k, which depends on the joint statistics of the sequence a_i and a_{i+k}. The spectrum can be computed by modeling the source as a Markov source and the probabilities are computed as a relative frequency of the samples of the signal. The statistics of the sequence b_k can also be computed analytically from the higher order moments of a_k. Since

the probability distribution of b_k depends upon the higher order moments of the modulating sequence, N-PPM is a high non-linear modulation as the sequence length increases.

However when a_k takes on two values the spectrum of PPM as shown later is a filtered version of the spectrum of the modulating sequence.

Let A be a two valued random variable which takes values a_1 and a_2 with probabilities $P_A(a = a_1) = p$ and $P_A(a = a_2) = 1 - p$. The autocorrelation of the sequence a_i is given by

$$R_a(k) = E[a_i a_{i+k}] - \mu^2 \neq 0 \quad \text{for} \quad k \neq 0 \tag{A.13}$$

where $\mu = E[A] = p$ is the mean and μ^2 is subtracted from $E[a_i a_{i+k}]$ to remove the dc offset. Since the random variable A can take only two values (a_1 and a_2), the sequence b_k takes three values $-(a_1 - a_2)$, 0 and $a_1 - a_2$. To compute the probability distribution of the sequence b_k we need three equations, since we have three unknowns.

We use the moments of the random variable b_k to get the three equations

$$E[{b_k}^0] = P_{Bk}(a_2 - a_1) + P_{Bk}(0) + P_{Bk}(a_1 - a_2) = 1$$

$$E[{b_k}^1] = P_{Bk}(a_2 - a_1) - P_{Bk}(a_1 - a_2) = 0$$

$$E[{b_k}^2] = (a_1 - a_2)^2.[P_{Bk}(a_1 - a_2) +$$

$$P_{Bk}(a_2 - a_1)] = 2(R_a(0) - R_a(k))$$

Solving the above equations, we get

$$P_{Bk}(b) = \begin{cases} 1 - 2{\cdot}(R_a(0) - R_a(k))/(a_1 - a_2)^2 & b = 0 \\ (R_a(0) - R_a(k))/(a_1 - a_2)^2 & b = \pm(a_1 - a_2) \\ 0 & \text{otherwise} \end{cases} \tag{A.14}$$

Thus the probability distribution $P_{Bk}(b)$ of the sequence b_k is completely determined by the probability distribution of the sequence a_i and its autocorrelation function $R_a(k)$ when the random variable a takes only two values. Now that we know $P_{Bk}(b)$ for all k, we can substitute it in Eq. (A.6) and obtain the spectrum of the PPAM signal $S_{rc}(f)$ modulated by a correlated binary random variable.

$$S_{rc}(f) = \frac{1}{T}|C(f)|^2 S_x(f) + \frac{4\sin^2(\pi f T_d(a_1 - a_2))}{T}(S_a(f) * S_x(f)) \tag{A.15}$$

The PSD can be further reduced to

$$\frac{1}{T}S_x(f)|C(f)|^2 + \frac{1}{T}\frac{S_a(f) * S_x(f)}{R_a(0)}(1 - |C(f)|^2)$$

where $S_a(f) = \sum_k R_a(k)e^{-j2\pi fkT}$ is the PSD of the sequence a_k, $S_a(f)*S_x(f)$ is the convolution of the two power spectra given by $S_a(f)*S_x(f) = \sum_k R_a(k)R_x(k)e^{-j2\pi fkT}$ and $|C(f)|^2 = \left|pe^{-j2\pi f a_1 T_d} + (1-p)e^{-j2\pi f a_2 T_d}\right|^2 = 1 - 4p(1-p)\sin^2(\pi f T_d(a_1 - a_2))$ and $R_a(0) = (a_1 - a_2)^2 p(1-p)$. When the amplitude of the impulses are not modulated $R_x(k) = 1$, we have

$$S_{rc}(f) = \frac{1}{T}|C(f)|^2 \sum_k \delta(f - kf_r) + \frac{1}{T}\frac{S_a(f)}{R_a(0)} \cdot (1 - |C(f)|^2)$$

An interesting point to note is that binary PPM is a linear modulation with respect to the input modulating sequence. As the number of values taken by the modulating sequence increases the probability distribution of b_k depends upon higher order moments of the modulating sequence a_k. Thus the PSD of the N-PPM signal for $N > 2$ depends on the higher order moments of the modulating sequence. Hence N-PPM is a nonlinear modulation for $N > 2$.

A.1.4 PPM by a two bit correlated sequence

Let $a_c[i]$ be a two bit sequence formed by combining two independently generated one bit sequences $a_1[i]$ and $a_2[i]$ with uniformly distributed ones and zeroes. Let $R_a(k)$ and $S_a(f) = \sum_k R_a(k)e^{-j2\pi fkT}$ be the autocorrelation function and the PSD of the two one bit sequences. The sequence $b_k = a_c[i] - a_c[i-k]$ can take values $\in [-3, 3]$. The probability distribution $P_{Bk}(b)$ of the sequence b_k for all k is given by

$$P_{Bk}(b) = \begin{cases} {P_0}^2 & \text{for } b = 0 \\ {P_1}^2 + P_1P_0 & \text{for } b = \pm 1 \\ P_1P_0 & \text{for } b = \pm 2 \\ {P_1}^2 & \text{for } b = \pm 3 \\ 0 & \text{otherwise} \end{cases} \tag{A.16}$$

where $P_0 = p^2 + (1-p)^2 + 2R_a(k)$ and $P_1 = p(1-p) - R_a(k)$. Now that we know $P_{Bk}(b)$ for all k, we can substitute it in Eq. (A.6) and obtain the spectrum of the PPAM signal $S_{rc}(f)$ modulated by a correlated two bit random variable

$$\frac{1}{T}S_x(f)|C_4(f)|^2 + \frac{2}{T}S_a(f) * S_x(f)\left(\sin^2(\pi fT_d) + \sin^2(3\pi fT_d)\right)$$

$$+\frac{4}{T}S_a(f) * S_x(f)\left(2\sin^2(2\pi fT_d) + \sin^2(\pi fT_d) - \sin^2(3\pi fT_d)\right)$$

where $S_x(f)*S_{a2}(f) = \sum_k R_x(k)(R_a(k))^2e^{-j2\pi fkT}$, $S_a(f)*S_x(f) = \sum_k R_x(k)R_a(k)e^{-j2\pi fkT}$. Though the PSD of the two bit correlated PPM depends only on its autocorrelation function, it is not a linear modulation as its spectrum depends upon the squared auto correlation function as well. When the impulse amplitudes are not modulated ($R_x(k) = 1$), the PSD of the PPM signal is given by

$$\frac{1}{T^2}\sum_k \delta(f - kf_r)|C_4(f)|^2 + \frac{2}{T}S_a(f)\left(\sin^2(\pi fT_d) + \sin^2(3\pi fT_d)\right)$$

$$+\frac{4}{T}S_{a2}(f)\left(2\sin^2(2\pi fT_d) + \sin^2(\pi fT_d) - \sin^2(3\pi fT_d)\right)$$

where $S_{a2}(f) = \sum_k (R_a(k))^2 e^{-j2\pi fkT}$

A.1.5 PPM by a finitely correlated sequence

When the pulse amplitudes are not modulated $R_x(k) = 1$, the PSD $S_{rc}(f)$ of the correlated PPM signal is obtain by taking the Fourier transform of the above equation Eq. (A.6)

$$S_{rc}(f) = \frac{1}{T} \sum_k C_{bk}(f) e^{-j2\pi fkT} \tag{A.17}$$

where $C_{bk}(f)$ is the characteristic function of the random variable b_k for all k. Let $a[i] = \sum_{s=0}^{2} 2^s z[i-s]$, be a three bit uniformly distributed sequence generated by three shifted versions of the one bit iid sequence $z[i]$. Then $a[i]$ and $a[i-k]$ are correlated for $|k| = 0, 1$ & 2 and for any $|k| \geq 3$ the sequences are independent of each other. When the total number of shifts k for which the sequence is correlated is finite, we can express the power spectrum of the PPM signal modulated by a correlated sequence as

$$S_{rc}(f) = \frac{1}{T^2} \sum_k \delta(t - kNf_r) + C_c(f) \tag{A.18}$$

$$C_c(f) = \frac{1}{T} \sum_{l \in L} \left[C_{Bl}(f) - |C(f)|^2 \right] e^{-jl2\pi fT} \tag{A.19}$$

where L is the set of all the values of the time shifts for which the sequence $a[i]$ and $a[i-k]$ are correlated. For the example sequence $a[i]$, the set L is $-2, -1, 0, 1, 2$. It can be seen from Eq. (A.18), the spectrum of the PPM signal is still filtered by the pseudo moving average filter ($C_N(f)$). But the redistributed noise is now dependent on $C_c(f)$ which is a function of the joint distribution of $a[i]$ & $a[i-l]$ for all the values of l for which the sequence is correlated. The first term of Eq. (A.18) has no spurs at kf_r for $k \in [1, N-1]$. For the spurs to be absent in $S_{rc}(f)$, $C_c(f)$ should be finite at these frequencies. $|C_N(kf_r)| = 0$ for a uniformly distributed sequence a_k. $C_{Bk}(f)$ is the Fourier transform of $P_{Bk}(\tau/T)$, which is

real and non-negative and has an unit area. We have

$$|C_{Bk}(f)| < \int_{-\infty}^{\infty} P_{Bk}(\tau/T)d\tau = 1 \tag{A.20}$$

Using these conditions, we can readily show a crude upper bound on the noise level to be

$$S_{rc}(kf_r) \leq \frac{N_1}{T} \tag{A.21}$$

where N_1 is the cardinality[3] of the set L. If N_1 is finite, then $S_{rc}(kf_r)$ converges to a finite value which implies there is no harmonic at kf_r. So for finitely correlated sequences, uniform distribution of the modulating sequence a_k is a sufficient condition for spur elimination.

A.1.6 PPM by a correlated periodic sequence

If the samples of the sequence a_k, in addition to being correlated, are also periodic with a period M then the spectrum of the PPAM signal depends not only on the correlation properties of the sequence a_k but also the redistributed noise is concentrated only on the harmonics of the modulating signal's periodicity. The spectrum of the PPAM signal whose pulse positions are modulated by a sequence that is periodic and correlated can be expressed as

$$S_{rcp}(f) = \frac{1}{T} S_x(f)|C(f)|^2 + C_c(f) \tag{A.22}$$

where

$$C_c(f) = \frac{1}{T} \sum_k \sum_{l \in L} \left[C_{Bl}(f) - |C(f)|^2 \right] R_x(kM + l) e^{-jl2\pi f(kM+l)T}$$

[3]number of elements in L

Assuming only the pulse positions are modulated ($R_x(k) = 1$), the spectrum of the PPM signal is given by

$$S_{rcp}(f) = \frac{1}{T^2}\sum_k \delta(f - kf_r)|C(f)|^2 + C_c(f) \tag{A.23}$$

where

$$C_c(f) = \frac{1}{MT^2}\sum_{l\in L}\left[C_{Bl}(f) - |C(f)|^2\right] e^{-j2\pi flT}\sum_k \delta(f - \frac{kf_r}{M})$$

A similar analysis can be performed like in the correlated case to find the 'reference harmonic strength bound' when the sequence a_k is uniformly distributed. It can be shown that

$$S_{rc}(kf_r) \leq \frac{N_1}{MT^2}\delta(f - kf_r)$$

A.2 Practical considerations for the choice of PRBS length

Let $a[i]$ be a m-bit sequence formed by m single bit sequences $\{z_s[i]\}$. Generally such pseudo random sequence are implemented using a LFSR. A maximum length LFSR of length L is a state machine that goes through $2^L - 1$ states. That is it undergoes all the states except the all zero state. In such a sequence, the number of 1's is equal to 2^{L-1} and the number of zeroes is $(2^{L-1} - 1)$. One can then compute the relative frequency of the occurrence of ones (p) and zeroes($1 - p$) to be $p = P(z_s[i] = 1) = \frac{2^{L-1}}{2^L - 1}$ and $1 - p = P(z_s[i] = 0) = \frac{2^{L-1} - 1}{2^L - 1}$. It is clear from these expressions that p & $1 - p$ are not equal and they approach 0.5 as L increases. So increasing the length of the LFSR ensures that the random binary data generated is of uniform distribution.

If $a[i] = \sum_{s=0}^{m-1} 2^s z_s[i]$, the probability distribution of $a[i]$ is given by

$$P_A(q) = p^q(1 - p)^{m-q}$$

where q is the number of $1'$s in the m-bit number $a[i]$. we can readily see that if $p = 1/2$, then $a[i]$ has an uniform distribution. For a PRBS of length 7, $p = 0.5034$ (which is very close to 0.5). For a 3-bit sequence generated by taking three consecutive tap outputs, we can easily compute $P_A(0) = 0.128$, $P_A(7) = 0.122$, $P_A(1) = P_A(2) = P_A(4) = 0.124$ and $P_A(3) = P_A(5) = P_A(6) = 0.126$ which are all close to 0.125.

APPENDIX B

Ring Oscillator Basics

An n-stage ring oscillator is formed by a cascade of n single pole amplifiers with the final output negatively fed back to the input of the first stage amplifier as shown in Fig. B.1. A cascade of such n-stages ideally should produce sinusoidal output if the Barkhausen criterion is exactly met. However the amplifier gain is prone to process variations and when it's value is smaller than the nominal value, the oscillations will die out with time. Thus in practice the gain is chosen higher than the nominal value to ensure that the system produce sustained oscillations. However when the gain is chosen greater than the nominal value, the output of the oscillator grows unbounded and in practice the amplifiers saturate resulting in a clipped sinusoidal waveform. The following sections analyze the oscillators under such conditions, first assuming that the gain is just sufficient for oscillation and then assuming highly nonlinear amplifiers (saturating non-linearity) and compare their performance in the presence of noise as a function of the number of stages n.

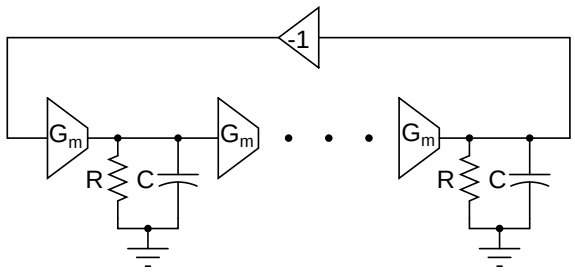

Figure B.1: n-stage ring oscillator

B.1 Sinusoidal ring oscillators

The loop gain the n- stage ring oscillator shown in Fig. B.1 is given by

$$A(s) = \frac{{A_0}^n}{(1 + \frac{s}{\omega_p})^n} \tag{B.1}$$

The closed loop poles of the feedback system are the solutions of

$$1 + \frac{{A_0}^n}{(1 + \frac{s}{\omega_p})^n} = 0 \tag{B.2}$$

Solving this we obtain the closed loop poles as

$$\frac{s_k}{\omega_p} = -1 + A_0 \exp \frac{jk\pi}{n} \tag{B.3}$$

$$\frac{s_k}{\omega_p} = A_0 \cos \frac{k\pi}{n} - 1 + jA_0 \sin \frac{k\pi}{n} \tag{B.4}$$

where $k = 1, 3, ...2n - 1$. From the Barkhausen criteria for oscillation we have $|A(j\omega)| = 1$ and $\angle A(j\omega) = \pi$. For these conditions to be met, since all the stages are identical each stage must introduce a phase shift of π/n. Using this result, we get

$$\frac{\pi}{n} = \tan^{-1}(\omega_{osc} RC) f_{osc} = \frac{1}{2\pi RC} \tan(\frac{\pi}{n})$$

Additionally from the gain constraint ($|A(j\omega)| = 1$) we have

$$A_0 = \sqrt{1 + \tan^2 \frac{\pi}{n}} = \frac{1}{\cos \frac{\pi}{n}} \tag{B.5}$$

using the value of A_0 from Eq. (B.5), and substituting it in Eq. (B.4)

$$\frac{S_k}{\omega_p} = \frac{\cos(k\pi/n)}{\cos(\pi/n)} - 1 + j\frac{\sin(k\pi/n)}{\cos(\pi/n)}$$

since $\cos(k\pi/n)/\cos(\pi/n) \leq 1$, the real part of all the poles are negative except for two cases when $k = 1$ and $k = 2n - 1$, where the real part vanishes and the poles are purely imaginary $(\pm j\omega_p \tan(\pi/n))$. This implies that out of the n poles only two poles contribute to the oscillation and the transients due to the other poles die out over time. From a frequency domain perspective, placing n first order poles in a feedback loop results in a single resonant frequency with an infinite Q and the remaining resonant points have finite Q and hence their natural response die out in the steady state. Hence such an oscillator generates sinusoidal oscillations.If the gain of the amplifier is made larger than the nominal value, then the poles move to the right half s-plane. Thus ideally the system will produce an exponentially growing sinusoid. In reality the amplifiers saturate once the voltage reach the supply voltage level. Thus the amplitude of the sinusoid that is fed back remains same (without increasing exponentially) and the oscillator's output is no longer a sinusoidal signal, but a clipped sinusoid. Section B.2 analyzes such a system and shows the existence of multiple harmonics in the presence of high gain saturating nonlinearities.

B.2 Oscillators with non-linear gain elements

A non-linear oscillator is one that employs high gain non-linear blocks with memory (in this case a delay element) to obtain sustained oscillation. A class of such non-linear oscillator that is of interest to the discussion is shown in Fig. B.2. CMOS based ring oscillators are classic examples of such non-linear oscillators. A CMOS inverter can be modeled as a high gain saturating amplifier with a delay, the delays of n such stages can be combined as a single delay of value T_d and the high gain blocks can be combined to a single slicer as shown in Fig. B.2. One can readily see that feeding an impulse input to the system will produce a sustained oscillation as the impulse is fed back every T_d seconds with opposite polarity. When

an impulse input is fed to the system, the output of the system is given by

$$y(t) = \sum_k \delta(t - 2kT_d) - \delta(t - (2k+1)T_d)$$

It can be easily shown that such an output has harmonics at odd multiples of $f_{osc} = 1/(2T_d)$.

The above result can be intuitively seen from a frequency domain analysis as well. The reminder of the section discusses the result using a linear analysis.

Consider a system with a delay in the feedback path and a memory less unity

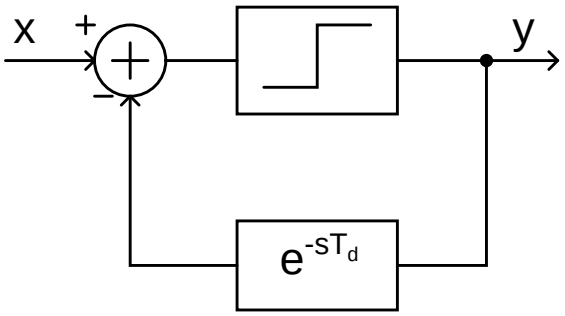

Figure B.2: Nonlinear oscillator

gain in the forward path. The loop gain of such a system is $L(s) = e^{-sT_d}$. The characteristic equation of the system is given by

$$1 + e^{-sT_d}$$

The frequencies at which the system oscillates is determined by the frequencies at which the loop gain becomes -1[1]. The magnitude of the loop gain is unity for all frequencies but the phase of the loop gain reaches π at odd multiples of $1/(2T_d)$. The magnitude of the closed loop transfer function of the system is given by

$$\frac{1}{\cos(\pi f T_d)}$$

[1]In the frequency domain, these are the points at which the close loop transfer function blows up on the $j\omega$ axis.

The magnitude of the closed loop transfer function blows up when $\cos(\pi f T_d) = 0$. That is, when $\pi f T_d = k\pi/2$, k is an odd integer. Thus the system has multiple oscillation frequencies that are odd harmonics of $1/(2T_d)$.

A point to note is that in an all pole system free of delays, when the Barkhausen criterion is met, only a single pair of poles can exist on the $j\omega$ axis and hence only a single frequency of oscillation is possible. However in a system with linear phase delay as discussed above, traditional root locus analysis cannot be used and one has to resort to Nyquist plot for it stability. The Nyquist plot for the system with the linear phase delay is a circle on the imaginary plane. As one increases the frequency, the Nyquist diagram intersects the real axis at -1 infinite number of times indicating the presence of infinite number of poles on the $j\omega$ axis.

Considering the system again with a gain A in the forward path as shown in Fig. B.3. To analyze the general stability of a system, bode plot alone would be insufficient. A bode plot provides the value of the loop gain as a function of frequency and thus is helpful in finding any singularities on the $j\omega$ axis only. If the pole is either in the right half or left half s-plane, bode analysis would not reveal any singularities in the closed loop transfer function. In such a case one has to vary the real part of s and find the appropriate $j\omega$ line where the loop gain exhibits a singularity[2]. In the above example When an impulse is applied to the system, a delayed and amplified version is fed back after T_d seconds and the process repeats indefinitely. If $A < 1$, the magnitude of the fed back impulses dies down exponentially and when $A > 1$, the output grows indefinitely. Thus when $A > 1$, the system is unstable[3]. The closed loop transfer function of the system is given by

$$H(s) = \frac{A}{1 + Ae^{-sT_d}}$$

The inverse Laplace transform is obtained by the series expansion of the above

[2]It can be easily verified that for a transfer function with a right half plane pole, the value on the $j\omega$ axis is finite.

[3]For a bounded input, it produces unbounded output.

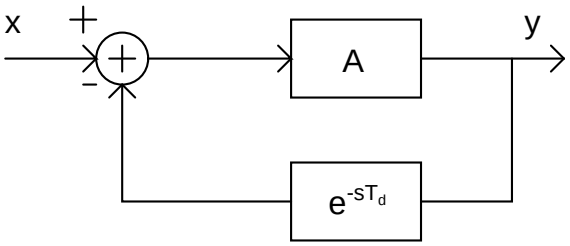

Figure B.3: Delay with gain in the feedforward path.

transfer function

$$\frac{A}{1 + Ae^{-sT_d}} = A \cdot \sum_i \frac{(-Ae^{-sT_d})^i}{i!}$$

The inverse Laplace transform of the above series is

$$A \cdot \sum_{i=0}^{\infty} (-A)^i \delta(t - iT_d)$$

For $A > 1$ the output grows exponentially as expected.

Now consider the system with a saturating gain as shown in Fig. B.2. The saturating gain assumes an infinite gain for signal levels around zero amplitude and a zero gain for values greater than or less than zero. The behavior of the system is very similar to the systems considered above with finite gain. But the amplitude of oscillation is decided by the saturating amplifier shown in Fig. B.2. One can readily see that feeding an impulse input to the system, the output would be very similar to the system with $A = 1$. However as the amplitude of the input is increased, the steady state output amplitude increases proportionately in case of an unity gain amplifier. In case of non-linear oscillator, the amplitude of oscillation is determined by the forward slicer's saturating amplitude (hence it remains constant) and the frequency of oscillation is determined by the delay element in the loop.

B.2.1 Conventional inverter based ring oscillator

In a given technology, the maximum obtainable frequency of oscillation (f_{max}) is the oscillation frequency of the three stage ring oscillator with minimum length devices. Changing the width of the devices increases the current drawn from the supply and also the load capacitance at each stage. Thus the frequency of oscillation which depends upon the rise and fall times of the inverter remains unchanged (since both current and capacitance scale by the same factor). However increasing the length of the devices increases the load capacitance but reduces the current drawn and hence lowers the frequency of oscillation. For an n-stage ring

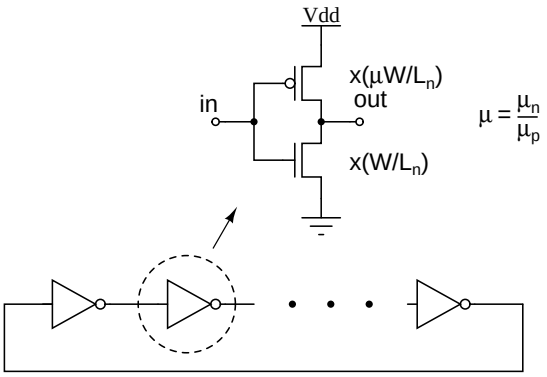

Figure B.4: n-stage inverter based ring oscillator shown with device sizes.

oscillator there is a unique length L_n of the inverter corresponding to a given frequency of oscillation f_{osc} and supply voltage V_{dd}. Since increasing the number of stages demands that the per-stage delay be reduced for the same frequency of oscillation, the value of L_n decreases for increasing n.

$$L_i > L_j \qquad \text{for } i < j$$

The problem is now to decide the number of stages given a target frequency of oscillation.

For a given frequency of the oscillation, the maximum length L_{max} of the inverter used in the ring oscillator corresponds to the one when $n = 3$. That is $L_{max} = L_3$. The frequency of oscillation is inversely proportional to the per stage delay T_d of

the inverter chain. The delay is further proportional to rise (t_r) and fall times (t_f) of the inverter. Assuming symmetric rise and fall times $(t_r = t_f)$, the rise and fall times is proportional to the current provided by the device to charge the output node capacitance. Let I be the current drawn from the supply and C be the output node capacitance, then

$$f_{osc} \propto \frac{1}{nT_d} \propto \frac{1}{nt_r} \propto \frac{I_n}{nC} \propto \frac{1}{nL_n{}^2} \tag{B.6}$$

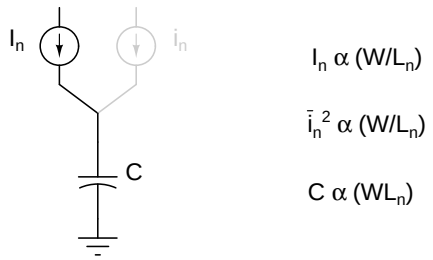

Figure B.5: Model of the inverter as a current charging and discharging a capacitor.

B.2.2 Effect of impedance scaling

For any ring oscillator, as the width of the devices is doubled, the signal current and the output node capacitance doubles (frequency of oscillation remains same). The noise power doubles (3 dB increase). Thus there is a 6 dB increase in the signal power whereas a 3 dB increase in the noise power and the signal to noise ratio improves by 3 dB. So once the number of stages n and the corresponding length L_n is fixed, increasing the width of the devices increases the power consumption and improves the phase noise of the VCO (For every 6 dB increase in signal power, the signal to noise ratio improves by 3 dB).

B.2.3 Noise as a function of n

Let f_{osc} be the desired oscillation frequency such that $f_{osc} < f_{max}$[4]. The minimum number of stages necessary to obtain the desired frequency of oscillation is 3, and the corresponding length is L_3 which is larger than the minimum possible length in a given technology. In practice there exists a maximum number of stages n_{max} that can oscillate at f_{osc}[5]. Thus for a given frequency of oscillation f_{osc}, there are many possible number of stages n (with different lengths), such that $3 < n < n_{max}$. Fig. B.5 shows the model of the inverter in a ring oscillator as a current source I charging (discharging) a capacitor with an additive noise current source I_n. As shown in the figure, the signal current is proportional to the device width to length ratio W/L_n and the power of the noise current is also proportional to the width to length ratio (channel transconductance of the devices). The total power[6] consumed in the ring oscillator is $I_n V_{dd}$. In every cycle of oscillation, the capacitor is charged and discharged by the signal current I_n and the additive noise current i_n. The phase of the VCO output is determined by the signal and noise current as they charge and discharge the output capacitance.

The phase of the signal gets corrupted only when it is transitioning from 0 to V_{dd}. For simplicity of analysis this time is taken to be equal to the rise time of the inverter. The output voltage in the interval $[0, t_r]$ can be written as

$$v_{out}(t) = \frac{I_n}{C} t + \int_0^t \frac{i_n(t)}{C} dt$$

[4] f_{max} refers to the maximum frequency of oscillation of a three stage ring oscillator with minimum lengths.

[5] The maximum number of stages n_{max} can be found by maintaining the lengths of the devices at a minimum and increasing the number of stages till the desired frequency of oscillation is obtained.

[6] In a n-stage ring oscillator the current drawn from the supply is switching between a max and minimum value. The average value of the current is proportional to per stage current I_n and the high frequency zero average current switches at a frequency nf_{osc}. Thus the average power dissipated by a n-stage ring oscillator is given by $I_n V_{dd}$

When $t = t_r$, the signal should ideally reach V_{dd}. That is $V_{dd} = I_n t_r / C$.

$$v_{out}(t_r) = \frac{I_n}{C} t_r + \int_0^{t_r} \frac{i_n(t)}{C} dt$$

$$= \frac{I_n}{C} \left[t_r + \int_0^{t_r} \frac{i_n(t)}{I_n} dt \right]$$

From the above expression the rise time in the presence of noise can be written as

$$t_{r1} = t_r + \int_0^{t_r} \frac{i_n(t)}{I_n} dt \tag{B.7}$$

The amount by which the rise time deviates from its ideal value depends upon the noise current and the signal current injected into the capacitor. This deviation is nothing but the per stage jitter added by the inverter. Let ${\sigma_{dt}}^2$ be the per stage jitter variance, then $t_{r1} = t_r + \sigma_{dt}$. Assuming the noise current to be a zero mean Gaussian noise process with variance ${\sigma_i}^2$. $i_n(t)$ is a stationary random process and the integral version of the gaussian process is a Wiener process [20]. The variance of the integral in Eq. (B.7) is proportional to the integration interval[20] t_r

$${\sigma_{dt}}^2 = \frac{k {\sigma_i}^2}{{I_n}^2} t_r$$

where k is a proportionality constant. The variance of the noise current is proportional to transconductance of the devices, which in turn is proportional to the per stage current I_n for a fixed gate over drive voltage. Thus we have

$${\sigma_{dt}}^2 = \frac{k_1 I_n}{{I_n}^2} t_r = \frac{k_1 t_r}{I_n}$$

The total jitter at the ring oscillator output is the sum of the jitter of the n stages. Let ${\sigma_{tot}}^2$ be the total jitter of the n-stage ring oscillator, then

$${\sigma_{tot}}^2 = n {\sigma_{dt}}^2 = n \cdot \frac{k_1 t_r}{I_n}$$

The figure of merit (FOM) of the n-stage ring oscillator is given by

$$FOM = \frac{1}{jitter \cdot P_d} = \frac{1}{nk_1 t_r V_{dd}}$$

From Eq. (B.6) we have that $f_{osc} \propto 1/(nt_r)$. Thus the FOM can be further reduced to

$$FOM = \frac{k_3 f_{osc}}{V_{dd}}$$

An interesting observation to make is that the FOM is independent of n. Thus for a given frequency of oscillation and supply voltage, the FOM is independent of the number stages in the ring oscillator. As the number of the stages increase the pulse shape also changes. But in case of sinusoidal oscillators, as the number stages increases the per stage delay reduces but the shape of the sinusoidal signal remains the same and there is no advantage due to faster rise/ fall times. Hence for a large n, as the number of stages are increased the signal amplitude does not change, but the noise power changes. Another point to observe is that the FOM is proportional to the oscillation frequency in case of saturating ring oscillators, but inversely proportional to the frequency of oscillation in case of the sinusoidal oscillators.

APPENDIX C

Asymmetric Sidebands in the Presence of both Amplitude and Phase Modulation

C.1 Amplitude modulation

Amplitude modulation (AM) refers to the modulation of the amplitude of the carrier signal proportional to a low frequency modulating signal. The amplitude modulated signal is represented as

$$x_{AM}(t) = A_1(1 + m(t))\cos(2\pi f_c t)$$

The spectrum of the signal contains impulses at the carrier frequency and a frequency translated version of the low frequency modulating signal. For a sinusoidal modulation $m(t) = m_1\cos(2\pi f_m t)$, the time domain signal can be represented as

$$x_{AM}(t) = A_1\cos(2\pi f_c t) + \frac{A_1 m_1}{2}\cos(2\pi(f_c + f_m)t) + \frac{A_1 m_1}{2}\cos(2\pi(f_c - f_m)t)$$

The spectrum of the AM signal modulated by a sinusoidal signal is given by

$$S_{AM}(f) = \frac{A_1}{2}\delta(f - f_c) + \frac{A_1 m_1}{4}\delta(f - f_c - f_m) + \frac{A_1 m_1}{4}\delta(f - f_c + f_m)$$

$$+\frac{A_1}{2}\delta(f + f_c) + \frac{A_1 m_1}{4}\delta(f + f_c + f_m) + \frac{A_1 m_1}{4}\delta(f + f_c - f_m)$$

In case of AM the magnitude of both the sidebands are same and the sidebands are in phase.

C.2 Frequency modulation

In Frequency modulation (FM), the frequency of the carrier signal is modulated proportional to a low frequency modulating signal. The time domain representation of such a signal is given by

$$x_{FM}(t) = A_2 \cos(2\pi f_c t + 2\pi \int_{-\infty}^{t} m(\tau) d\tau)$$

For an arbitrary modulating signal $m(t)$, it is not possible to write a general expression for the spectrum of $x_{FM}(t)$ in terms of the spectrum of $m(t)$. However when the modulating signal is sinusoid, the spectrum of the signal is completely known [10].

For the purposes of the discussion carried out here, we consider an even simpler version of sinusoidal FM called narrow-band FM, where the amplitude of the modulating signal is much smaller than 1[1]. Let the modulating signal be $m_1 \cos(2\pi f_m t)$. The time domain representation of an FM signal modulated by a sinusoid is given by

$$x_{FM}(t) = A_2 \cos(2\pi f_c t + m_2 \sin(2\pi f_m t))$$

where $m_2 = m_1/f_m$. In case of a narrow band FM, the time domain signal can expressed as

$$x_{FM}(t) \approx A_2 \cos(2\pi f_c t) + A_2 m_2 \sin(2\pi f_c t) \sin(2\pi f_m t)$$

$$= A_2 \cos(2\pi f_c t) + \frac{A_2 m_2}{2} \cos(2\pi (f_c + f_m) t) - \frac{A_2 m_2}{2} \cos(2\pi (f_c - f_m) t)$$

The spectrum of the resulting signal is given by

$$S_{FM}(f) = \frac{A_2}{2}\delta(f - f_c) + \frac{A_2 m_2}{4}\delta(f - f_c - f_m) - \frac{A_2 m_2}{4}\delta(f - f_c + f_m)$$

[1]The same conclusions can be drawn even if it were wide band FM. But the complex analysis is avoided for the sake of brevity.

$$+\frac{A_2}{2}\delta(f+f_c)+\frac{A_2 m_2}{4}\delta(f+f_c+f_m)-\frac{A_2 m_2}{4}\delta(f+f_c-f_m)$$

A few points to note here are

- The modulating signals in case of AM and FM are in quadrature[2]
- The sidebands in the narrow band FM signal have opposite polarity.

C.3 Both AM and FM

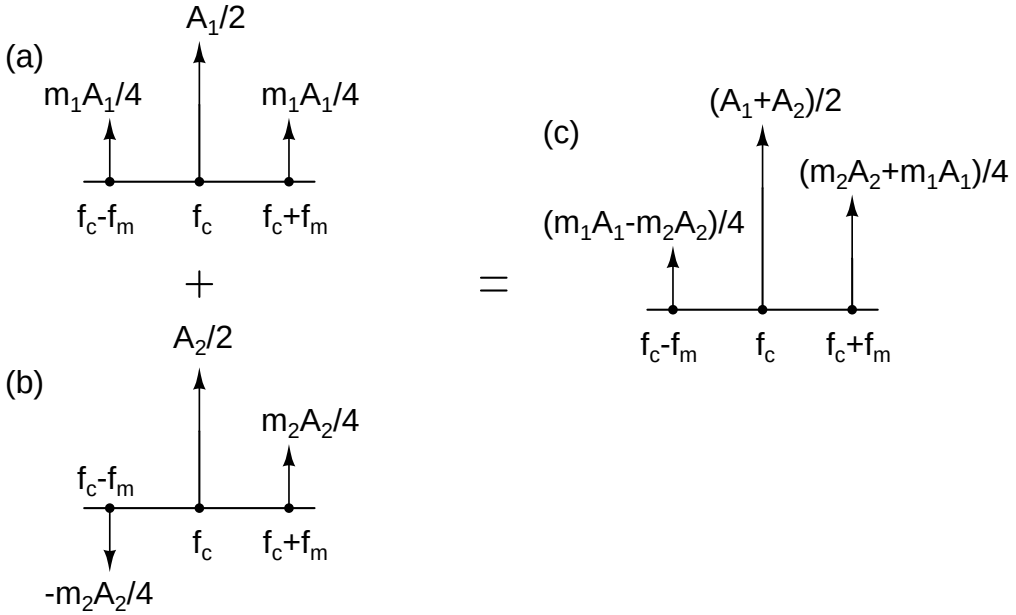

Figure C.1: Asymmetric sideband in the presence of AM and FM. (a) Spectrum of an AM signal, (b) Spectrum of an FM signal and (c) Spectrum of the combined AM and FM signal

Adding the AM signal with an FM signal generates a signal with asymmetric sidebands. Let $x(t)$ be the resulting signal, then the time domain representation is given by

$$x(t)=x_{AM}(t)+x_{FM}(t)=\frac{A_1+A_2}{2}\cos(2\pi f_c t)+\frac{A_1 m_1+A_2 m_2}{2}\cos(2\pi(f_c+f_m)t)$$

$$+\frac{A_1 m_1-A_2 m_2}{2}\cos(2\pi(f_c-f_m)t)$$

[2]This is due to the integration of the modulating signal in case of FM.

The spectrum of the AM and FM signal and the resultant signal obtained by adding the two signals is shown graphically for positive frequencies in Fig. C.1. The spectrum of the signal (for positive frequencies) is given by

$$S_x(f) = \frac{A_1 + A_2}{2}\delta(f-f_c)+\frac{A_1 m_1 + A_2 m_2}{4}\delta(f-f_c-f_m)+\frac{A_1 m_1 - A_2 m_2}{4}\delta(f-f_c+f_m)$$

APPENDIX D

Pin Details of the Fabricated Test Chip

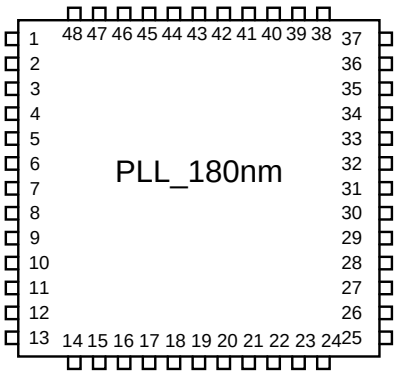

Figure D.1: Pin diagram of the PLL.

Table D.1: Functionality of each pin.

Pin	**Name**	**Functionality**
1, 6, 12, 21, 25, 44	gnd	Ground
2	VDD_PRBS	1.8 V Supply voltage of the PRBS
3	PRBS_EN	Enable signal for the PRBS (Enables PRBS when it is high)
4	REF_CLK	Reference clock signal for the PLL
5	VDD_PFD	1.8 V Suppy voltage for the PFD and delay cells
7, 8, 9, 10	BW_CP0, BW_CP1, BW_LPF1, BW_LPF2	Control bits for charge pump current and loop filter capacitor tuning
11	VDD_DIV	1.8 V Supply voltage for the divider block
13, 14, 15, 16	DIV3, DIV2, DIV1, DIV0	Control bits for changing the divide value (nominal value is '1000')
17	PLL_SEL	Enables one of the two techniques in the PLL
18	VB_VCO_BUF	20 μA current bias input for the VCO buffer

Pin	Name	Functionality
19	VDD_VCO_BUF	2.4 V supply of the VCO output buffer
20, 22	PLL_OUTN, PLL_OUTP	Differential output signals of the VCO buffer
23	VDD_VCO	2.2 V supply voltage for the VCO
24	VCM_BUF	1.2 V common mode bias signal for the VCO buffer
26 and 28	IBIAS_VCO and ITUNE_VCO	1.2 mA and 240 μA current bias inputs for the VCO
27	VDD_REF	1.8 V reference signal for the VCO tuning circuit
29	PLL_VCONT_OUT	Buffered control voltage output of the PLL
30, 31, 32	Vr_cp, VDD_CP, VCM	0.9 V, 1.8 V,0.9 V bias and supply signals for the charge pump
33, 34	VTOP, VBOT	1.4 V and 0.4 V signals for the inverters driving charge pump switches
35	BW_MEAS_EN	when 'high' connects the buffered control voltage output to the PLL_VCONT_OUT pin
36	RST_PRBS	Reset signal for the PRBS
37	VD_EXT	External supply voltage for the delay cells
38	LCK_DET_EN	Enable high signal for the lock detector
39	VCONT_DLL	Buffered control voltage of the DLL
40	DLL_DISABLE	Disable 'high' signal for the DLL
41, 42	VDD_DLL, VCM_DLL	1.8 V and 0.9 V supply and bias voltages for the DLL
43	VBIAS_DLL	current input bias signal for the DLL
45	DLL_REF_CLK	Reference clock for the DLL
46, 47, 48	PRBS_EXT0, PRBS_EXT1, PRBS_EXT2	External PRBS signals for the PLL (Enabled when PRBS_EN=0)

List of Publications Based on the Thesis

- Chembiyan Thambidurai and Nagendra Krishnapura, "Spur Reduction in Wide band PLLs by Random Positioning of Charge pump Current Pulses," in *Proc. 2010 IEEE Int. Symposium on Circuits and Systems (ISCAS)*, June 2010.

- Chembiyan Thambidurai and Nagendra Krishnapura, "On Pulse Position Modulation and its Application to PLLs for Spur Reduction," *IEEE Transaction on Circuits and Systems I : Regular Papers*, July 2011.

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