Design of a 200 kHz Bandwidth 15 bit Continuous Time Delta-Sigma Modulator

A Project Report

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CERTIFICATE

This is to certify that the thesis titled **Design of a 200 kHz Bandwidth 15 bit Continuous Time Delta-Sigma Modulator**, submitted by **Ankur Guha Roy**, to the Indian Institute of Technology Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Finally I dedicate this thesis to my parents and my brother for their much needed support and encouragement through my entire life.

ABSTRACT

The project involves the design of a continuous-time delta-sigma modulator for analog-to-digital conversion. The primary motivation for building continuous-time delta-sigma converters is that the requirements on the anti-aliasing filter are greatly reduced in comparison to their discrete-time counterparts. The proposed third order modulator is operated at 25.6 MHz. It employs a 5-level internal quantizer and targets a resolution of 15 bits for a signal bandwidth of 200 kHz. The modulator's loop filter is implemented with active-RC integrators. Dynamic Element Matching is used to eliminate SNDR degradation due to device mismatch in the DAC elements. Appropriate design techniques are used to make the design robust with respect to process and temperature variations. The design was implemented in 0.18 μm CMOS process from UMC. It occupies an area of 0.7 mm^2 excluding the bond pads and consumes 550 μW static power from a 1.8 V supply. The simulated SQNR for the modulator is 107 dB.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABBREVIATIONS

ADC	Analog to Digital Converter
CIFF	Cascaded Integrators with distributed feedback
CIFF	Cascaded Integrators with distributed feedforward
CMFB	Common Mode Feed-Back
CT	Continuous Time
DT	Discrete Time
DAC	Digital to Analog Converter
DEM	Dynamic Element Matching
DSM	Delta Sigma Modulator
DWA	Data Weighted Averaging
GBW	Gain Bandwidth
LSB	Least Significant Bit
MSA	Maximum Stable Amplitude
MSB	Most Significant Bit
NTF	Noise Transfer Function
OBG	Out of Band Gain
PSD	Power Spectral Density
RNS	Residual Number System
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SoC	System on Chip
STF	Signal Transfer Function
$V_{pp,diff}$	Peak to Peak Differential Voltage

CHAPTER 1

Introduction

1.1 Motivation

A data converter is a key component in many electronic systems. Real world signals are inherently analog; however, the digital form of analog signals can be processed using robust, flexible and reliable digital-signal-processing (DSP). Digital signals are less susceptible to noise. Therefore, analog-to-digital conversion becomes a crucial part in modern days *System-on-Chip* (SoC).

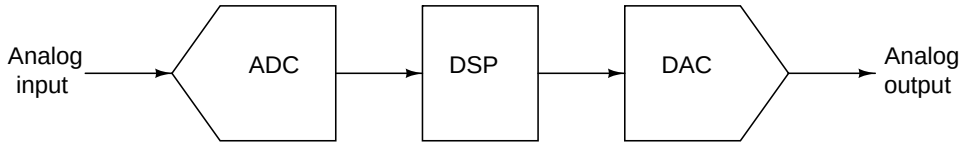


Figure 1.1: A modern signal processing system with DSP core surrounded by data converters

Any ADC is characterized by its resolution (usually effective number of bits), conversion speed and power consumption. The basic idea is to maximize the first two parameters while minimizing the third. Moreover, sampling at high frequency eliminates the need for abrupt cutoffs in the analog anti-aliasing filters. Conventional Nyquist converters require analog components that are precise and highly immune to noise and interference. In contrast, oversampling converters can be implemented using simple and poor-tolerance analog components. Moreover, a technique of noise shaping is used in $\Delta\Sigma$ converters in addition to oversampling to achieve a high-resolution conversion. A significant advantage of the method is that analog signals are converted using simple and poor-tolerance analog circuits and analog signal processing circuits having a precision that is usually much less than the resolution of the overall converter.

Previously, most of the $\Delta\Sigma$ ADC's have been built using discrete-time (DT) circuitry, most often switched-capacitor circuits. The speed of these converters

depends on the settling time of the circuit waveforms. One way of getting around this limitation is to use continuous-time (CT) circuitry in place of DT. Although practice of building CTDSMs for high-speed conversion is proven to be more difficult than anticipated.

In this thesis the design of a high resolution continuous time $\Delta\Sigma$ modulator is presented. The modulator is designed for GSM applications. The theory and design of the building blocks of the modulator is discussed. Impulse-invariant-transformation is used to transform a discrete-time (z-domain) loop-filter transfer function into continuous-time (s-domain). The continuous-time loop-filter is then implemented using an active-RC filter. A method of time constant tuning is also introduced.

1.2 Organization

Chapter 2 introduces the basic theory of $\Delta\Sigma$ modulators, performance measurement and equivalence between a CT and a DT modulator.

Chapter 3 discusses the practical issues related to the design of a $\Delta\Sigma$ modulator.

Chapter 4 explains the design of the loop filter.

Chapter 5 explains the circuit level design of several blocks used in the $\Delta\Sigma$ modulator, viz. design of opamps, internal flash ADC, internal DAC, dynamic element matching block and generation of reference voltages and bias currents respectively.

Chapter 6 discusses measurement and tuning of time constants in a $\Delta\Sigma$ ADC using successive approximation algorithm.

Chapter 7 concludes the thesis with the simulation results.

CHAPTER 2

$\Delta\Sigma$ Modulator Concepts

In this chapter we discuss what a $\Delta\Sigma$ modulator is and how it converts an analog signal into a digital one. The various design choices in $\Delta\Sigma$ modulator design and performance measurement of a $\Delta\Sigma$ modulator is also discussed.

2.1 Operating Principles

Fig. 2.1 shows the basic architecture of a $\Delta\Sigma$ ADC. It is a feedback loop containing a loop filter along with internal low resolution ADC and DAC.

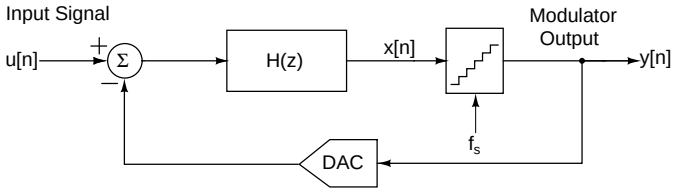


Figure 2.1: Block Diagram of a $\Delta\Sigma$ Modulator

For the system shown in Fig. 2.1 the quantizer is the only non-linear element. A linear model for the system is shown in Fig. 2.2 where the quantizer is replaced by an adder. It is assumed that the adder has two *independent* inputs. The quantization noise added by the quantizer is denoted as e[n]. It is assumed that it is independent of the input signal u[n] and uniformly distributed.

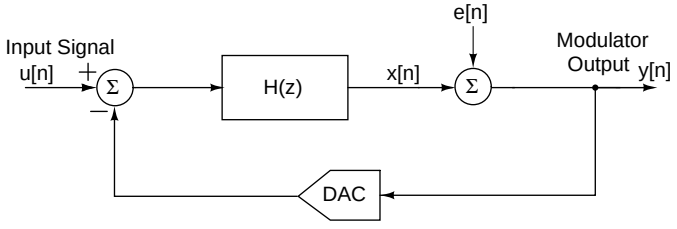


Figure 2.2: Linear model of the Modulator

Let us consider a simple case where $H(z) = \frac{z^{-1}}{1-z^{-1}}$. The output of the modulator y can be written as:

$$y[n] = u[n-1] + e[n] - e[n-1] \tag{2.1}$$

Thus the digital output contains a delayed replica of the input signal and a differentiated version of quantization error e. The differentiation of error signal suppresses it at frequencies which are small compared to sampling rate f_s.

In terms of z-domain analysis,

$$Y(z) = \frac{H(z)}{1+H(z)}U(z) + \frac{1}{1+H(z)}E(z) \tag{2.2}$$

$$= STF(z)U(z) + NTF(z)E(z) \tag{2.3}$$

where $STF(z)$ and $NTF(z)$ are the signal transfer function and noise transfer function respectively. From eq. (2.3) we see that the zeros of $NTF(z)$ are equal to the poles of $H(z)$. The loop filter $H(z)$ has a large magnitude in the frequency band of interest. As a result $STF(z)$ will approximately be unity over the frequency band of interest and the output will resemble the input very closely at these frequencies. Also $NTF(z)$ will be very small over the same frequency band. This process is commonly known as *noise shaping*. Thus, the quantization noise is reduced within the band of interest.

e.g. For a first order $\Delta\Sigma$ modulator H(z) is a simple discrete time integrator i.e. $H(z) = \frac{z^{-1}}{1-z^{-1}}$. Now from equation

$$STF(z) = z^{-1}, NTF(z) = 1 - z^{-1} \tag{2.4}$$

Since $H(z) \to \infty$ at dc, input signals around dc will be reproduced faithfully at the output. The STF is simply a delay, while the NTF is a discrete time high pass filter function.

The modulator minimizes the quantization noise in a bandwidth much smaller than the sampling frequency f_s. To obtain a higher resolution from the converter

the signal must be bandlimited to a value much smaller than f_s. This is achieved by sampling the signal at frequencies much higher than the Nyquist rate i.e. $f_s >> 2f_B$. Hence, $\Delta\Sigma$ modulators are also called *oversampling converters* and the *oversampling ratio (OSR)* of the converter is defined as:

$$OSR = \frac{f_s}{2f_B} \tag{2.5}$$

2.2 Quantizer Resolution

The quantizer used in the circuit can be singlebit or multibit. As specified in [1], multibit quantizers offer the following advantages:

1. For a fixed full-scale, the quantization error reduces by 6 dB for every bit added to the resolution of the quantizer.

2. It improves the stability of higher order modulators. Therefore by choosing sharper NTF, better SNR can be obtained.

3. Non-idealities in the quantizer do not degrade the system performance much because the quantizer is preceded by several high gain integrators. As a result the input referred offset error is small.

The drawbacks of using a multi-bit quantizer are the increase in complexity of the quantizer and the non-idealities in the feedback DAC. Any non-ideality in the feedback DAC is directly referred to the input. So a small error in one DAC level corrupts the converter performance greatly. Hence, it becomes necessary to compensate for multi-bit DAC errors. In contrast, the biggest advantage of single-bit design is that it is inherently linear.

2.3 Discrete-time vs. Continuous-time

Discrete time $\Delta\Sigma$ modulators are constructed with switched-capacitor (SC) loop filters. SC filters are attractive because they offer good accuracy and good lin-

earity. The difference equations describing a SC circuit are independent of the clocking frequency and hence the transfer function of a SC circuit scales automatically with the clock frequency. The continuous-time loop (CT) loop filters have inferior accuracy, linearity and have large variations in their time constants. The CT loop filter transfer function also does not scale naturally with clock frequency, thus requiring calibration for a particular frequency.

The CT $\Delta\Sigma$ modulators have following advantages compared to their discrete time counter parts.

1. *Inherent anti-aliasing* property is one of the biggest advantages of CT modulators. The use of a CT filter postpones the inevitable sampling of the signal, which now takes place at the output of the loop filter. Thus, folding of the wide-band noise take place at a much less sensitive point in the loop.

   Inherent anti-aliasing simplifies system design by eliminating the sharp cut-off anti-alias filter, which typically appears at the input of every other ADC.

2. The maximum clock rate of a CT modulator is determined by the regeneration time of the quantizer and the update rate of the feedback DAC, whereas in a SC modulator the clock rate is determined by the opamp settling time requirements. In practice, a CT modulator operates at a clock frequency 2-4 times greater than that of SC modulators [1].

2.4 CT/DT Modulator Equivalence

The quantizer in a CT $\Delta\Sigma$ modulator is clocked. Hence, there is a sampling action that takes place inside the modulator and sampled circuits are DT circuits. As shown in upper left diagram of Fig. 2.3 the sampling can be made obvious by placing a sampler before the quantizer.

In order to show the equivalence between the CT and DT modulator, the external inputs are set to zero and both loops are opened around the quantizer.

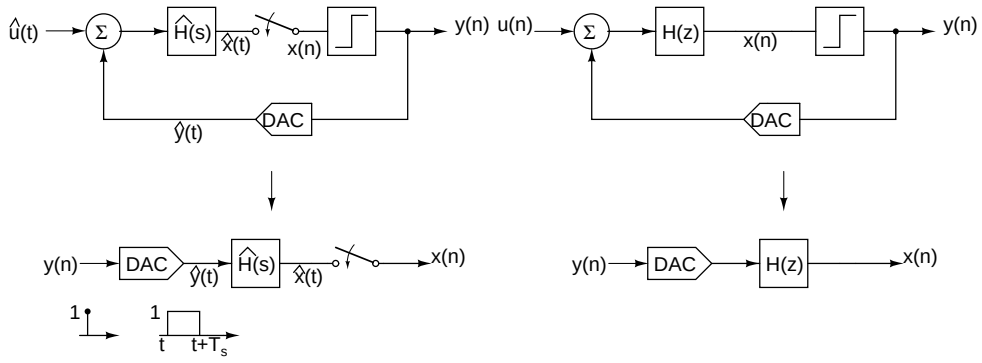


Figure 2.3: Open-loop CT $\Delta\Sigma$ modulator and its DT equivalent

This leads to the two diagrams of Fig. 2.3.

In the CT open-loop diagram, the output of the quantizer is a discrete time quantity. The DAC generates a CT pulse $\hat{y}(t)$ from the output sample y[n] of the quantizer. This pulse is filtered by the CT loop filter to generate $\hat{x}(t)$ which is then sampled to produce the quantizer input x[n]. The input and output of the CT and DT open loop configurations are DT quantities. The CT modulator will produce the same sequence of output bits y[n] as the DT modulator if their quantizer have the same inputs at all sampling instants.

$$x(n) = \hat{x}(t)|_{t=nT_s} \tag{2.6}$$

This would be true if the open loop configurations shown in Fig. 2.3 have the same impulse responses at all sampling times.

$$Z^{-1}\{H(z)\} = L^{-1}\{\hat{R_D}(s)\hat{H}(s)\}|_{t=nT_s} \tag{2.7}$$

Or, in the time domain,

$$h[n] = [\hat{r_D}(t) \otimes \hat{h}(t)]_{t=nT_s} = \int_0^{nT_s} \hat{h}(\tau)\hat{r_D}(nT_s - \tau)\,\mathrm{d}\tau \tag{2.8}$$

$$\tag{2.9}$$

where $\hat{r_D}(t)$ is the impulse response of the DAC. Since the CT and DT impulse responses are the same, this transformation is called the *impulse-invariance transformation* [2].

CHAPTER 3

Implementation Issues in $\Delta\Sigma$ Modulators

In this chapter we take a brief look at the effect of various circuit non-idealities that affect the performance of a $\Delta\Sigma$ modulator.

3.1 Operational Amplifiers

The loop filter of a $\Delta\Sigma$ modulator is usually built by using opamps that are connected as active-RC integrators. If the opamp deviates from its ideal behaviour, the performance of the modulator becomes worse. The various problems associated with opamp non-idealities are discussed here.

3.1.1 Finite Opamp Gain

Instead of infinite dc gain, the opamps have finite dc gain. When an opamp of dc gain A is connected in an integrator configuration, the low frequency gain of the integrator becomes A instead of ∞. For a third order modulator, the dc gain of loop filter is roughly $\sim A^3$. Therefore, magnitude of NTF near DC at dB scale is given by, $20\log(\frac{1}{A^3})$. To keep this value well below the quantization noise floor, the individual dc gains of three opamps are chosen to be more than 50 dB.

A thumb rule that is applicable for both CT and DT modulators is that the dc gain of the opamp, $A > OSR$. This condition ensures that the additional noise that is generated by the finite opamp gain is less than 0.2 dB as against that when $A \to \infty$ [1]. This shows that gain constraint of opamp is not critical.

3.1.2 Gain Bandwidth (GBW)

One of the most important parameters for low power $\Delta\Sigma$ modulator is the gain bandwidth of the opamps that will realize the loop filter.

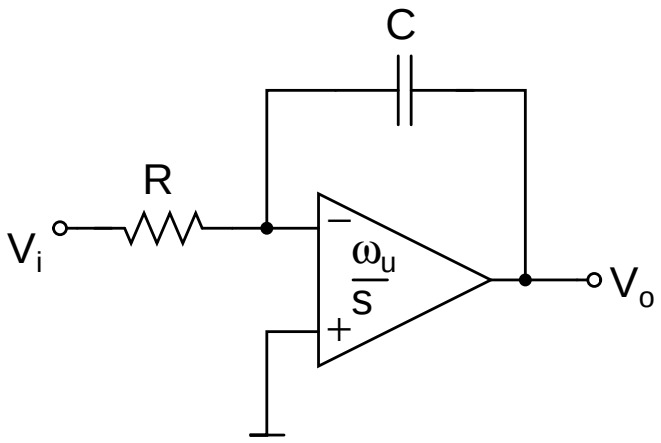


Figure 3.1: Integrator realized using an opamp of GBW ω_u

In [1] it is shown that the transfer function of a real integrator employing an opamp of GBW ω_u is:

$$H(s) = \frac{-1}{sCR(1+k_1)\{1+\frac{s}{\omega_u(1+k_1)}\}} \tag{3.1}$$

Here, $k_1 = \frac{1}{\omega_u RC}$. Assuming the second pole introduced is at sufficiently higher frequency, the unity gain frequency (UGF) of the integrator is reduced by a factor $(1+k_1)$. The additional pole introduces a delay $\frac{1}{\omega_u(1+k_1)}$ in the loop gain. In [3] it is suggested that the GBW of the opamp must be at least an order of magnitude greater than the sampling rate .

3.1.3 Finite Slew Rate

The phenomenon of slewing at the output of an opamp is non-linear. As a result input signal harmonics appear in the output spectrum which degrades the SNDR. In a $\Delta\Sigma$ modulator, the input signal is oversampled. This implies that the input signal is slow compared to the sampling process. Hence, we are more concerned about the slewing of the internal signals, like the output of the loop filter opamps.

3.2 Excess Loop Delay

Excess loop delay is a problem encountered in CT $\Delta\Sigma$ modulators. It is the delay between the arrival of the sampling clock and the change in the output bits as seen at the feedback point in the modulator. Ideally, the DAC current responds instantaneously to the sampling clock pulse. In actuality the transistors in the quantizer have non-zero switching delays. Hence, there is a delay between the quantizer clock and current pulse at the DAC output. This delay is called excess loop delay. It affects the equivalence between the CT and DT representation of the loop filter $\hat{H}(s)$ and H(z). Excess loop delay increases the in-band noise of the modulator and also decreases the maximum stable input amplitude [4]. Hence, the dynamic range of the converter is also reduced.

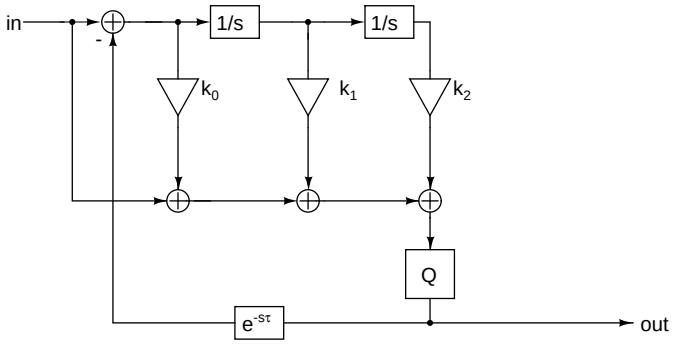


Figure 3.2: Second order CT nodulator with a direct path

As shown in [4], for a second order integrator with NTF $(1 - z^{-1})^2$ having an NRZ DAC, $k_1 = 1.5$, $k_2 = 1$. Usage of a direct path k_0 introduces phase lead compensation, which compensates for the phase lag τ between the two clocks.

Fig. 3.3 shows the first integrator output samples without excess loop delay.

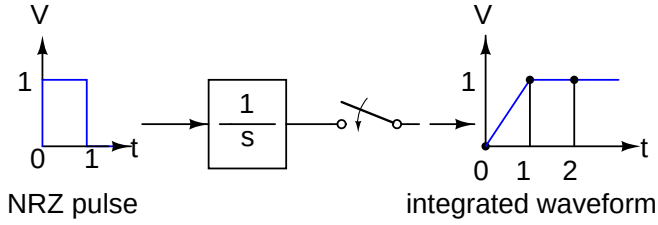


Figure 3.3: 1st integrator output samples for NRZ pulse

In absence of excess loop delay τ the DT equivalent is given by, $\frac{z^{-1}}{1-z^{-1}}$. In presence

of excess loop delay τ the DT equivalent given by,

$$\frac{1-\tau}{z-1} + z^{-1}.\frac{\tau}{z-1} = H_1(z) \tag{3.2}$$

Similarly, as shown in [4], it can be proved for two integrators in cascade, in presence of excess loop delay τ the DT output equivalent of second integrator for an NRZ input pulse is,

$$\frac{(0.5-\tau+0.5\tau^2).z + 0.5(1-\tau^2)}{z-1^2} + z^{-1}\frac{\tau(1-0.5\tau)z + 0.5\tau^2}{z-1^2} = H_2(z) \tag{3.3}$$

For a second order NTF $(1-z^{-1})^2$,

$$L(z) = \frac{1}{NTF} - 1 \tag{3.4}$$

$$= \frac{2z-1}{(z-1)^2} \tag{3.5}$$

Therefore,

$$k_0 z^{-1} + k_1 H_1(z) + k_2 H_2(z) = \frac{2z-1}{(z-1)^2} \tag{3.6}$$

Solving, the following set of simultaneous equations are obtained.

$$k_0 = 1.5\tau + 0.5\tau^2 \tag{3.7}$$

$$k_1 = 1.5 + \tau \tag{3.8}$$

$$k_2 = 1 \tag{3.9}$$

The same idea can be utilized for higher order modulators to find the direct path and integrator output coefficients.

There is another approach to find out the factors k_i [5]. If we closely look at the circuit it is found that there is a delay $e^{-s\tau}$ because of the NRZ pulse delay. Theoretically it can be compensated by adding a block $e^{s\tau}$ in cascade. However,

such a block is non-causal and cannot be realized practically. But it can be expressed as a truncated Taylor series. If denominator is of the order k then the series can be expanded upto $(k+1)^{th}$ term. With this approximation in mind,

$$\frac{k_1}{s}e^{s\tau} \rightarrow \frac{k_1}{s}(1+s\tau) \tag{3.10}$$

$$\frac{k_2}{s^2}e^{s\tau} \rightarrow \frac{k_2}{s^2}(1+s\tau+\frac{s^2\tau^2}{2}) \tag{3.11}$$

For a second order modulator, loop filter transfer function is now,

$$k_1\tau + k_2\frac{\tau^2}{2} + \frac{k_1+k_2\tau}{s} + \frac{k_2}{s^2} \tag{3.12}$$

From this expression,

$$\hat{k_0} = k_1\tau + k_2\frac{\tau^2}{2} \tag{3.13}$$

$$\hat{k_1} = k_1 + k_2\tau \tag{3.14}$$

$$\hat{k_2} = k_2 \tag{3.15}$$

For a second order loop filter with NTF $(1-z^{-1})^2$, $k_1 = 1.5$, $k_2 = 1$. Putting these values,

$$\hat{k_0} = 1.5\tau + 0.5\tau^2 \tag{3.16}$$

$$\hat{k_1} = 1.5 + \tau \tag{3.17}$$

$$\hat{k_2} = 1 \tag{3.18}$$

i.e. the two methods yield same result.

The second method can be generalized for an arbitrary order loop filter in following way:

Here, y_0 is the NRZ pulse. Let, $u(t)$ be the step function and $u_k(t)$ is $u(t)$ integrated

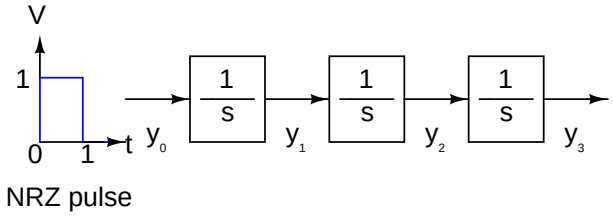


Figure 3.4: Cascade of integrators with NRZ pulse input

k-times.

$$y_0(t) = u(t) - u(t-1) \tag{3.19}$$

$$y_1(t) = u_1(t) - u_1(t-1) \tag{3.20}$$

$$y_k(t) = u_k(t) - u_k(t-1) \tag{3.21}$$

$$y_2(t) = y_2(t-\tau) + \tau y_1(t-\tau) + \frac{\tau^2}{2!} y_0(t-\tau) + \frac{\tau^3}{3!} y_0'(t-\tau) \tag{3.22}$$

If t is an integer, the last term is zero. Therefore, $y_2(t)$ can be reconstructed from $y_2(t-\tau)$ by adding the other terms of previous equation.

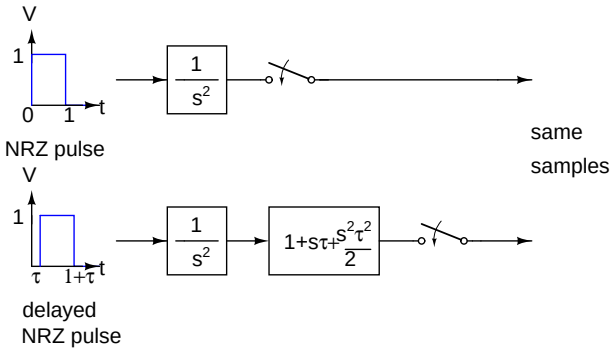


Figure 3.5: Compensation using truncated Taylor series form

In s-domain,

$$Y_2(s).e^{s\tau} = Y_2(s) + \tau s Y_2(s) + \frac{\tau^2}{2!} s^2 Y_2(s) \tag{3.23}$$

Any y_k can be computed in this way.

CHAPTER 4

Loop Filter

The loop filter is the heart of a $\Delta\Sigma$ modulator. It shapes the quantization noise out of the signal band. According to the design specifications we have to reach an SNR of at least 90 dB over a bandwidth of 200 kHz. Using 'Delta-Sigma toolbox' it is found that an SNR of that order can be easily obtained with a third order loop filter, with a reasonable out of band gain (OBG). This chapter deals with the basic properties of a loop filter and design of a third order loop filter for a multibit $\Delta\Sigma$ modulator. The third order $\Delta\Sigma$ modulator gives better noise shaping compared to first and second order modulators with the expense of more complicated hardware.

4.1 High-Order Single-Quantizer Modulators

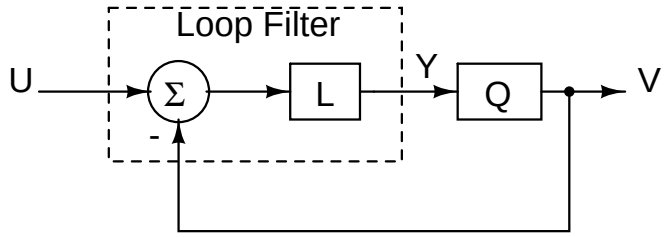


Figure 4.1: Single feedback topology

1. A linear part (loop filter) containing the memory elements.
2. A non-linear memoryless part (the quantizer).

The loop filter can be is modeled as a two input (U and V) single output (Y) system [6]. The output of the modulator, Y can be expressed in terms of two inputs U and V as:

$$Y(z) = L(z)U(z) - L(z)V(z) \tag{4.1}$$

The quantizer is modeled as addition of an error signal to its input.

$$V(z) = Y(z) + E(z) \tag{4.2}$$

Using the above two equations the output of the modulator, V can be written as a linear combination of the input signal U and the quantization error E:

$$V(z) = STF(z)U(z) + NTF(z)E(z) \tag{4.3}$$

where,

$$STF(z) = \frac{L(z)}{1 + L(z)} \quad and \quad NTF(z) = \frac{1}{1 + L(z)} \tag{4.4}$$

There must be at least one clock cycle delay in the loop in Fig. 4.1. Otherwise, a given value of y[n] would change the quantizer output which in turn changes the loop filter input. This sample is then filtered through $-L$ and y[n] would change instantly. Thus the value of y[n] would change continuously during the same period. This delay is accounted for in the noise shaping function $-L(z)$.

Fig. 4.2 shows another special case where a direct path is added to the structure shown in Fig. 4.1. Here, the NTF remains the same as given in equation (4.4) while the STF becomes:

$$STF(z) = \frac{L(z) + 1}{1 + L(z)} = 1 \tag{4.5}$$

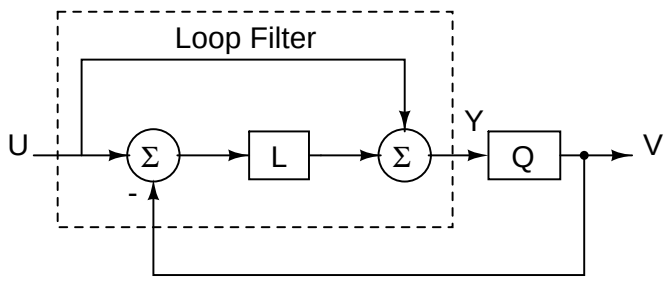


Figure 4.2: Single feedback topology with a feedforward path

Since the signal transfer function is unity the input U appears at the output directly. The loop filter input is given by:

$$U - V = U - (STF.U + NTF.E) = -NTF.E = \frac{-E}{1+L} \tag{4.6}$$

The above equation suggests that the loop filter input no longer contains the input signal component, it has only the filtered quantization noise. This simplifies the design of the loop filter since it need not have very high linearity.

4.2 Loop Filter Architecture

In this section one type of loop filter architecture is discussed.

4.2.1 CIFF Architecture

Figure 4.3 shows the block diagram of a third order loop filter with a CIFF architecture. The zeros of the NTF are realized using the feedforward path.

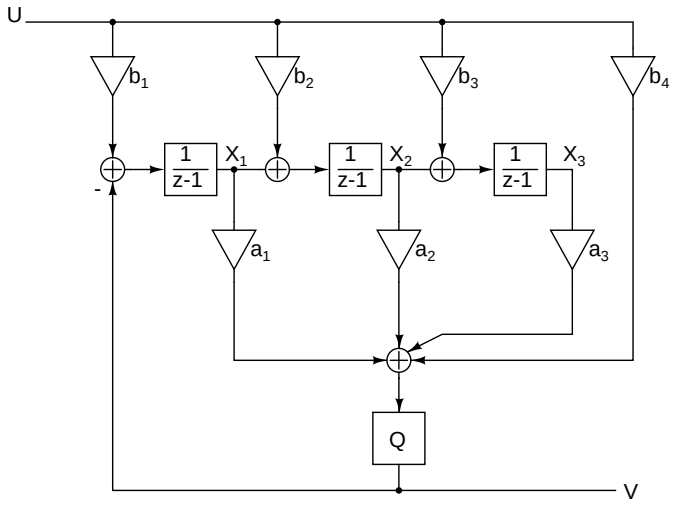


Figure 4.3: Third order CIFF architecture

The transfer function of the feedback filter is:

$$L_1(z) = \frac{-a_1}{(z-1)} + \frac{-a_2}{(z-1)^2} + \frac{-a_3}{(z-1)^3} \tag{4.7}$$

The signal filter function is:

$$L_0(z) = b_1(\frac{a_1}{(z-1)} + \frac{a_2}{(z-1)^2} + \frac{a_3}{(z-1)^3}) + b_2(\frac{a_2}{(z-1)} + \frac{a_3}{(z-1)^2}) + b_3\frac{a_3}{(z-1)} + b_4 \tag{4.8}$$

If $b_1 = b_4 = 1$ and $b_2 = b_3 = 0$. Then from equations (4.7) and (4.8), $L_0(z) = 1 - L_1(z)$ holds, and the STF turns out to be unity. The input to the loop filter is given by:

$$U(z) - V(z) = U(z) - (U(z) + NTF(z)E(z)) = -NTF(z)E(z) \tag{4.9}$$

Thus, the loop filter need not process the input signal and hence, this configuration has low-distortion property.

4.2.2 CIFF Architecture, NTF Zero Optimization

Normally all poles of the $L(z)$ lie at dc (z=1) hence do all zeroes of NTF. A typical way of improving SNR is to optimize the NTF zeroes such that NTF possesses an inverse Chebychev characteristic instead of Butterworth. In this way for a third order modulator SNR can be increased by 8 dB. To obtain optimized zeroes, resonators are created by internal feedback within the loop filter. One such structure is shown in Fig. 4.4. For simplification only first and last input weight factors are included.

4.3 Selection and Implementation of Loop Filter Transfer Function

The first step in the design of a $\Delta\Sigma$ modulator is the choice of the modulator order and its noise transfer function(NTF) [7]. A third order modulator with an OSR of 64 and a 5-level internal quantizer gives a signal-to-quantization noise ratio of around 107 dB. The NTF of the modulator has an out-of-band gain (OBG) of 1.9.

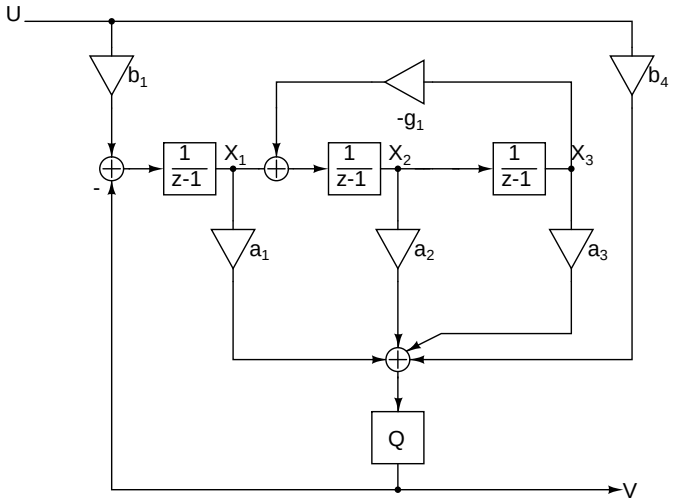


Figure 4.4: Third order CIFF architecture with resonator

OBG is defined as the gain of the NTF at frequencies close to $\omega = \pi$. The NTF zeros are optimised to achieve an inverse Chebyshev characteristic, thus introducing a higher SNR. A modulator with the above characteristics was simulated in MATLAB. The output spectrum of the modulator output is shown in Fig. 4.5.

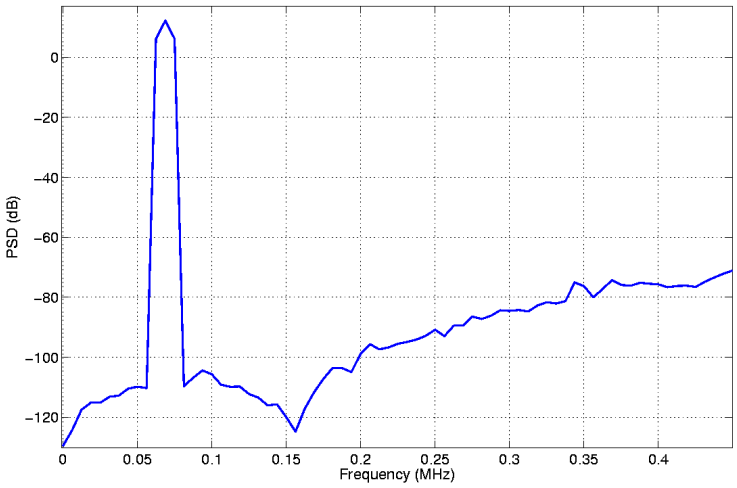


Figure 4.5: PSD of the modulator output

The following steps were followed to find the transfer function of the CT loop filter:

1. Using the Sigma-Delta toolbox in MATLAB the NTF of a third order DT

$\Delta\Sigma$ modulator with an OBG of 1.9 is determined for a sampling rate of 1 Hz.

$$NTF(z) = \frac{(z-1)(z^2 - 1.999z + 1)}{(z - 0.5344)(z^2 - 1.226z + 0.5174)} \tag{4.10}$$

2. The DT loop filter transfer function L(z) is given by:

$$L(z) = \frac{1}{NTF(z)} - 1 \tag{4.11}$$

$$= 1.2385 \frac{z^2 - 0.474z + 0.5842}{(z-1)(z^2 - 1.999z + 1)} \tag{4.12}$$

for a sampling rate of 1 Hz.

3. The impulse invariance transformation is used to determine the transfer function L(s) of the equivalent CT modulator. Excess loop delay of 9 ns is incorporated in finding the equivalent CT transfer function. The normalized sampling rate is 1 Hz.

$$L(s) = 0.2348 + \frac{1.0808}{s} + \frac{0.5460}{s^2 + 0.0014} + \frac{0.1353}{s(s^2 + 0.0014)} \tag{4.13}$$

The above equation for L(s) can implemented by a cascade of three integrators with second and third integrators connected to form a resonator and a summer. Fig. 4.6 shows the block diagram for the implementation of L(s).

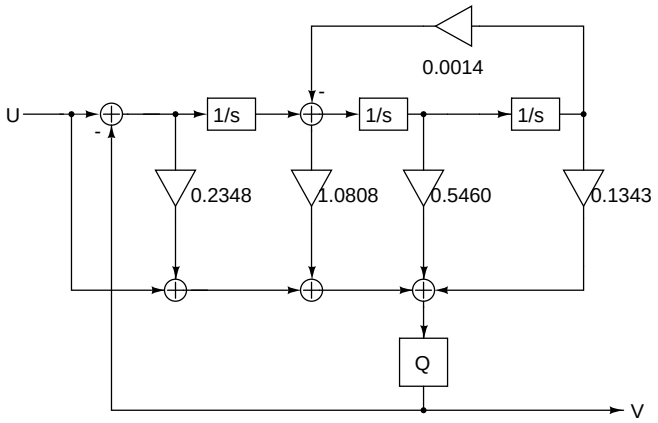


Figure 4.6: Block diagram of third order CT loop filter for $f_s = 1$ Hz

It is now necessary to perform dynamic-range scaling. Dynamic scaling is necessary to ensure that all nodes have approximately the same power level. After dynamic scaling all nodes have the same maximum output level. Dynamic scaling is done as follows: The maximum output level of each integrator is determined by MATLAB simulation. The maximum outputs of all integrators are set to the same level by adjusting their gains. To increase the output level at a node by a factor of k, the input branches should be multiplied by k while the output branches should be divided by k.

The CT model shown in Fig. 4.6 needs to be frequency scaled to the frequency of operation of the modulator i.e $f_s = 25.6\,\text{MHz}$. The loop filter obtained after frequency scaling and node scaling is shown in Fig. 4.7. Here, only single ended equivalent is shown for the clarity of picture. The '-1' gain blocks are implemented by switching the output nets in actual fully differential implementation. The first integrator input resistance is kept at $10\,\text{k}\Omega$ to constrain the in band thermal noise at $70^0\,\text{C}$ so that in band SNR due to thermal noise is $93.5\,\text{dB}$.

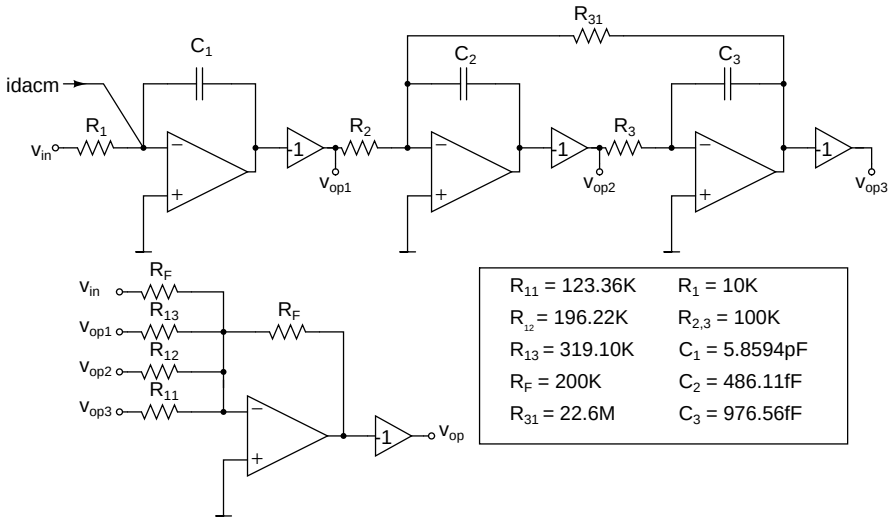


Figure 4.7: Loop filter with ideal op amps for $f_s = 25.6\,\text{MHz}$

4.3.1 Reduction of NTF Zero Optimization Resistance

It is observed from Fig. 4.7 that R_{31} is excessively large for an on chip resistance ($22.6\,\text{M}\Omega$). Here, we are generating a current $\frac{v_{op3}}{R_{31}}$ from a large swinging node v_{op3}. If the node voltage is scaled by means of a potential divider and we take the

voltage from the low swing node, R_{31} can be reduced. The Thëvenin equivalent of the resistive divider circuit is shown in figure 4.8.

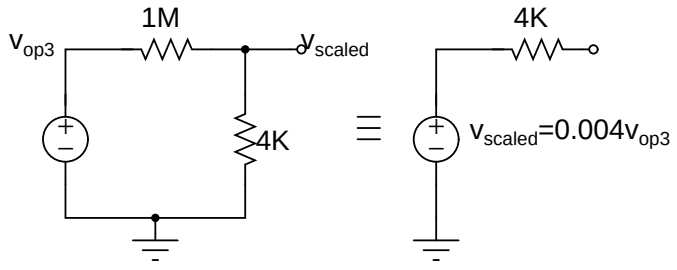


Figure 4.8: Thëvenin equivalent of the resistive divider circuit

R_{31} is now 90.0398 kΩ. From the resistive divider we get 4 kΩ. So externally, 86 kΩ should be connected.

The final structure is shown in Fig. 4.9.

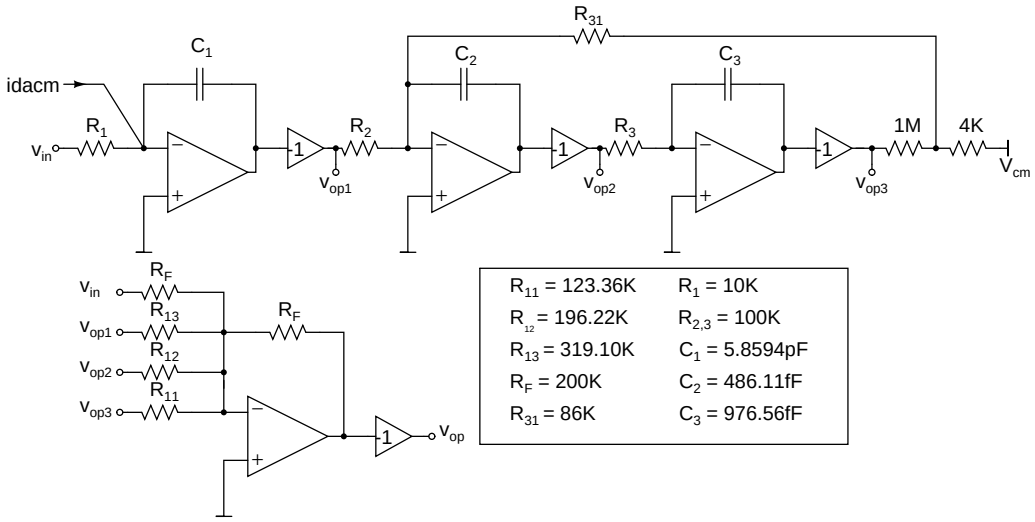


Figure 4.9: Loop filter with ideal op amps and scaled NTF zero optimization resistance

4.3.2 Excess Loop Delay Compensation

9 ns excess loop delay is computed because of the finite GBW of opamps. A way to mitigate this problem is to have a direct path around the quantizer. As worked out in [8] This is achieved by using a feed-in capacitor $C_F = \frac{k_0 R_1 C_1}{R_F}$, where k_0 is the direct path gain. C_F is found out to be 66.79 fF. The strategy is shown in Fig.4.10.

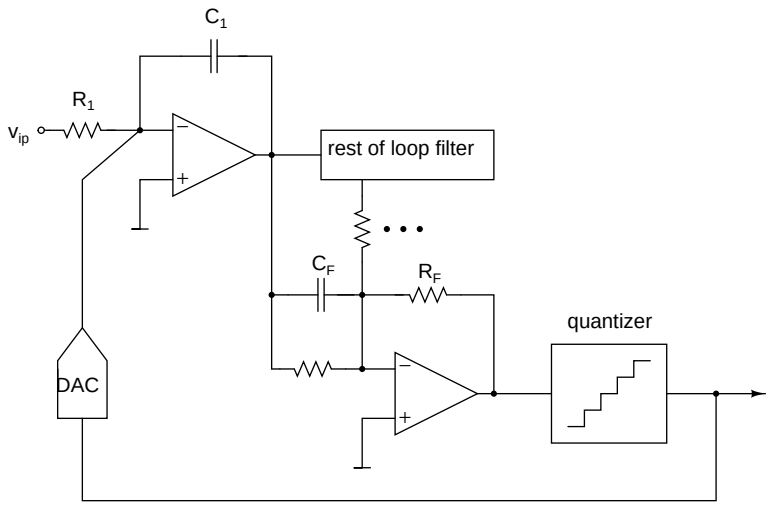


Figure 4.10: Compensation of excess loop delay with feed in capacitor

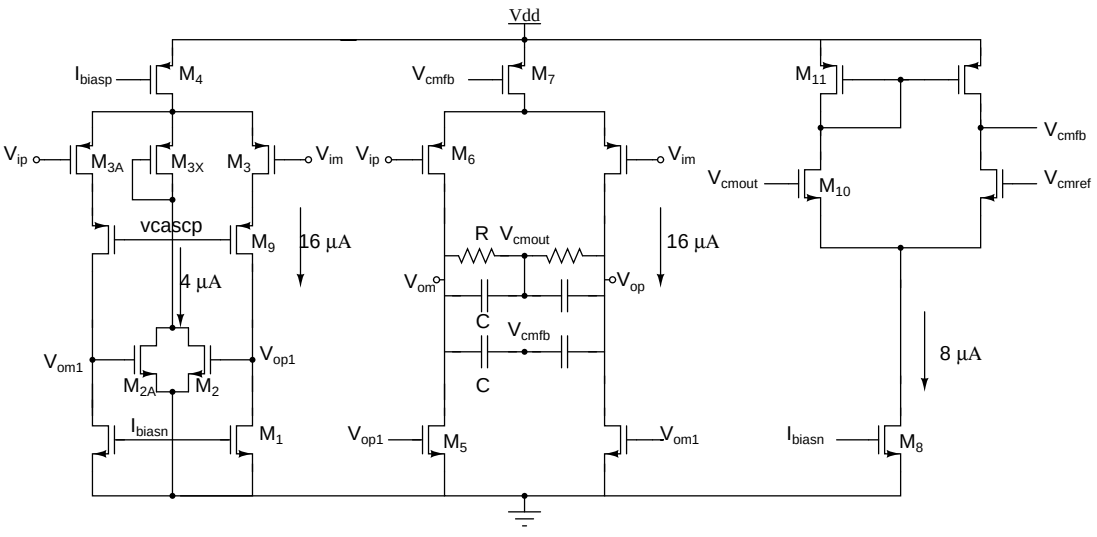
CHAPTER 5

Design of The Various Blocks Used in $\Delta\Sigma$ Modulator

5.1 Operational Amplifier Design

5.1.1 First Integrator Opamp

The first integrating opamp determines the overall distortion and noise of the data converter. Non-linearities of the succeeding opamps become insignificant when referred back to the input. The first integrating opamp is a two-stage design. It is implemented using a feedforward topology. Fig. 5.1 shows the schematic diagram.



M_1- 16(1/10)	M_5 - 16(0.5/1)	M_9 - 16(0.5/0.18)
M_2 - 2(0.5/1)	M_6 - 10(0.5/0.25)	M_{10} - 8(2/0.18)
M_3 - 32(0.5/0.25)	M_7 - 32(2/0.5)	M_{11} - 4(2/0.5)
M_{3X} - 8(0.5/0.25)	M_8 - 8(1/10)	C - 20 fF
M_4 - 38(1/0.5)	R - 1 MΩ	

Figure 5.1: First Integrator Opamp

Noise is an important consideration while choosing the opamp input stage. The major source of noise at low frequencies is the $\frac{1}{f}$ noise of the MOS transistors.

Typically, p-channel transistors have less $\frac{1}{f}$ noise than the n-channel transistors. Therefore, using p-channel transistors for the input stage of the first integrator opamp minimizes the overall input referred noise of the loop filter.

The second stage of the opamp is a class A amplifier. A feedforward stage is added by current reuse method. The second stage of the opamp is frequency compensated. The feedforward opamp employs feedforward compensation. A left half plane zero is introduced between the two poles of the opamp. At unity gain frequency it looks like a first order system. No separate compensating capacitor is required.

We should note that the feed-forward architecture implemented is optimal with respect to power as the feed-forward stage shares current with the second stage. Though the drawback is that this architecture limits the output swing of the opamp. So, to ensure proper operation, the loop filter has been node scaled to $1.2V_{pp,diff}$ ensuring that the integrator swings are well within the swing limits.

The frequency response of fully differential output is shown in Fig. 5.2.

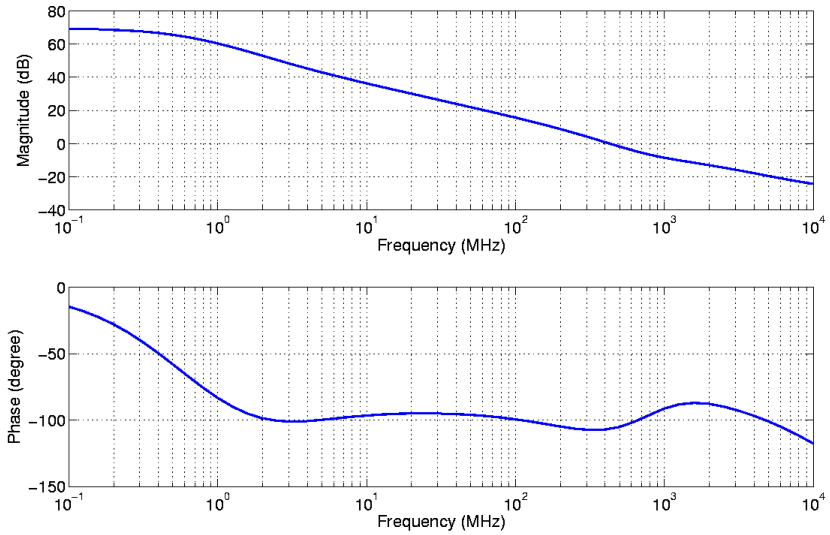


Figure 5.2: First integrator opamp (a) Magnitude response (b) Phase response

Linear Model of First Integrator Opamp

Linear model of first integrator opamp is shown in Fig. 5.3.

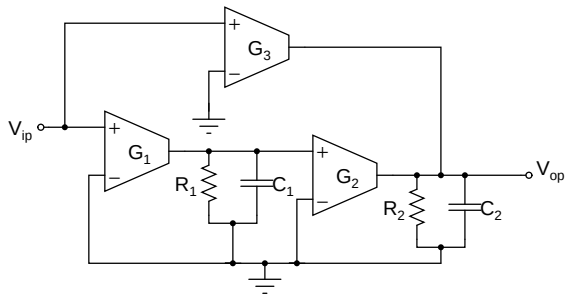


Figure 5.3: First integrator opamp linear model

Here, $G_1 = 246\,\mu$S, $G_2 = 242.8\,\mu$S, $G_3 = 210.3\,\mu$S, $R_1 = 107.673\,\text{k}\Omega$, $R_2 = 39.402\,\text{k}\Omega$, $C_2 = 55\,\text{fF}$.

The calculated dc gain of opamp is $G_1R_1G_2R_2 = 68.07\,\text{dB}$ and UGF $= \frac{G_3}{2\pi C_2} = 608\,\text{MHz}$.

The simulated value of dc gain is 68.01 dB and UGF is 534 MHz.

Common-Mode Feedback Circuits

In fully-differential circuits with feedback, the feedback determines the differential signal voltages, but does not affect the common mode voltages. Hence, additional circuitry is needed to control the output common mode voltage and set it to some specified voltage. This circuitry is referred to as the *common-feedback feedback (CMFB) circuitry.*

First Stage CMFB Circuitry

First stage CMFB circuitry sets the output common mode of the first stage of the opamp. It employs a current mode feedback. The total bias current through M4 is constant. If output common mode of first stage increases, current through M2 and M2A increases. Therefore current through M3 and M3A reduces. This in turn reduces the output common mode voltage of first stage.

Second Stage CMFB Circuitry

The right half simple differential amplifier acts as CMFB circuit that sets the output common mode of the first stage of the opamp. The desired value of the output common mode voltage equals V_{cm}. The output common-mode level is $V_{CMout} = (vop + vom)/2$, where vop and vom are the single ended outputs. The output common-mode level is sensed by the averaging resistors connected between vop and vom. This voltage is then compared with the required output common-mode V_{cmref} by the error amplifier. The output of the error amplifier controls the bias current of the output stage of the opamp.

In order to illustrate the working of the common-mode loop consider the case when the output common-mode exceeds the desired voltage V_{cm}. This causes the current in M7 to increase, thereby output voltage of error amplifier increases. This voltage is the bias voltage that sets the current levels in the pMOS current source M10. The current sources at the output will now pull lower currents from the supply, which will cause the output common-mode voltage to decrease, bringing it back to V_{cm}. Capacitors are connected between the opamp output and the error amplifier output for compensating the common mode feedback loop.

The CMFB circuit's step response is shown in Fig. 5.4.

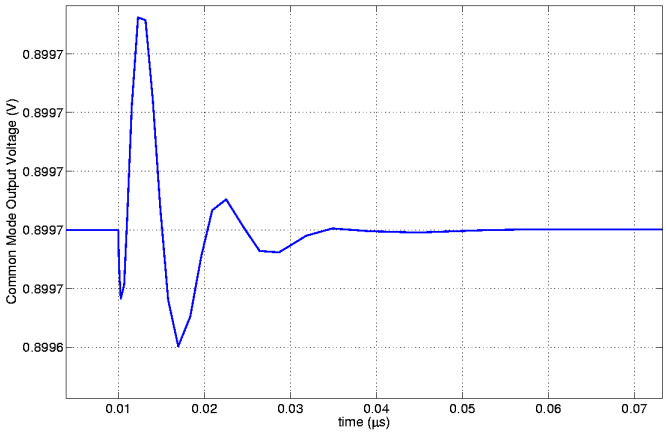


Figure 5.4: Common mode feedback response of first integrator opamp

Noise Analysis

At low frequencies the major source of noise is the flicker noise or 1/f noise of the MOS transistors. In the designed opamp since the first stage has high gain most of the noise comes from the transistors in the first stage. In the noise calculation presented the noise added by the second stage is neglected. The total rms noise at the input of the opamp integrated over 1 KHz to 200 KHz is 5.7549 μV.

5.1.2 Second Integrator Opamp

The second integrating opamp has less stringent specifications on gain, unity gain bandwidth, slew rate and speed in comparison to the first opamp. It also has a feedforward structure but with nMOS input pair. Fig. 5.5 shows the schematic of the second opamp.

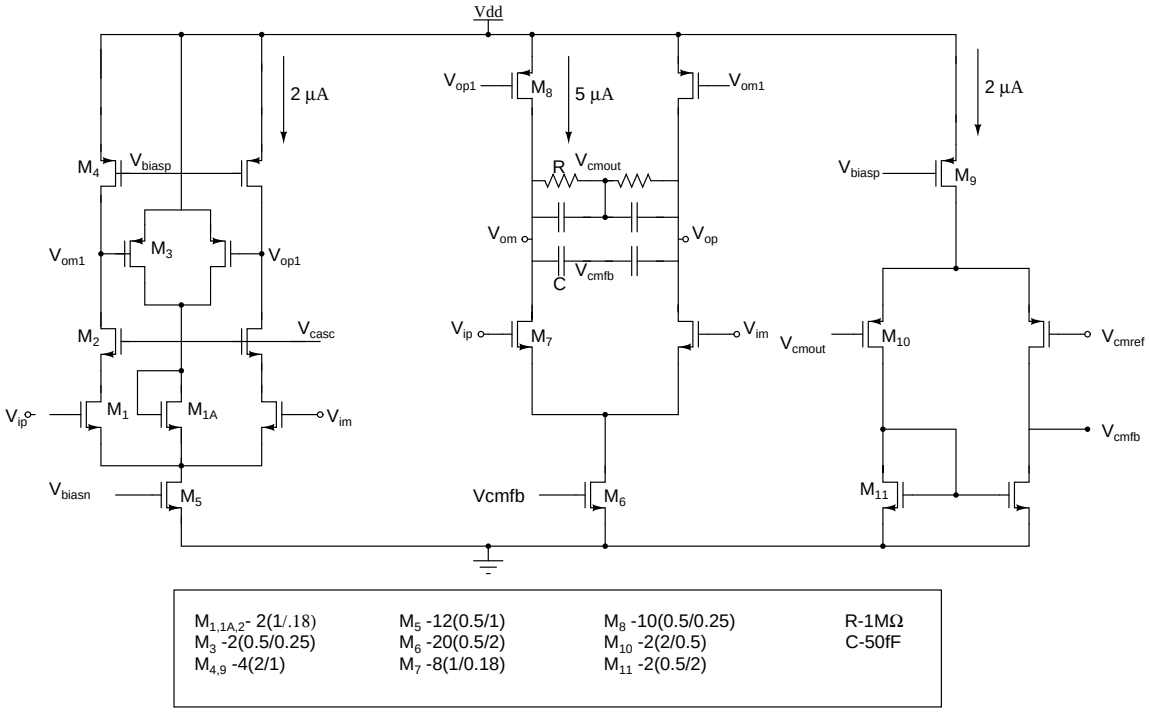


Figure 5.5: Second Integrator Opamp

The input stage is a differential pair of n-channel transistors. The differential pair is cascoded to increase the first stage output impedance and hence the gain. The differential output of the first stage is fed to transistors M13 and M14 of the second stage. A feedforward path with current reusing is implemented by M15

and M16. Like the previous case, no separate compensating capacitor is required. An UGF of 250 MHz and a phase margin of 65^0 is achieved.

The frequency response of fully differential output is shown in Fig. 5.6.

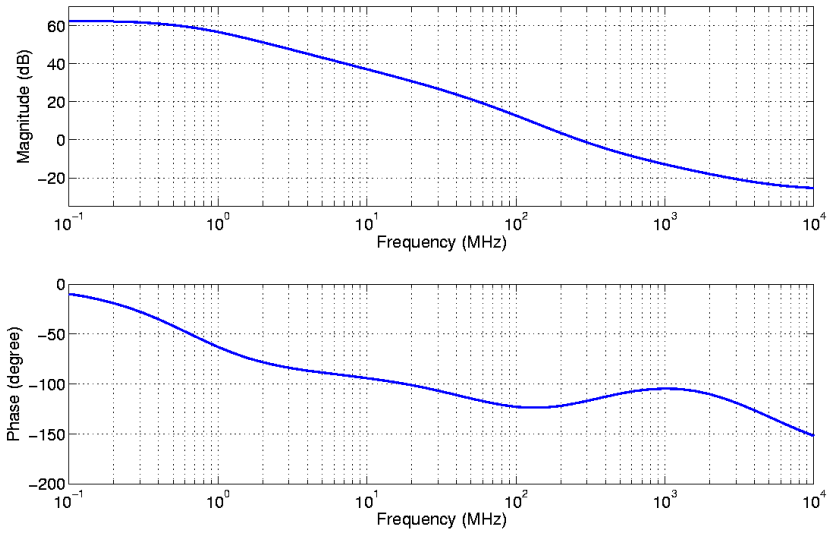


Figure 5.6: Second integrator opamp (a) Magnitude (b) Phase response

CMFB Circuitry

The common mode feedback circuitry acts exactly in the same fashion as first integrator opamp. Only difference is here, the circuit is like exact mirror image with all nMOS replaced by pMOS and vice versa.

The CMFB circuit's step response is shown in Fig. 5.10.

The third integrator opamp of the loop filter has an architecture that is identical to the second opamp except that the CMFB averaging resistors are connected to a series resistance of 4 kΩ each for NTF zero optimization as discussed in chapter 3.

5.1.3 Summer Opamp

The output of the summer should have a very large swing (0.15 V to 1.65 V). It is implemented with a Miller compensated class A 2-stage opamp with 250 MHz UGF

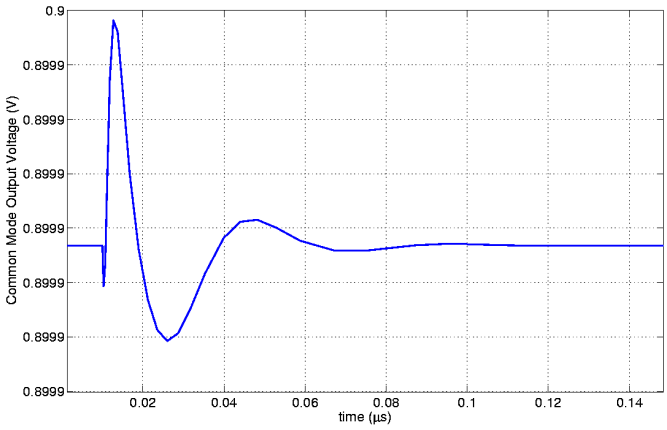


Figure 5.7: Common mode feedback response of second and third integrator opamp

and 50.14^0 phase margin. Fig. 5.8 shows the schematic of the summer opamp.

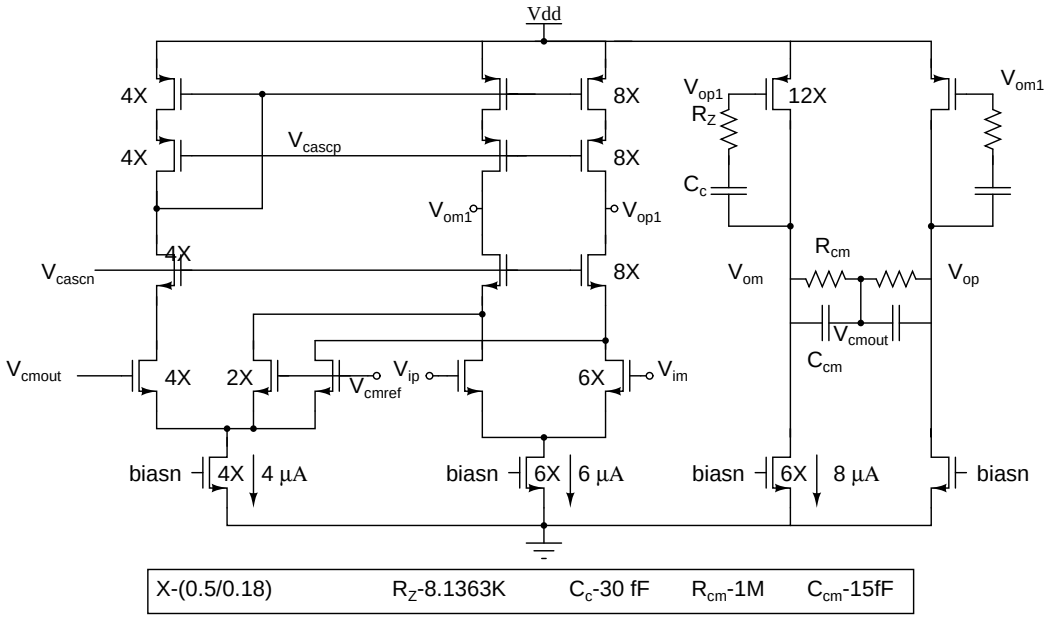


Figure 5.8: Summer opamp

The frequency response of fully differential output is shown in Fig. 5.9.

CMFB Circuitry

It is observed that if the first stage common mode voltage changes that in turn affects the second stage common mode voltage also. So, instead of two separate CMFB circuits, a single one is used that senses the output common voltage at

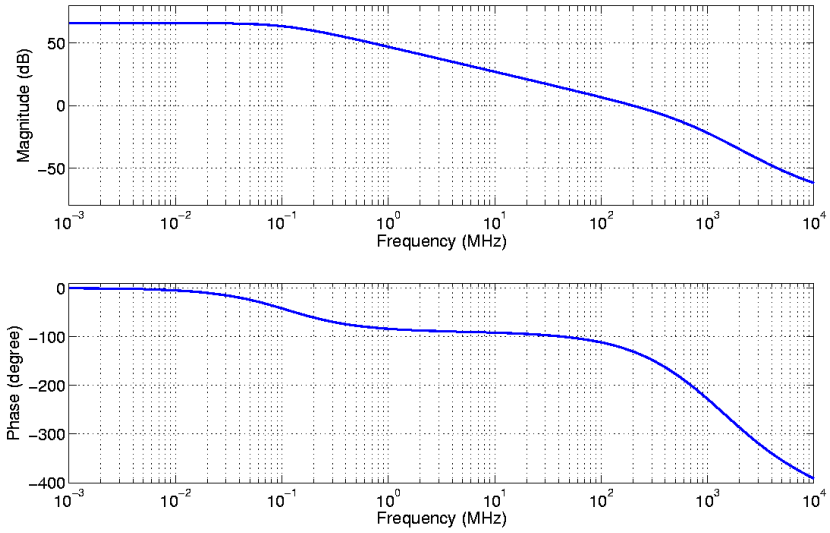


Figure 5.9: Summer opamp (a) Magnitude (b) Phase response

second stage and adjusts first st stage common mode voltage accordingly.

The CMFB circuit's step response is shown in Fig. 5.10.

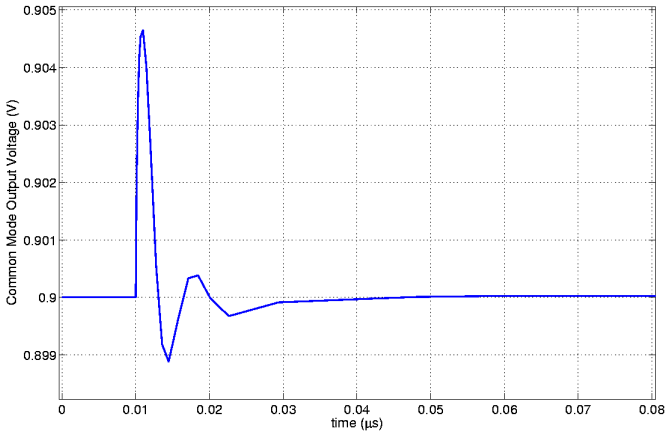


Figure 5.10: Common mode feedback response of summer opamp

5.2 Flash ADC

5.2.1 Introduction

Flash converter is a type of simultaneous type ADC i.e. the working methodology is based on comparing the analog input voltage simultaneously with a set

of reference voltages. It is the standard approach for realizing a very-high-speed data converter. To convert an analog signal to an N bit digital signal, $2^N - 1$ comparators are used in parallel. The basic block diagram of a 5-level differential Flash ADC is shown in Fig. 5.11.

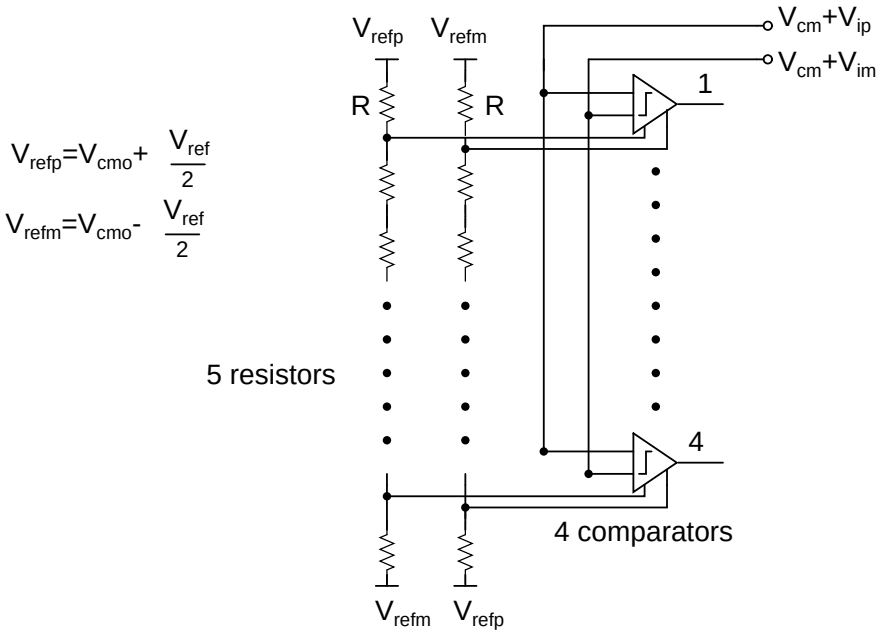


Figure 5.11: The Flash converter

The two resistive ladders provide the differential reference voltage for the comparators. If the differential input voltage to a comparator exceeds its differential reference voltage, the output of the comparator goes high, otherwise it goes low. The Flash ADC gives a thermometer code at its output. A thermometer code is a sequence of ones followed by a sequence of zeroes. The transition point identifies in which range the signal lies. Complexity of the flash converter exponentially depends on the number of bits. However, in our particular case the complexity is fairly simple due to presence of only 4 comparators.

The basic building blocks of the 5-level flash are:

1. Resistive ladder.
2. Comparator.

5.2.2 Resistive Ladder

The resistive ladder is a string of five 100 kΩ resistors that generates the differential reference voltage for the comparators. Larger resistors in the ladder minimize the power consumed by it. For one of the resistive ladders the top and bottom voltages are 1.65 V and 0.15 V respectively. For the other ladder it is just the opposite. The voltage difference between two successive nodes of the resistive ladder is 300 mV. The center node of the two resistive ladders are at $V_{cm} = 0.9\,\text{V}$. In order to minimize the variation in the ladder node voltages, each ladder node is connected to ground by a 2.5 pF capacitor.

5.2.3 Comparator

A standard approach of making the comparator is to use positive feedback. A voltage controlled current source (VCCS) loaded by a capacitor is used. The basic block diagram is shown in Fig. 5.12.The input voltage is sampled across the capacitor. IF $V_{in} > 0$, current is pushed so that voltage across capacitor gradually increases. Just the opposite phenomenon happens if $V_{in} < 0$.

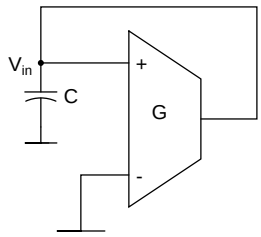


Figure 5.12: Comparator with positive feedback

Say, one infinitesimally small voltage V_1 is applied across the capacitor.

$$C\frac{dV_c}{dt} = GV_c \tag{5.1}$$

$$or, V_c = V_1.e^{\frac{TG}{C}} \tag{5.2}$$

Eventually due to positive feedback this voltage will reach infinity theoretically.

But we can't wait for infinite time. So, we have to specify some regeneration time, which is much less than the time period. So, gain is a function of time. Minimum resolvable voltage by this circuit is, $\frac{V_{DD}}{e^{\frac{TG}{C}}}$. $(\frac{C}{G})$ is called the *regeneration time constant.*

In our circuit, the signal is processed differentially. Therefore, one differential VCCS is required that will measure the difference of input voltages and charge or discharge the capacitances accordingly. One such configuration is shown in Fig. 5.13. Here, if the differential input voltage is positive, current is pushed in top capacitor and pulled from the bottom capacitor. The opposite thing happens if the differential input voltage is negative.

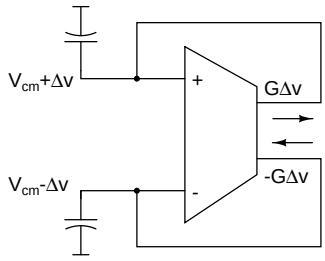


Figure 5.13: Differential Comparator Macromodel

Realization of VCCS

The simplest circuit for VCCS is a CMOS inverter biased at trip point.

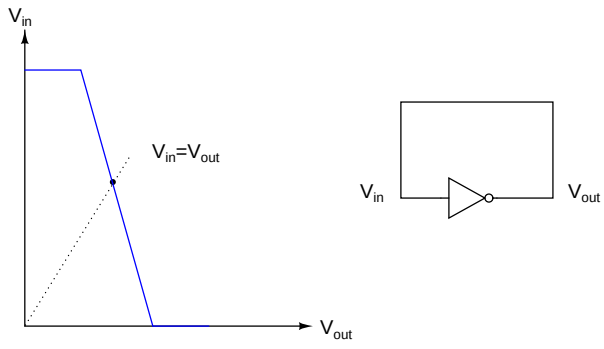


Figure 5.14: An inverter biased at trip point

The inverters have parasitic capacitance at their output and input. So, two inverters when biased at the trip point and driven by small signal differential inputs can act as differential VCCS.

Therefore, the comparator circuit can be drawn as Fig. 5.15.

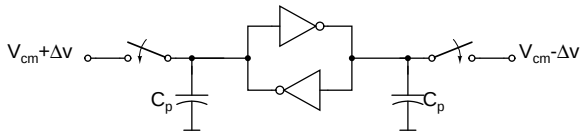


Figure 5.15: Back to Back Connected Inverter

The two switches at input when open helps the signal to regenerate.

The transistor level circuit of the latch is shown in Fig. 5.16.

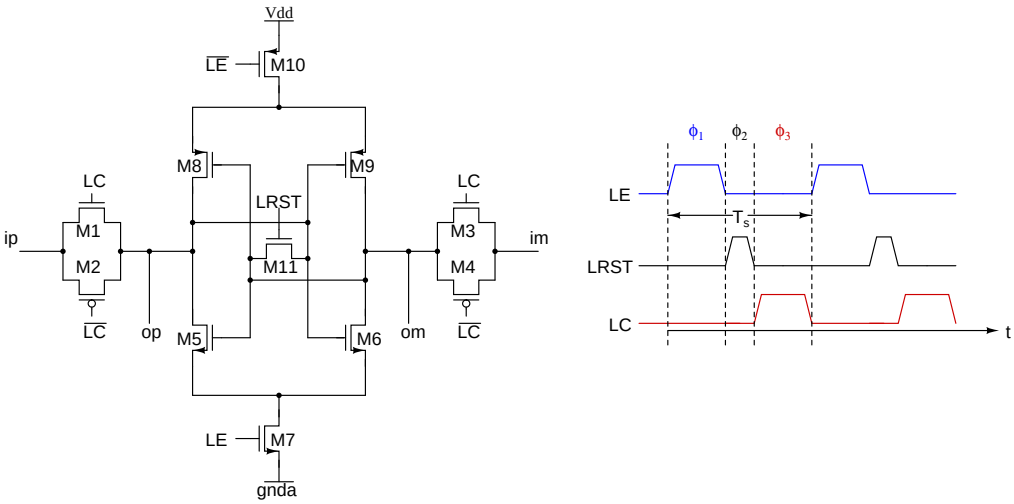


Figure 5.16: Regenerative latch

Transistor	Wμm/Lμm
M1,M2,M3,M4	1(0.24/0.18)
M5,M6,M7,M8,M9,M10	1(0.5/0.18)
M11	2(0.24/0.18)

Table 5.1: Transistor sizes used in latch

The latch has a three phased operation. The three phases are:

1. Track
2. Regeneration and
3. Reset

In the track phase ϕ_3, the parasitic capacitance at the inputs of the latch get charged to the differential input voltages ip and im. The latch as such is in the OFF state because the control signal 'LE' is low. Since no path exists between Vddd and gnda the latch burns zero static power in this phase.

In the regeneration phase, ϕ_1, the latch can be represented by a simplified circuit consisting of two back-to-back inverters.

Due to random mismatches in the threshold voltages of the transistors in the latch, the latch can have an offset voltage. For, the latch to give correct decisions at output the difference between its input voltage must be greater than the offset voltage of the latch. The offset voltage of the latch due to random mismatches can be calculated as follows:

Let g_{mp} and g_{mn} denote the transconductances of the pMOS and nMOS transistors forming the cross-coupled inverter pair in the latch respectively. Let ΔV_{tp} and ΔV_{tn} denote the variation in the threshold voltage of the pMOS and nMOS transistors about their nominal value respectively. The output offset current of the cross coupled inverter pair due to the random mismatches is given by:

$$I_{offset} = g_{mp}\Delta V_{tp} + g_{mn}\Delta V_{tn} \tag{5.3}$$

The output offset current can be represented by an equivalent input offset voltage given by:

$$V_{offset} = \frac{g_{mp}\Delta V_{tp} + g_{mn}\Delta V_{tn}}{g_{mp} + g_{mn}} \tag{5.4}$$

Thus the standard deviation of the offset voltage of the latch is:

$$\sigma_{offset} = \frac{\sqrt{g_{mp}^2\sigma_{V_{Tp}}^2 + g_{mn}^2\sigma_{V_{Tn}}^2}}{g_{mp} + g_{mn}} \tag{5.5}$$

For $(W/L)_{M5,6,8,9}$=0.5 μm/0.18 μm, σ_{offset} = 11.83 mV. The offset voltage of the latch lies between $3\sigma_{offset}$ = $\pm$35.5 mV, which is much smaller than the LSB voltage of flash.

This latch is the basic building block of the comparator shown in Fig. 5.17.

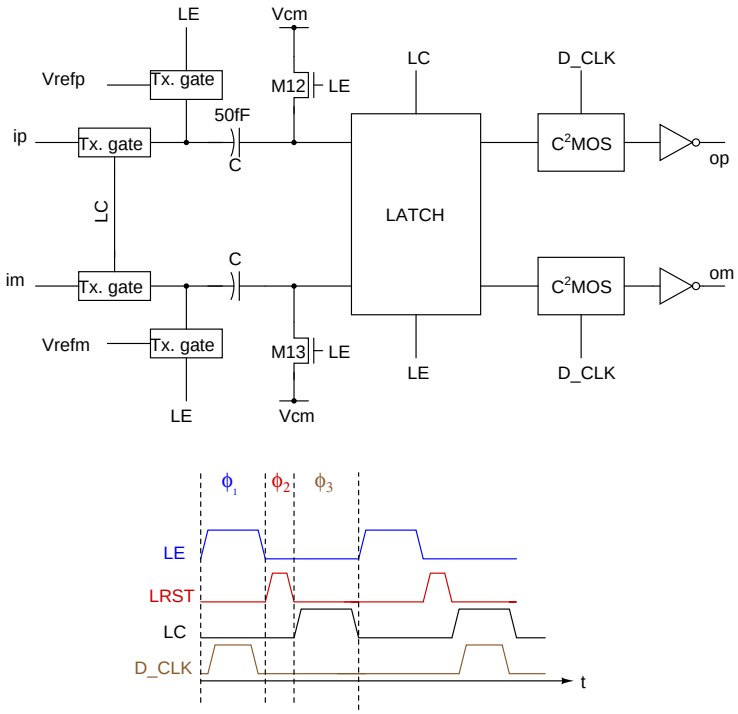


Figure 5.17: Comparator

Transistor	W(μm)/L(μm)
TX gates	1(0.24/0.18)
M12,M13	1(0.24/0.18)

Table 5.2: Transistor sizes used in comparator

During phase ϕ_1 the capacitors get charged to required reference voltages. At the end of phase ϕ_1 the total voltage on the upper capacitor is given by ($V_{cm} - V_{refp}$) and that on the lower capacitor is ($V_{cm} - V_{refm}$).

In phase ϕ_3 the voltage at the two inputs of the latch are:

$$V_{cm} + (V_{ip} - V_{refp}) \tag{5.6}$$

and

$$V_{cm} + (V_{im} - V_{refm}) \tag{5.7}$$

In this phase the regenerative latch is in the track mode as explained in the earlier part.

In phase ϕ_1 the latch goes into the regeneration mode. The positive feedback action in the latch forces its output to go high when $(V_{ip} - V_{im}) > (V_{refp} - V_{refm})$. The comparator gives both true and complementary outputs. The C^2MOS latches the output of the latch after the regeneration is over.

After the regeneration is over, the outputs of the latch are reset in phase ϕ_2 to prepare it for the next conversion cycle.

During ϕ_1 comparator is connected to the resistive ladder, then it draws a small amount of transient current from the ladder to charge the 50fF capacitor.

5.2.4 Flash Clocks

The operation of the Flash requires a pair of non-overlapping clocks viz LE and LC. These clocks determine when the charge transfer occurs and they must be non-overlapping in order to guarantee proper operation of the flash.

One simple method for generating non-overlapping clocks is shown in Fig. 5.18. The clocks CK_a and CK_b gives the non-overlapping clocks. The delays t_{d1} and t_{d2} are realized using a cascade of even number of inverters. The two clocks at the output have the same frequency as the input clock signal.

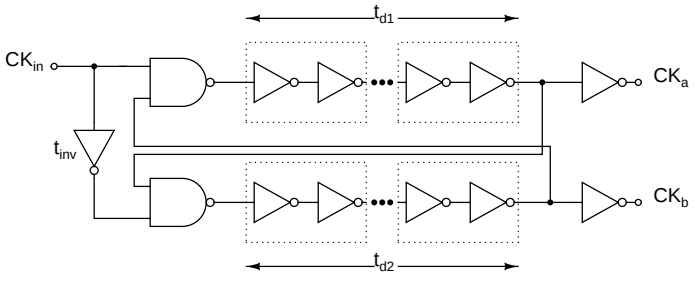


Figure 5.18: NAND clock generator

The latch reset pulse, LRST, must be of sufficient duration to reset the output of the latch to its common mode value. Failing to do so the comparator will take erroneous outputs due to hysteresis. The comparator will consume zero static

power if it is ensured that the LRST pulse and the LE pulse are never high at the same time. LRST is generated by nanding CK_a and CK_b.

The clock to the C^2MOS, D_CLK, should go high only after the output of the latch has reached at the logic level.

5.3 Digital to Analog Converter

5.3.1 Introduction

The Digital to Analog Converter (DAC) converts digital or binary data to its equivalent analog quantity (voltage or current). In noise-shaping modulators employing multibit quantizers, quantization noise power reduces by 6 dB for every additional bit. System stability is also enhanced if multibit quantizer is used. For a DAC with 3 V full-scale and 5 level resolution the DAC LSB voltage is about 600 mV. Hence, the permissible deviation of the DAC output levels from their ideal values is of the order of 300 mV. Therefore the matching characteristics are much relaxed compared to [7].

This chapter discusses the design of the internal multibit current mode DAC and a feedforward current steering DAC used in the $\Delta\Sigma$ modulator.

5.3.2 Feedback DAC

Internal DAC Topology

The most common architecture for the internal N-bit DAC employs $2^N - 1$ parallel unit elements. In such a DAC, the k^{th} output level is generated by turning on k equal valued elements and summing up their currents. Fig. 5.19 shows the schematic of the 4-bit DAC implemented in the design.

For better linearity, the switches in the resistive DAC are implemented by Transmission gates having pMOS size 4 times the nMOS size.

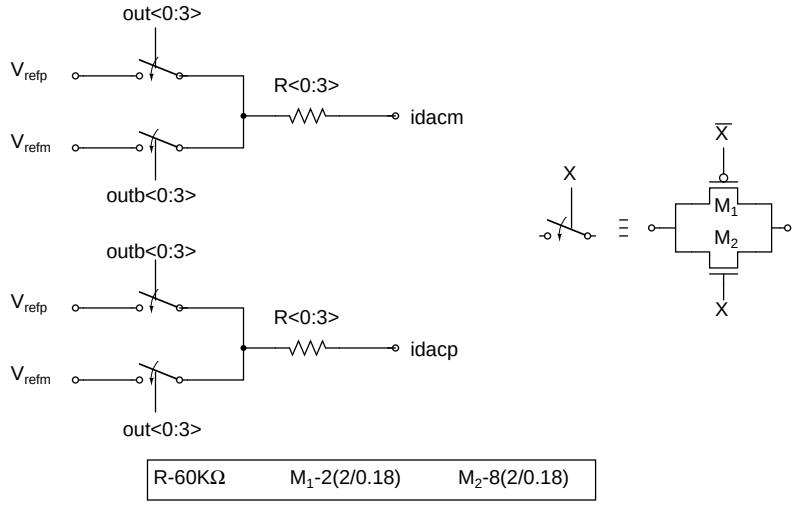


Figure 5.19: Internal DAC schematic

The DAC implemented in the design is a differential resistive DAC. A resistive DAC has been preferred over the conventional current steering DAC because it is less noisy. When the input control bit to any DAC element in the lower section is 1(0) it sources (sinks) a current of half LSB. The reverse is true for DAC cells in the upper section.

When the DAC is non-ideal the low frequency noise shaping of the $\Delta\Sigma$ modulator is lost and harmonics related to DAC errors appear at the output of the modulator within the signal bandwidth. To reduce these effects dynamic matching techniques (DEM) are applied.

Thermal Noise with Feedback DAC

In presence of the resistive DAC, the op input referred thermal noise is multiplied by a factor 4, which is proved below:

Each resistance value is R and the band of interest is B Hz.

$\overline{v_{n1}^2} = 4kTRB = \overline{v_{n2}^2} = \overline{v_{n3}^2} = \overline{v_{n4}^2} = \overline{v_n^2}$ (say)

Consider only the noise source due to R_1. The voltage across opamp input is $\frac{v_{n1}}{2}$. Therefore opamp output noise because of a single resistor is $v_{on1} = \frac{v_{n1}}{2}.A$, where A is the opamp gain. If the opamp input referred noise is $v_{in,OP}$ then output noise component because of opamp's internal noise is $v_{on,OP} = v_{in,OP}.A$

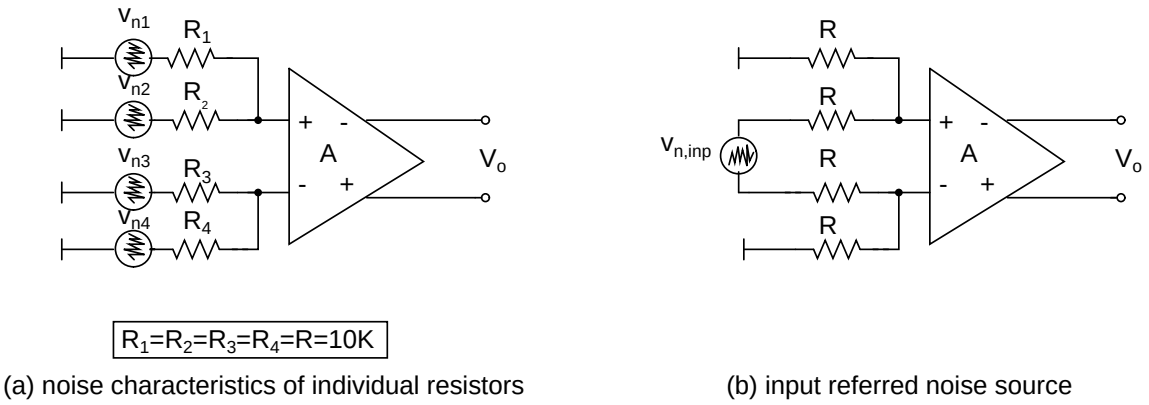


Figure 5.20: Noise response

Since, each noise source is independent, total output noise power is

$$v_{on}^2 = \frac{v_{n1}^2}{4}.A^2 + \frac{v_{n2}^2}{4}.A^2 + \frac{v_{n3}^2}{4}.A^2 + \frac{v_{n4}^2}{4}.A^2 + v_{in,OP}^2.A^2 \tag{5.8}$$

If equivalent input referred noise power is P_{vi} we have

$$P_{vi} = 16kTRB + 4.v_{in,OP}^2 \tag{5.9}$$

Opamp input referred rms noise is $5.755\,\mu$V. Choosing R as $10\,\text{k}\Omega$, the input referred SNR is found to be $\frac{A^2}{2.S_{vi}} = 93.35\,\text{dB}$.

A= 1.2 V (differential input voltage), $T = 70^0$ C, $R = 10\,\text{k}\Omega$, $B = 200\,\text{kHz}$.

5.3.3 Feedforward DAC

Motivation

If a closer loop is taken at the first integrator opamp, it is observed that it takes the difference of $\frac{V_{ip}}{R}$ and $idacm$ and passes the current $\frac{V_{ip}}{R} + idacm$ through the capacitor C_1. This current has to be supplied by the opamp. Since, the opamp used has a class-A stage at the output, it should be designed for maximum possible current to avoid slewing. As implemented in [9], the opamp's quiscent current can be reduced by employing a feedforward DAC. It generates the same current

$\frac{V_{ip}}{R} + idacm$ and feeds it to the output of the opamp. So, virtually the opamp is sitting idly, it doesn't have to provide any external current. It can behave more like an ideal opamp. The quiescent current at the output stage of the opamp can be reduced to a very small value.

Feedforward DAC Architecture

The feedforward DAC comprises of a transconductor block and a current steering DAC. The basic strategy is shown in Fig. 5.21.

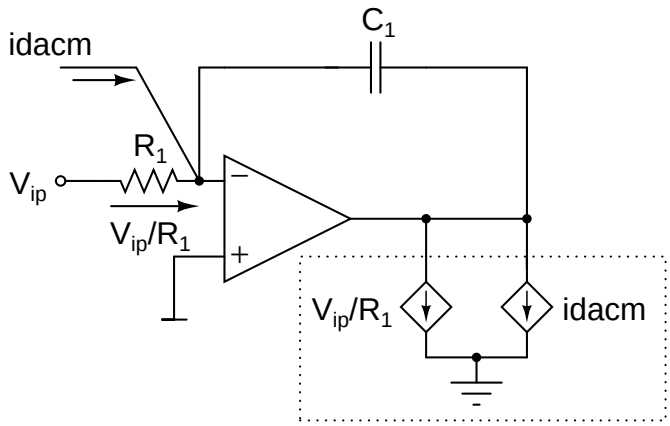


Figure 5.21: Feedforward DAC working method

Transconductor (g_m) Block

The transconductor block is implemented that generates a current $\frac{V_{ip}}{R} + idacm$ and $\frac{V_{im}}{R} + idacp$. The transconductor block is differential in nature. It feeds the current at the o/p of first opamp. So, the opamp quiscent current can be reduced. The input of the transconductor block gets scaled version of a current proportional to input voltage and output code respectively and subtracts them. The structure of transconductor is class AB so that it can drive a large current even though biased in a small quiescent current condition. The transconductor block is shown in Fig. 5.22.

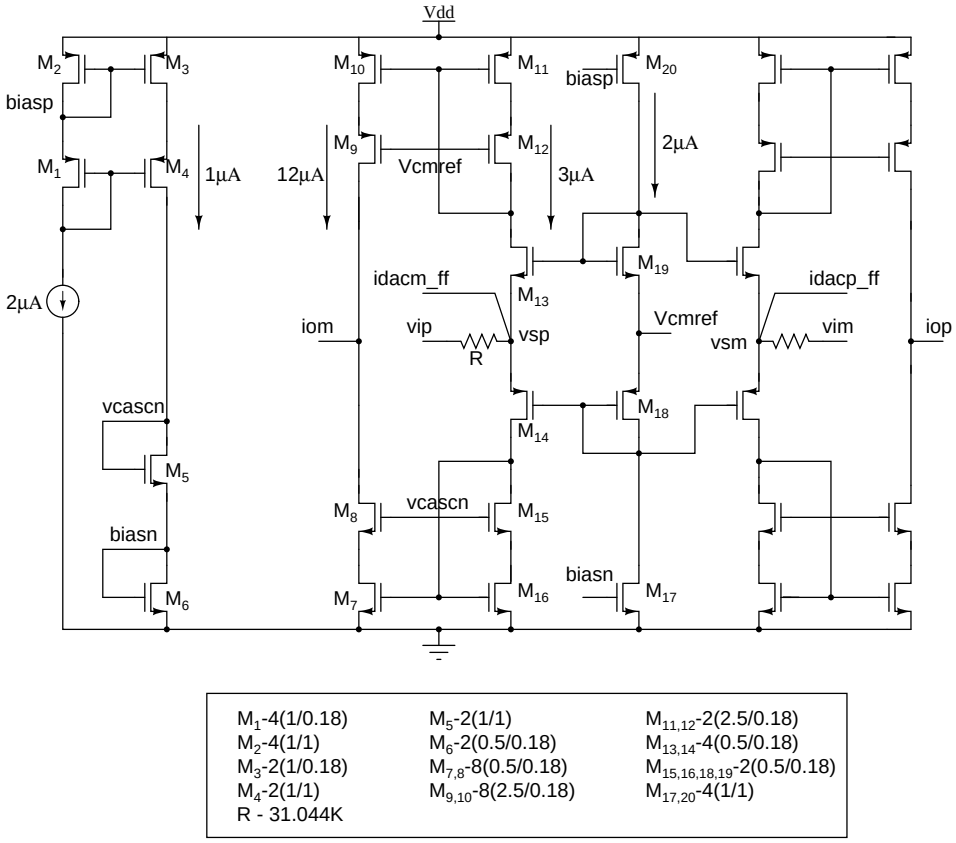


Figure 5.22: Internal DAC schematic

Current Steering DAC Structure

The differential current steering DAC structure is shown in Fig. 5.23.

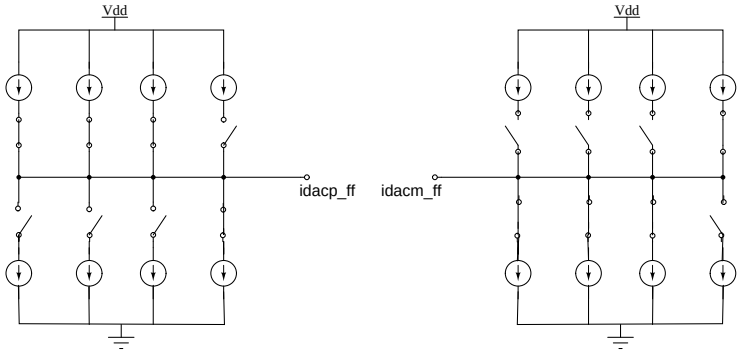


Figure 5.23: current steering DAC

The current steering DAC comprises of a resistor servo (Fig. 5.24) to generate a current that tracks the process dependence of resistor. The generated current through the resistor servo is replicated to make the unit current cells (both p and

n type).

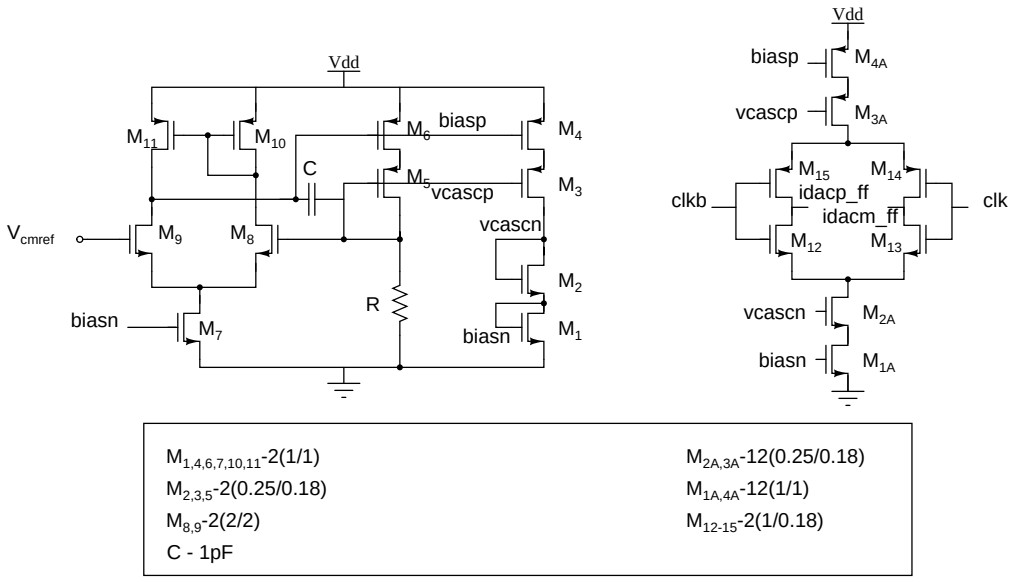


Figure 5.24: Resistor servo and one current steering DAC cell

In the resistive feedback DAC, each current cell (p & n) carries a current of $15\,\mu$A. Let the resistor servo has a reference resistance R. By small signal ac analysis it is observed that for a small signal current injected in virtual ground of transconductor block, it has a current gain of 3.8333 at output node, then current generated by each p & n cell in the current steering DAC structure is $\frac{0.9}{R} \times 6\,\mu$A

Hence, $\frac{0.9V}{R} \times 6 \times 3.8333 = 15\,\mu$A

i.e. or, $R = 1.38\,\mathrm{M}\Omega$

Fig. 5.25 shows the current supplied by feedforward DAC and the difference current supplied by first integrator opamp.

Limited Swing Circuit

The current steering DAC control voltage need not be supplied from rail to rail. A difference of $\sqrt{2}.V_{dsat}$ is enough for swinging the current entirely through the two branches. A swing limited circuit is implemented that limits rail to rail swing to 1V peak to peak differential. The basic idea is to generate the limited reference voltage by unity gain follower circuit and driving them as Fig. 5.24 shows the basic

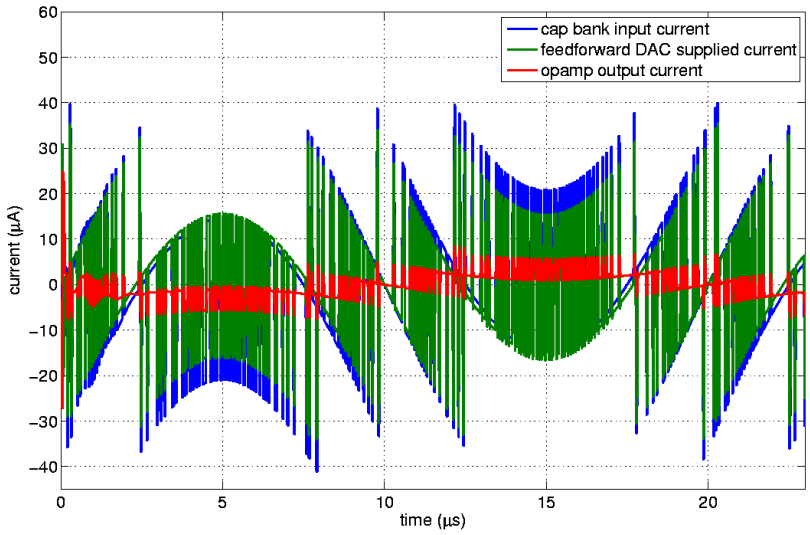
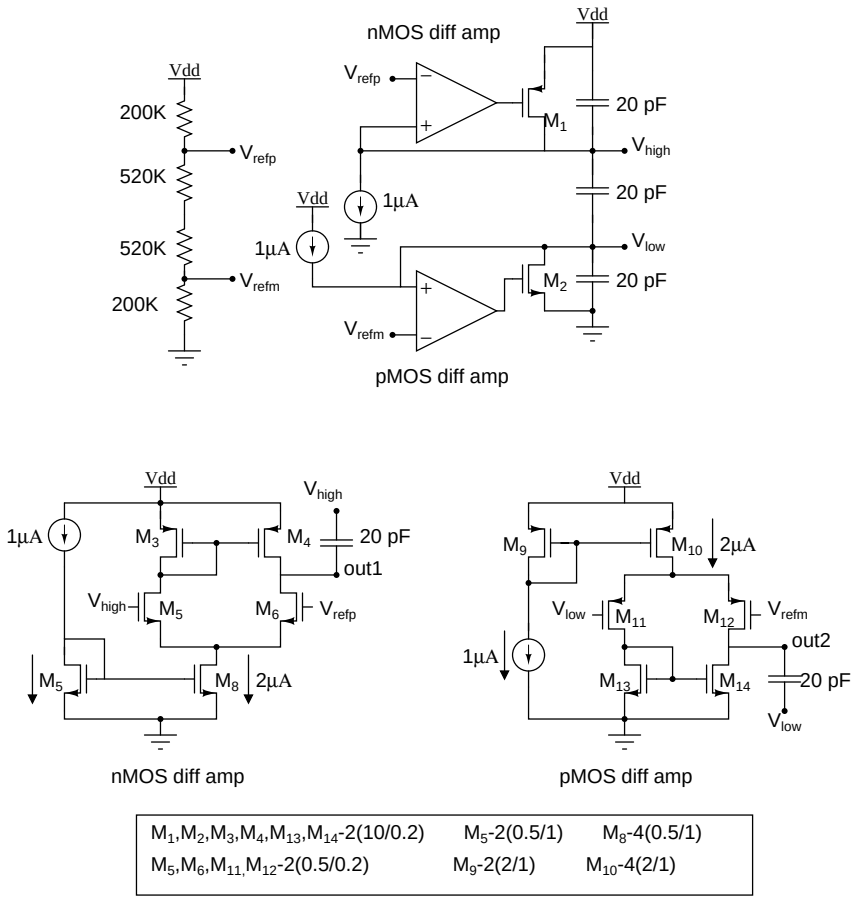


Figure 5.25: Current supplied by feedforward DAC, first integrator opamp

circuit implemented.



M_1,M_2,M_3,M_4,M_{13},M_{14}-2(10/0.2)	M_5-2(0.5/1)	M_8-4(0.5/1)
M_5,M_6,M_{11},M_{12}-2(0.5/0.2)	M_9-2(2/1)	M_{10}-4(2/1)

Figure 5.26: Swing limiter for current steering DAC

5.4 Dynamic Element Matching (DEM)

DEM modulates mismatch errors away from the signal bandwidth. The DAC elements are selected in such a way that the DAC errors sum to zero over multiple sample instances. The static DAC errors are converted into a wide-band noise signal.

By choosing the DAC elements at random the DAC error at the output averages out to zero quickly thereby moving the distortion due to DAC component mismatch to higher frequencies. Subsequent filtering leaves the signal band free of distortion. A technique called data weighted averaging is used to implement DEM [7].

5.4.1 Data Weighted Averaging (DWA)

The DWA technique uses all the DAC elements at the maximum possible rate. This is done by sequentially selecting the DAC elements, beginning with the next available unused element. Fig. 5.27 explains the concept of the DWA algorithm.

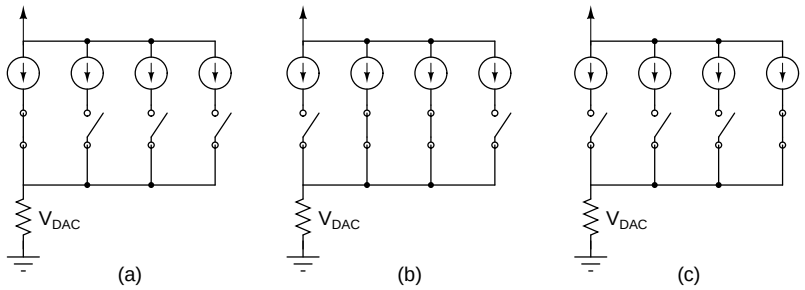


Figure 5.27: DWA element selection for a 5-level DAC with an input sequence of 0001,0011,0001

The first element is turned ON when the input bit pattern is 0001 as shown in Fig. 5.27(a). When the input sequence 0011 is applied the next two elements are turned on as shown in Fig. 5.27(b). Finally when the input sequence 0001 is applied the last DAC element is selected. This selection procedure continues as the input data is applied.

The element averaging is controlled only by the input sequence. Hence, this

algorithm is called 'data weighted averaging'. Since all the DAC elements are used at the maximum possible rate it ensures that the DAC errors quickly sum to zero thereby moving distortion to higher frequencies. An added advantage of the DWA technique is that the distortion spectra from the DAC linearity errors are first order noise shaped [10]. This offers a dynamic range improvement of 9 dB/octave.

5.4.2 DWA Implementation

Fig. 5.28 shows the block diagram of DWA algorithm implemented in the design.The basic building blocks are:

1. Accumulator
2. Barrel Shifter
3. Latch

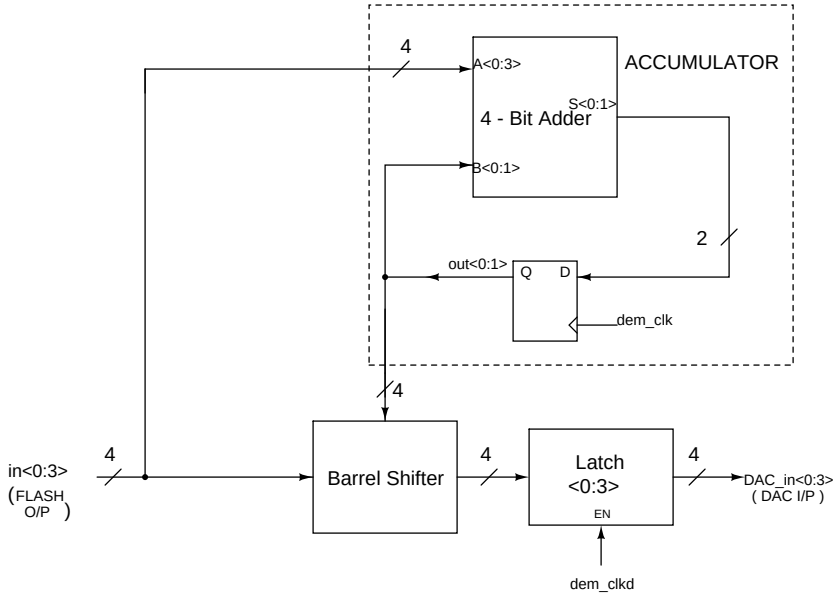


Figure 5.28: Schematic for the DWA implementation

Accumulator

The accumulator generates the control signals for turning on the basic current cells of the DAC, starting with the next available unused element. The DAC

is thermometer coded. It is basically a residual number system (RNS) adder. The RNS adder architecture is quite simple. Since it is a % 4 adder which adds four input bits from thermometer coded flash output to the present two bit state $S<0:1>$, it is implemented with 3 full adders and neglecting the output carry from final adder.

The two output bits are calculated in terms of input thermometer code $in<0:3>$ and previous output no $S<0:1>$ as:

$$out<0>=S<1>\oplus in<3>\oplus Y \tag{5.10}$$

$$\begin{aligned} out<1> = (S<0>\oplus(in<0>.in<1>+(in<0>\oplus in<1>)in<2>) \\ \oplus\,(S<1>.in<3>+(S<1>\oplus in<3>).Y)) \end{aligned} \tag{5.11}$$

Where, $Y = in<0>\oplus in<1>\oplus in<2>$

The RNS adder architecture is shown in Fig. 5.29.

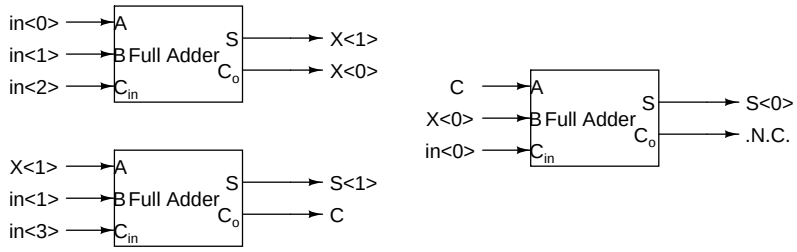


Figure 5.29: modulo 4 adder architecture

The operation of the accumulator is illustrated with the help of an example. Let the 4 basic DAC current cells be labeled CS1, CS2, CS3 and CS4.

The pointer points to the next available unused element.

D-flip flop

Fig. 5.30 shows the schematic of the used D-flip flop. This is a standard positive

Current Pointer Position	Input Data	Accumulator Output	Updated Pointer Position
CS1	0001	$0+0+0+1+000=001$	CS2
CS2	0011	$0+0+1+1+001=011$	CS4
CS4	0001	$0+0+0+1+011=100$	CS1 (4 MOD 4 =0)

Table 5.3: Working method of accumulator

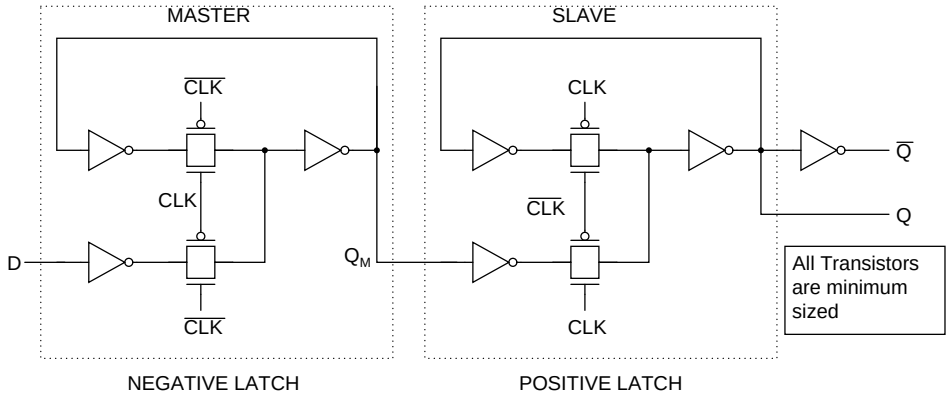


Figure 5.30: D-flip flop

edge triggered master-slave type D-flip flop.

Barrel Shifter

Fig. 5.31 shows the block diagram of the barrel shifter implemented in the design. The input to the barrel shifter is the 4-bit thermometer code generated by the internal flash ADC. The barrel shifter has two stages since maximum no of shifts necessary is 3. Each stage is built using 4 multiplexers.

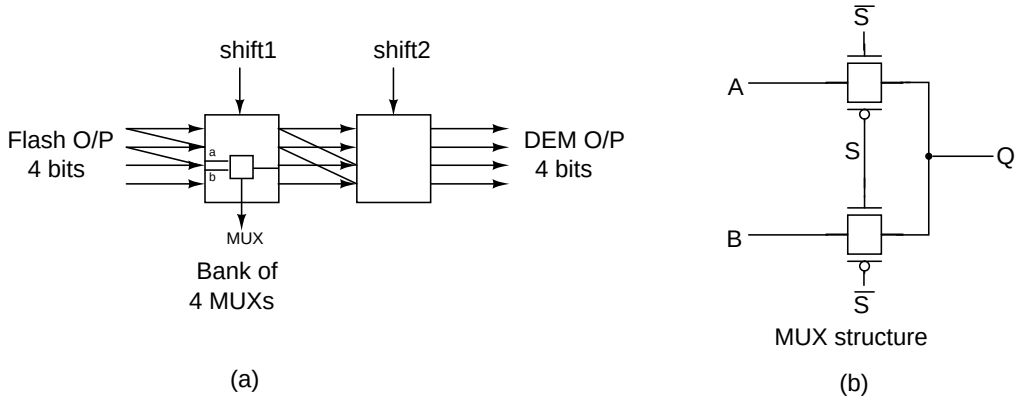


Figure 5.31: (a) Barrel Shifter and (b) Multiplexer structure

The control signals for the barrel shifter are generated by the accumulator. The i-th stage circularly rotates its 4-bit input by 2^{i-1} if its control signal is 1. Else the stage output is the same as its input.

Latch

A latch samples the output of the barrel shifter after it has settled to its final value. This way, glitches are removed. The clock to the latch is a delayed version of the clock applied to the accumulator. The outputs of the latches are used to control basic cells of the resistive DAC and feedforward DAC. Fig. 5.32 shows the schematic of the positive latch.

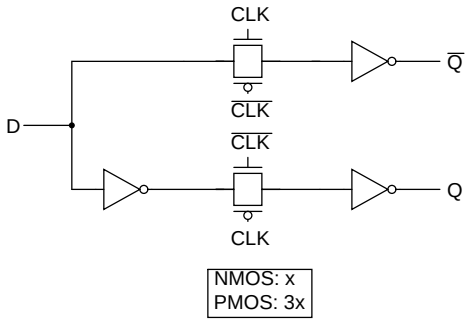


Figure 5.32: DAC latch

5.5 Reference Generator

This section discusses the design of the reference voltages and currents for the designed modulator. The different references that need to be generated are:

1. The reference voltages for the internal flash ADC. The top and bottom node of the resistive ladder are held at 1.65 V and 0.15 V respectively.

2. The reference currents for the flash ADC bias generator.

3. The biasing currents for the loop filter opamps, transconductor block and the limited swing inverter circuit. Each loop filter opamp has an input bias current of 1 μA or, 2 μA.

5.5.1 Generation of ADC References

The reference voltages for the flash ADC are generated using the arrangement shown in Fig. 5.33. The opamp shown in the Fig. 5.33 has an identical architecture to that of the first opamp of the loop filter in Ramalingam's design.

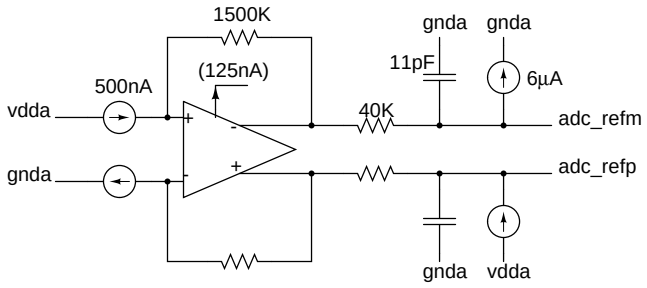
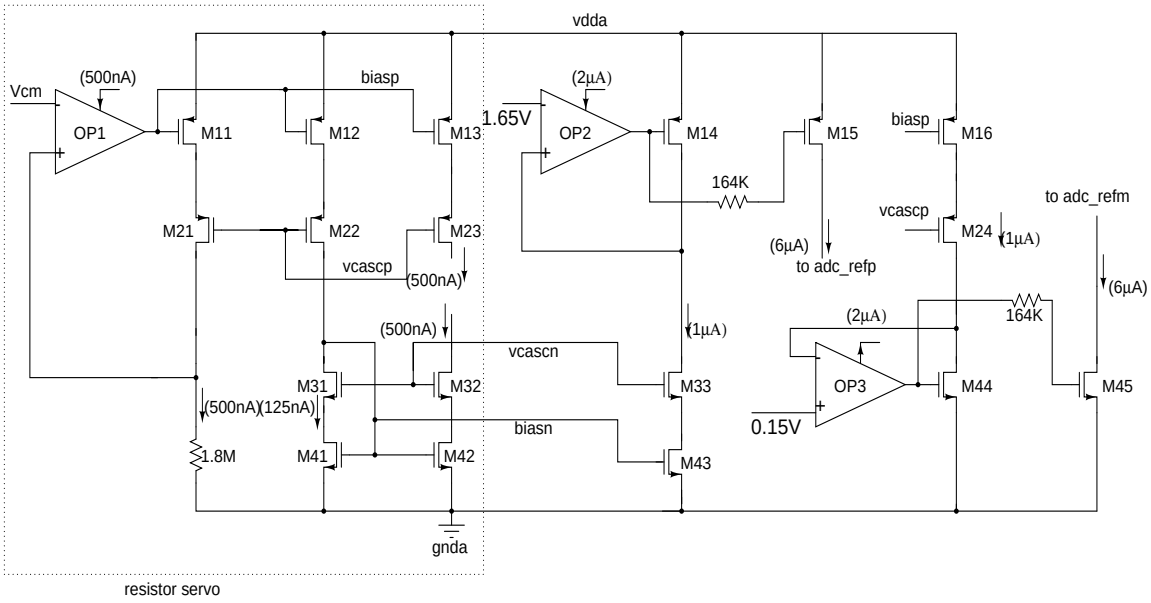


Figure 5.33: Generation of ADC references

The voltage drop across the 1.5 MΩ resistors is 0.75 V. The CMFB loop of the opamp forces its output voltages to 1.65 V and 0.15 V. A low pass filter is connected at the output of the opamp to filter out any noise present in the ADC references. Since, the flash ladder requires a current of 6 μA the opamp ideally need not supply any current. The currents used in the generation of ADC references are generated by the current generators discussed in the following section. The input current sources and the extra 6 μA current sources must be resistance dependent. Otherwise, output voltage can change drastically along 3 corners of resistance value. This is done by means of a resistor servo circuit.

5.5.2 Generation of Reference Currents

Fig. 5.34 shows the schematic that is used for generating reference currents for the various blocks of the reference generator. The inputs to the reference generator are - a bias current of 1μA and an input voltage of 0.9 V denoted as V_{cm} in Fig. 5.34. The The input bias current is mirrored to generate all the tail currents. A current of 500 nA is required for opamp OP1, which acts as a resistor servo. The negative feedback around R1 forces the voltage across the 1.8 MΩ resistor to be equal to 0.9 V. The current through M11 is mirrored to M13 via M12 and to M42 via M41. Hence, M13 is a current source of 500 nA while M42 is a current sink of 500 nA. The



M11,13 : 8(2/2)	M12 : 2(2/2)	M14 : 4(2/2)	M15 : 24(2/2)	M16 : 16(2/2)
M21,23 : 8(2/1)	M22 : 2(2/1)	M24 : 4(2/1)		
M41 : 2(0.5/1)	M42 : 8(0.5/1)	M43 : 16(0.5/1)		
M41 : 2(0.5/2)	M42 : 8(0.5/2)	M43 : 16(0.5/2)	M44 : 4(0.5/2)	M45 : 24(0.5/2)

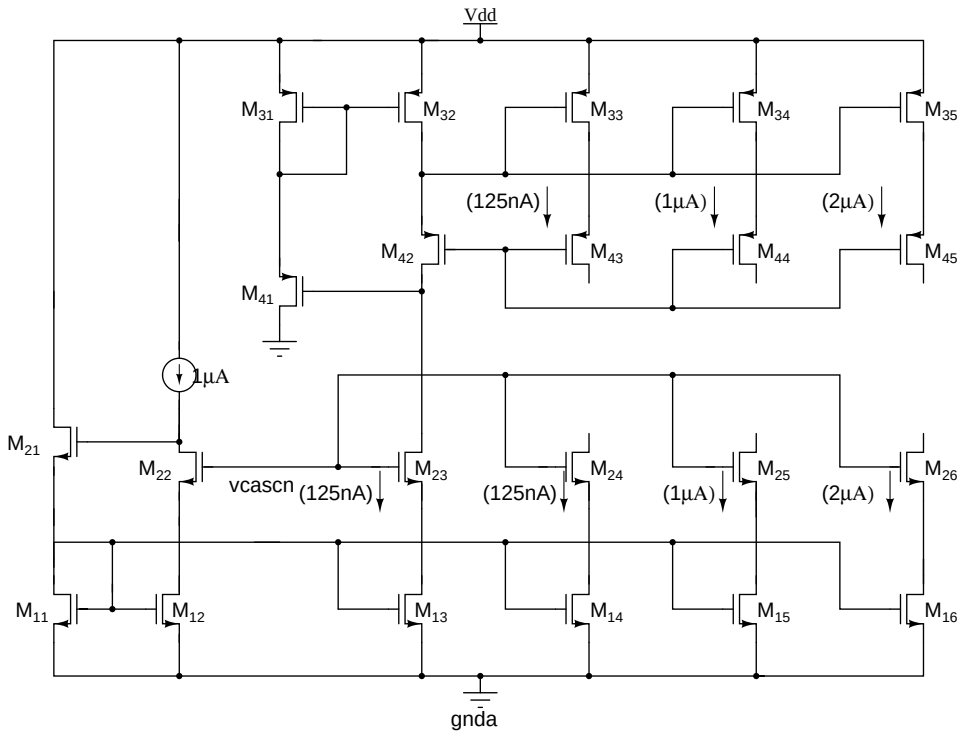
Figure 5.34: Generation of reference currents

currents through M12 and M41 can be mirrored to create more current sources and sinks respectively. This way the resistance dependant current sources are implemented.

5.5.3 Opamp Bias Currents

The loop filter opamps, the transconductor block and the limited swing inverter circuit require tail currents of value 1 μA and 2 μA. Opamp used for generating ADC and DAC references require a tail current of 125 nA. The tail current for these opamps is generated using the circuit shown in Fig. 5.35.

one external current source of 1 μA is used at input. From this several source and sink currents of 125 nA, 1 μA, 2 μA are generated using cascode current mirrors.



$M_{12,15}$ -16(0.5/2) $M_{22,25}$-16(0.5/1)	$M_{11,14}$ - 2(0.5/2) $M_{21,24}$ -2(0.5/1)	M_{16}- 32(0.5/2) M_{26}-32(0.5/1)
M_{35}-16(2/2) M_{45}-16(2/1)	$M_{31,32,33}$ -2(2/2) $M_{41,42,43}$-2(2/1)	M_{34}-32(0.5/2) M_{44}-32(0.5/1)

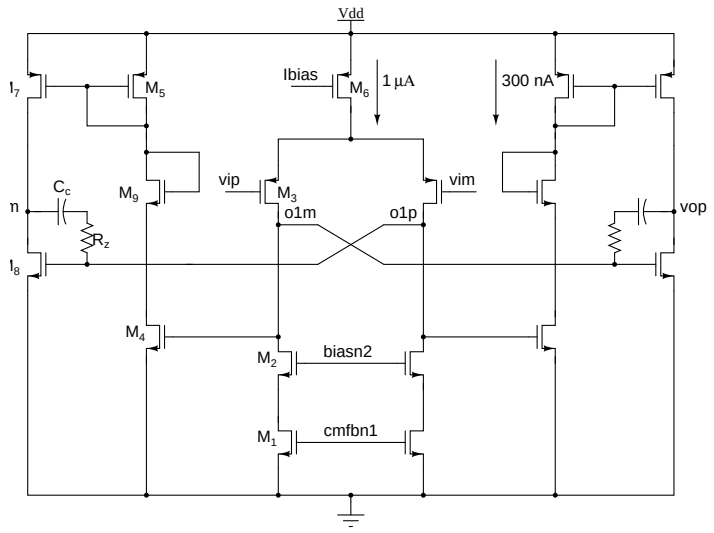
Figure 5.35: Generation of opamp bias currents

5.5.4 Reference Generator Opamp

The opamp OP2 in the reference current generation section is necessary to ensure that the drain voltage of transistor M4 is set to 1.65 V. This is because transistors M5 and M6 which source currents to the DAC and ADC respectively have their drains held at 1.65 V by the output CMFB loop of the opamp. The matching of the drain voltages is necessary to ensure exact mirroring of currents. Similarly opamp OP3 ensures that the drain voltage of M11 is equal to the drain voltage of M12 and M13 which sink currents from the DAC and ADC respectively. Without opamps OP2 and OP3 there will be large errors in the currents sourced and sinked to the ADC and the DAC.

The circuit used for reference generator opamp is taken from [7].

The circuit of the Opamp is shown in Fig. 5.36.



M_1-20(3/6)	M_5-8(1/0.25)	M_9-8(1/0.18)
M_2-12(1/1)	M_6-80(1/1)	R_z-68.0135K
M_3-5(0.5/2)	M_7-8(1/0.25)	C_c-630 fF
M_4-80(1/1)	M_8-12(0.5/0.25)	

Figure 5.36: Reference Generator Opamp

The first and second stage CMFB circuits are shown in Fig. 5.37 and Fig. 5.38

respectively.

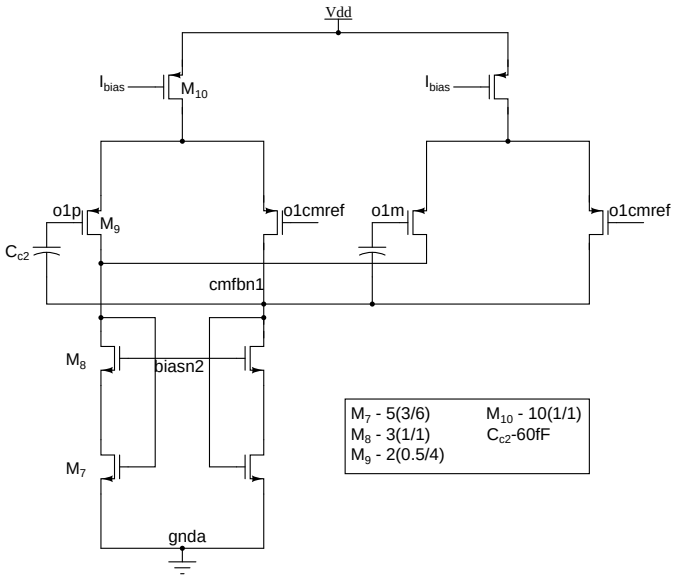


Figure 5.37: Refgen opamp first stage CMFB circuits

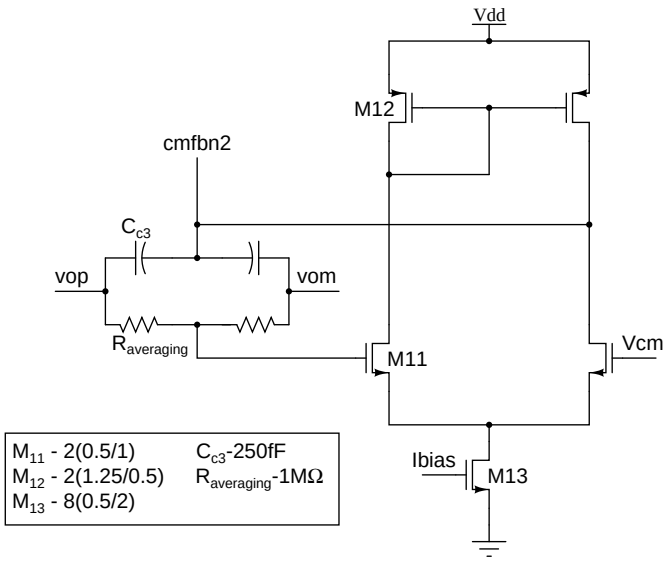


Figure 5.38: Refgen opamp second stage CMFB

CHAPTER 6

Tuning of time constant of integrators

6.1 Motivation

The on chip resistors and capacitors vary across the process corners. As observed from UMC180 technology file, on chip resistance can vary from -32.37 % and 38.5 % on chip capacitance can vary by ±15%. This variation in R and C causes change in $\Delta\Sigma$ modulator performance. If RC time constant goes down, the poles of the NTF moves to higher frequency causing increase in the out of band gain (OBG). The in band noise reduces, this may sound promising at first but this in turn may lead to the instability of the modulator. On the other hand increase in time constant causes increase in in-band quantization noise, thereby reducing the SNR. Therefore, some kind of tuning method is necessary to maintain the value of RC within certain tolerance limit.

6.2 Introduction of Capacitor Banks

With the intention to keep RC value constant across process corners, the capacitors in the circuit are replaced by capacitor banks. This is shown in Fig. 6.1.

In Fig. 6.1 the nMOS switches are kept at integrator input and capacitors are connected towards integrator output. In this way, the signal swing across the switches is small. Hence, they introduce less distortion. The pMOS switches are used to discharge the bank capacitors when they are disconnected from the loop.

As suggested from [11] and [12],

$C_{ARRAY} = C_{min} + n.\delta C,\ n = 0, 1, ..., 2^N - 1$, where N is the no. of bits.

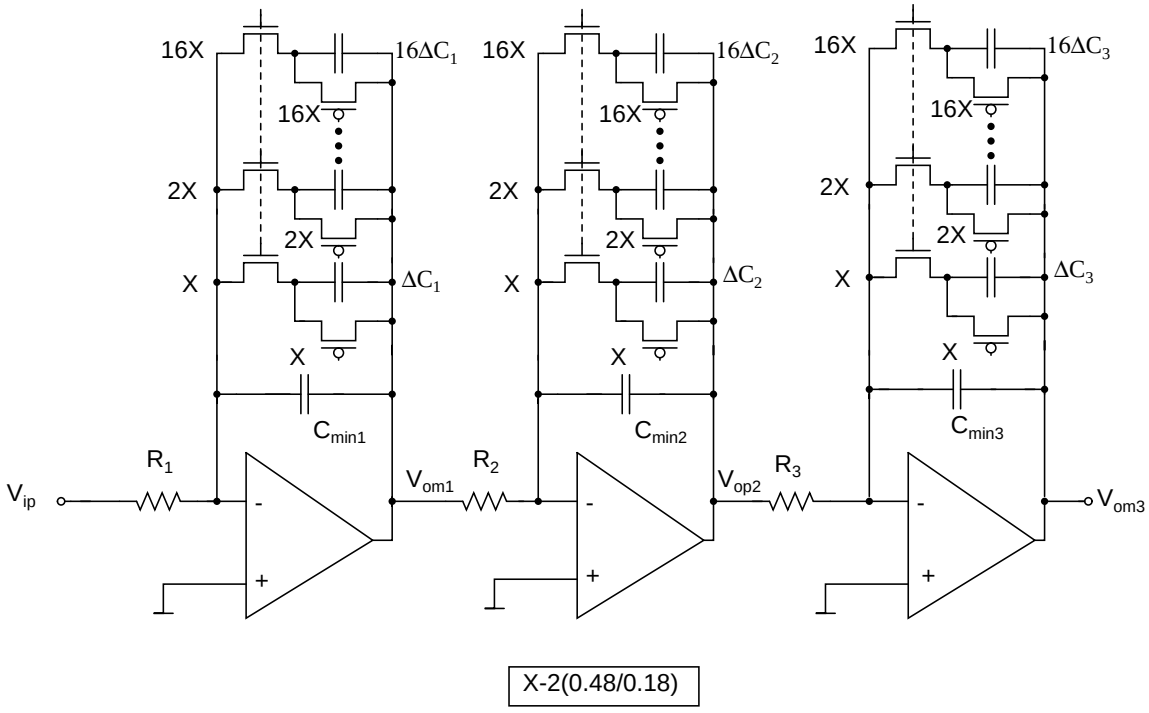


Figure 6.1: Integrators with capacitor banks

Suppose in a process corner R and C change by a factor α_R and α_C respectively. For the nominal RC to be equal to new RC value,

$$R_{corner}C_{corner} = R_{nominal}C_{nominal} \tag{6.1}$$

$$or, \alpha_R.R_{nominal}C_{corner} = R_{nominal}C_{nominal} \tag{6.2}$$

$$or, C_{corner} = \frac{C_{nominal}}{\alpha_R} \tag{6.3}$$

Now, to achieve a capacitance C_{corner} along a particular corner, we have to use a capacitor $C_{required}$.

$$C_{corner} = \alpha_C.C_{required} \tag{6.4}$$

$$or, C_{required} = \frac{C_{nominal}}{\alpha_R.\alpha_C} \tag{6.5}$$

Evidently, $C_{required}$ will be minimum at 'res-max','cap-max' corner and minimum at 'res-min', 'cap-min' corner. Therefore the cap bank is implemented in following way:

$$or, C_{fixed} = C_{min} \tag{6.6}$$

This corresponds to when all the switches are off.

For N bit tuning (N is taken as 5),

$$(2^N - 1)\Delta C = C_{max} - C_{min} \tag{6.7}$$

This gives the value of minimum capacitance in the binary weighted cap bank.

at 'min-min' corner, all the switches should be on.

The code to be applied in the cap bank is given by,

$$n = \frac{C_{nominal} - C_{min}}{\Delta C} \tag{6.8}$$

Nominal code should be equal to or the integer just exceeding n.

Cap	$C_{nominal}$	C_{min}	ΔC
C_1	5.208325 pF	3.678 pF	210.1636 fF
C_2	488.2813 fF	305.1 fF	17.4358 fF
C_3	976.53 fF	613.1 fF	35.0273 fF

Table 6.1: Value of cap bank components

Nominally a cap value $C_i = C_{min,i} + nominalcode \times \Delta C_i$ is kept.

6.3 Usage of Common Mode Voltage for RC Estimation

The implemented modulator is fully differential in nature. All the input signals are processed differentially. So, the common mode does not carry any information. Therefore, the common mode voltage can be utilized for estimating the time

constants. The basic idea is to inject a common mode square wave current with amplitude ±I to the virtual ground of any integrator opamp. For a sufficiently fast square wave input, the peak to peak output voltage across integrating capacitor will be approximately a triangular wave. The peak to peak voltage across the capacitor is a decreasing function of both R and C of the integrator. If C is replaced by a capacitor bank, this circuit basically acts like a DAC in disguise. Since, the peak to peak output voltage is dependent on the effective capacitance, which in turn depends on the code word used in the capacitor bank. By comparing this DAC voltage with a pre-generated reference voltage, which corresponds to voltage for nominal RC values, the RC value can be tuned back to original one even in presence of process variations.

The common mode equivalent small signal circuit is shown in Fig. 6.2.

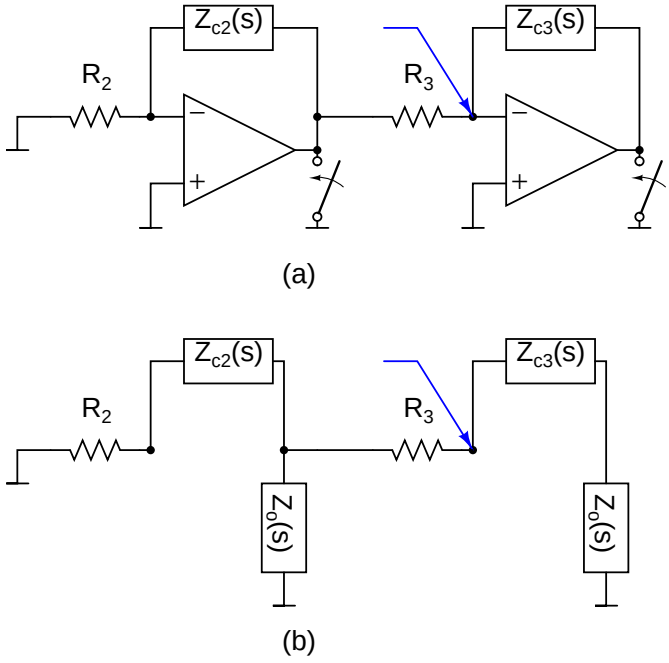


Figure 6.2: (a) Common mode circuit and (b) Small signal equivalent

The common mode gain of opamp is $\leq 20\,\mathrm{dB}$ at all frequencies. Hence they are neglected from the small signal model.

6.3.1 Modeling of Common Mode Response

The equivalent impedance of cap bank is given by,

$$Z_c(s) = \frac{1}{sC_{min} + \frac{sd0}{R+\frac{1}{s.\Delta C}} + \frac{sd1}{\frac{R}{2}+\frac{1}{s.2\Delta C}} + \frac{sd2}{\frac{R}{4}+\frac{1}{s.4\Delta C}} + \frac{sd3}{\frac{R}{8}+\frac{1}{s.8\Delta C}} + \frac{sd4}{\frac{R}{16}+\frac{1}{s.16\Delta C}}} \tag{6.9}$$

It is evident from Fig. 6.3.

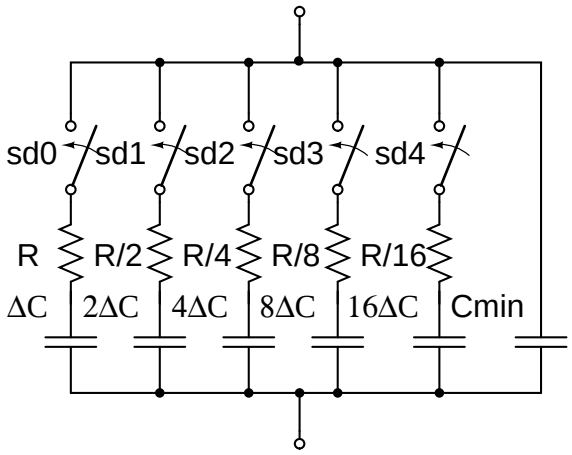


Figure 6.3: Capacitor bank equivalent circuit

The common mode output impedance of opamp has one inductive component. Outputs of opamps are connected to V_{cm} via transmission gates in tuning mode. During tuning mode the $\Delta\Sigma$ ADC is not functional. The nature of the effective output impedance shows that it can be modeled by an equivalent parallel RLC circuit.

From the graph in Fig. 6.4,

$Q = 0.0321$ and $f_c = 10\,\text{MHz}$

Therefore equivalent parallel RLC circuit has -

$R_P = 9.387\,\text{k}\Omega$

$C_P = 54.4296\,\text{fF}$

$L_P = 4.6538\,\text{mH}$

For an input step of unity amplitude the output voltage across capacitor bank

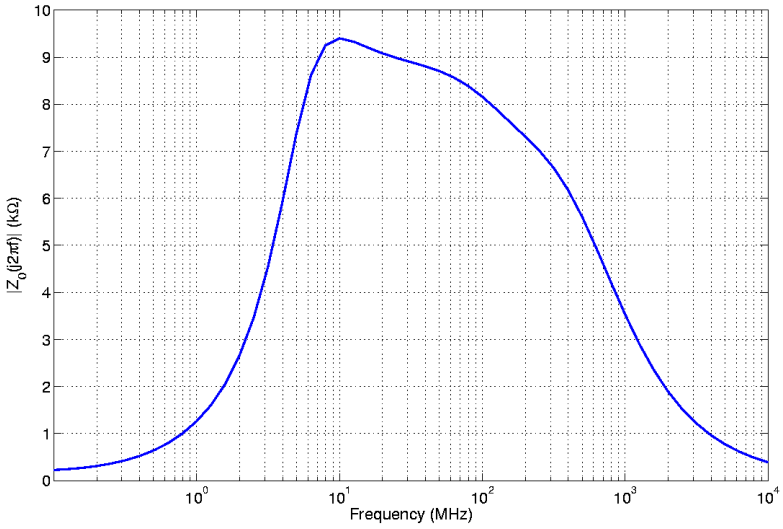


Figure 6.4: Output impedance

3 is given by,

$$\frac{R_3 + (Z_{o2} \| (Z_{c2} + R_2))}{Z_{c3} + Z_o + R_3 + (Z_{o2} \| (Z_{c2} + R_2))} \tag{6.10}$$

The input pulse train can be approximated by a sum of steps like:

$$I.u(t) - 2I.u(t - \tfrac{T_c}{2}) + 2I.u(t - \tfrac{2.T_c}{2}) + 2I.u(t - \tfrac{3.T_c}{2}) + ... + (-1)^n.2I.u(t - \tfrac{n.T_c}{2}).$$

All the transfer functions are modeled in Matlab. The output waveforms are shown in the Fig. 6.5.

Origin of Inductive Component in Opamp

The common mode equivalent small signal model of the feedforward opamp used in chapter 4 is shown in the Fig. 6.7.

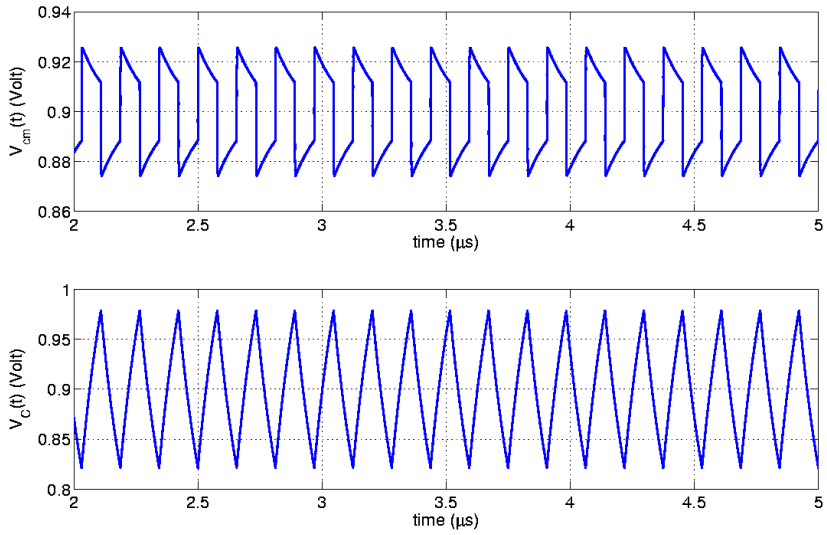


Figure 6.5: Matlab model output of common mode variation of (a) output node of opamp (b) across third integrator capacitance

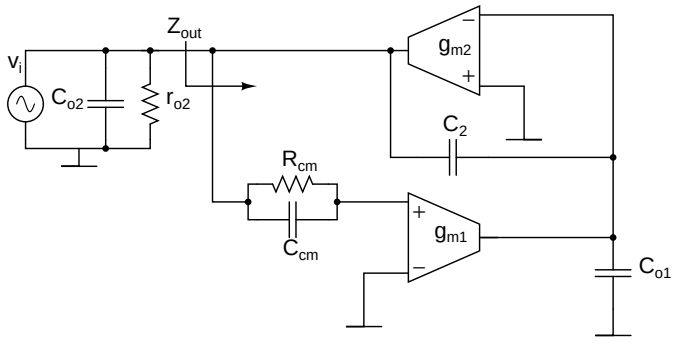


Figure 6.6: Common mode small signal equivalent circuit

$$i = v.\frac{g_{m1}g_{m2}}{sC_{o1}} + s.C_2.v.(1 - \frac{g_{m1}}{s_{co1}}) \tag{6.11}$$

$$or, \frac{i}{v} = Y_{out} \tag{6.12}$$

$$= \frac{g_{m1}g_{m2}}{sC_{o1}} + \frac{C_2}{C_{o1}} \tag{6.13}$$

$$= \frac{1}{s.Leq} + G_{eq} \tag{6.14}$$

(assuming $g_{m1} \ll 1$)

Therefore, the impedance has an inductive component.

6.3.2 Successive Approximation Algorithm

Successive approximation is a type of analog-to-digital conversion that finds out the discrete digital representation via a binary search through all possible quantization levels before finally converging upon a digital output. The conversion time is constant and proportional to the number of bits in the output.

The SAR logic operates by successively dividing the voltage range by half as explained in the following steps:

1. The counter is set to '0'.

2. The MSB is set to '1' and digital equivalent is compared to unknown analog input voltage.

3. If analog input voltage is higher than the digital equivalent, the MSB is retained as '1' and 2nd MSB is set to '1'. Otherwise, the MSB is set to '0' and 2nd MSB is set to '1'.

4. The above process is repeated down to LSB and by this time converted digital value is available in SAR.

6.3.3 Tuning Algorithm Implementation in Matlab

With the previously mentioned model of RC estimator, the tuning algorithm is implemented in Matlab. The SNR obtained by the Matlab model shows variation less than 1%.

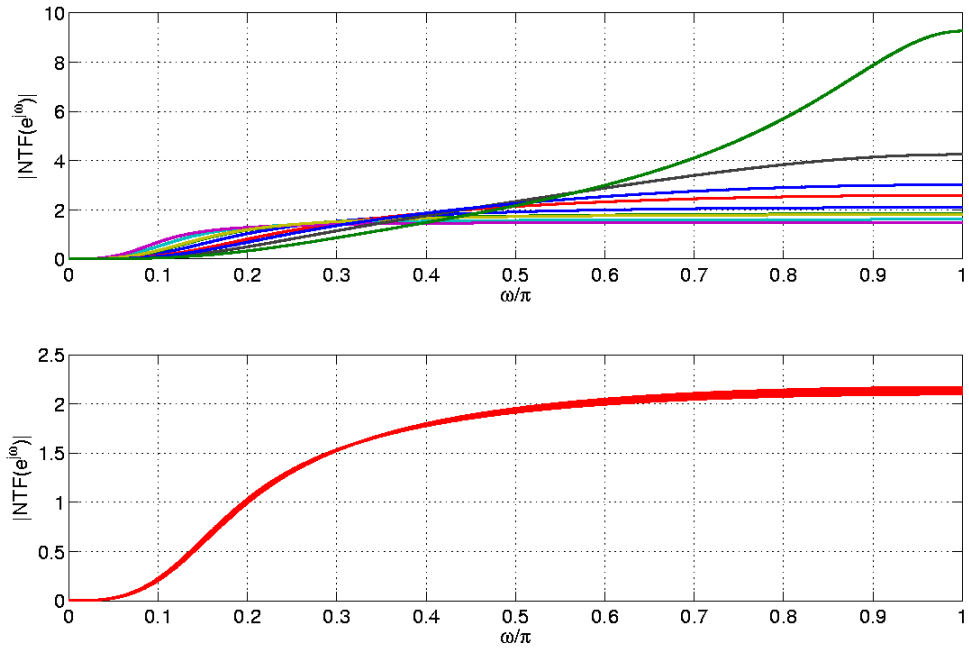


Figure 6.7: (a) NTF with resistance and capacitance variation (b) NTF after capacitor bank tuning

6.4 Single Bit RC Estimation Circuit

The basic circuit comprises of the following parts:

1. Common mode current injector.
2. Parallel RC circuit.
3. Track and Hold (T & H) peak and valley detector.
4. Switched capacitor subtractor.
5. Reference generator.
6. Comparator.
7. Successive Approximation Register (SAR) logic circuit.

8. Clock generator.

6.4.1 Common Mode Current Injector

A common mode square wave current with a time period 6.4 MHz is injected at the virtual ground of third integrator opamp. The square wave current is generated by means of a resistor servo (Fig. 6.8).

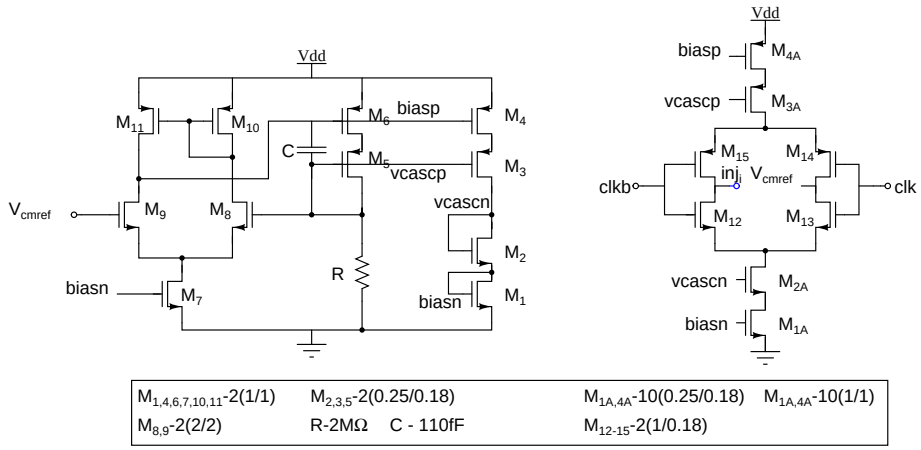


Figure 6.8: Common mode current injector

6.4.2 Parallel RC Circuit

Third integrator opamp is used to measure the value of time constant (RC). A common mode square wave current is injected at the third integrator opamp's virtual ground. By restructuring Fig. 6.2 the equivalent circuit obtained is as shown in Fig. 6.9.

Here Z_0 is the output impedance of the opamp and transmission gate in parallel. The output voltage is taken as potential difference across two terminals of the capacitor. To avoid the fluctuation of opamp output common mode being taken into account, the voltage is measured across two terminals of the capacitor bank. If Z_0 is sufficiently small, the output voltage across capacitor gives a reasonable estimate of time constant.

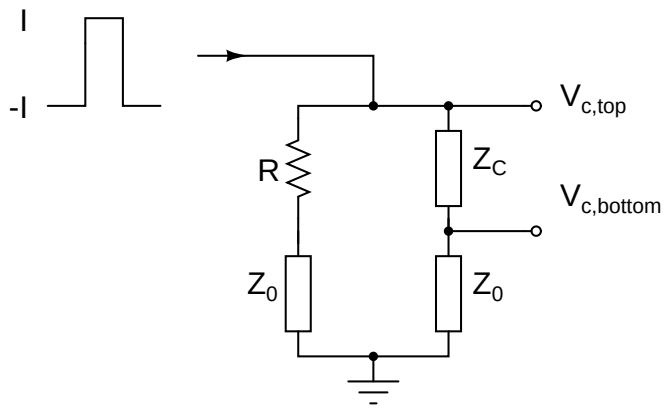


Figure 6.9: RC block

6.4.3 Track and Hold Peak and Valley Detector

Two T&H circuits are operated by complementary clock signals to detect the maximum and minimum value of the common mode signal respectively. The basic T&H circuitry is as shown in figure 6.10.

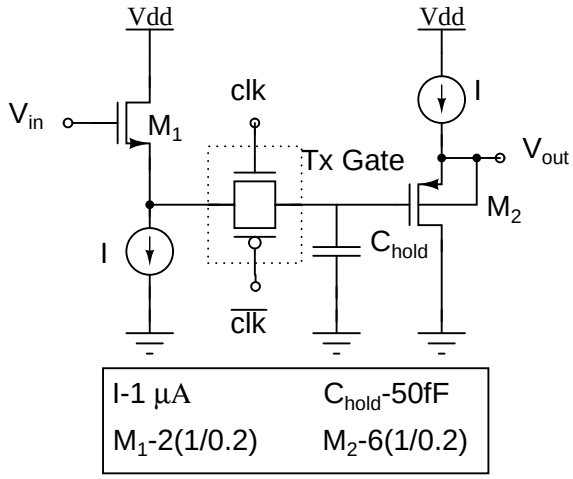


Figure 6.10: Track & Hold Circuit

The T&H outputs are shown in Fig. 6.11.

The outputs of first set of T&H circuits are delayed from each other by half clock cycle (maximum and minimum value of a triangular waveform occurs by half clock cycle delay) as shown in Fig. 6.11. To mitigate this problem, another set of T&H is used in cascade, operated by complementary set of clocks to bring back the sample in same time interval.

The architecture is shown in the figure 6.12.

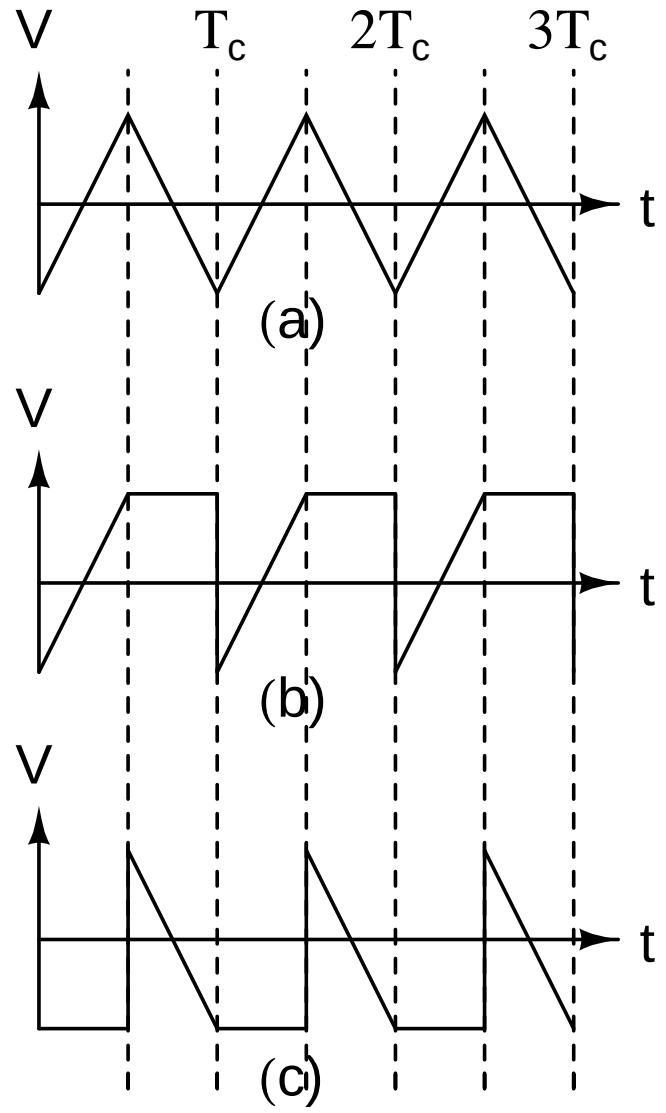


Figure 6.11: (a) Voltage across capacitor, (b) Output of T&H detecting maximum voltage, (c) Output of T&H detecting minimum voltage

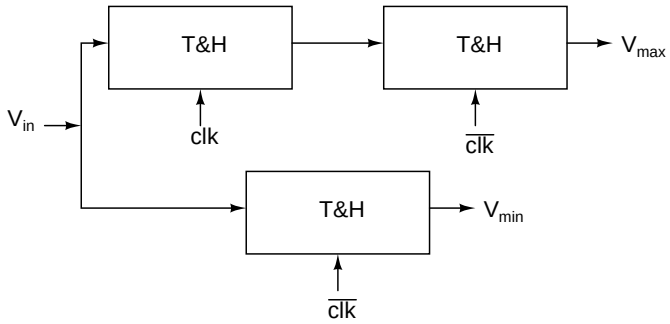


Figure 6.12: Peak and valley detector structure

6.4.4 Switched Capacitor Subtractor

Since, we are using common mode response of a fully differential circuit, the common mode peak to peak variation across the two integrating capacitors in third integrator are same. Hence, while measuring the voltage across the capacitor, to avoid asymmetry both of the third integrator opamp virtual grounds are loaded by same amount. This is achieved by employing two T&H-s to detect the maximum voltage across one capacitor and two T&H-s to detect the minimum voltage across the other capacitor. The voltage to be measured is

$$V_{meas} = (V_{C31,top} - V_{C31,bottom}) - z^{-\frac{1}{2}}(V_{C32,top} - V_{C32,bottom}) \tag{6.15}$$

Here, $C31$ and $C32$ implies the third integrator capacitors in the fully differential circuit. It is shown in Fig. 6.13.

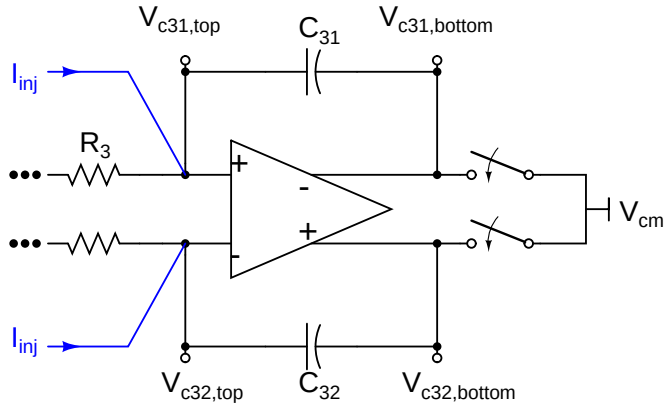


Figure 6.13: Voltages to be measured in fully differential structure of third integrator

After the second set of T&H circuitry are used, $V_{C31,top}$, $V_{C31,bottom}$, $V_{C32,top}$, $V_{C32,bottom}$ are available during same clock cycle. Fig. 6.14 shows the schematic of a simple switched capacitor subtractor that implements

$2\{(V_{C31,top} - V_{C31,bottom}) - (V_{C32,top} - V_{C32,bottom})\}$.

No separate gain stage is used. The subtractor itself introduces a gain of 2. A telescopic cascode having $2\,\mu$A at each branch, a dc gain of 50 dB and UGF 700 MHz is used in the subtractor.

The pamp in the switched capacitor subtractor is implemented by a telescopic

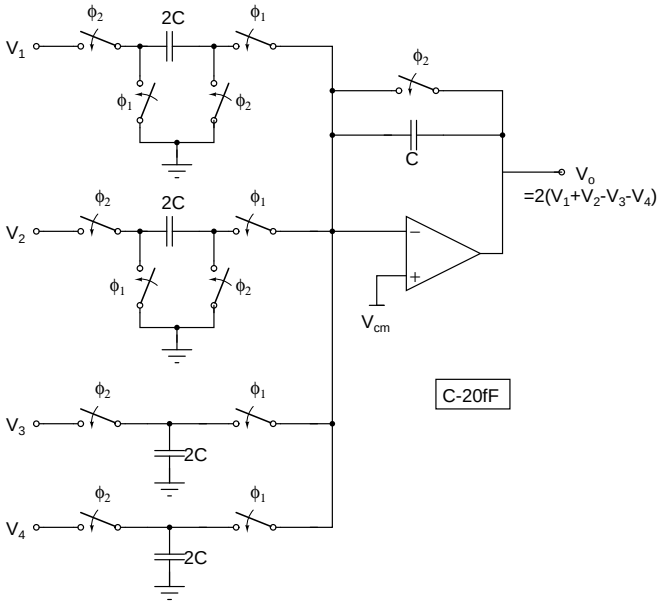
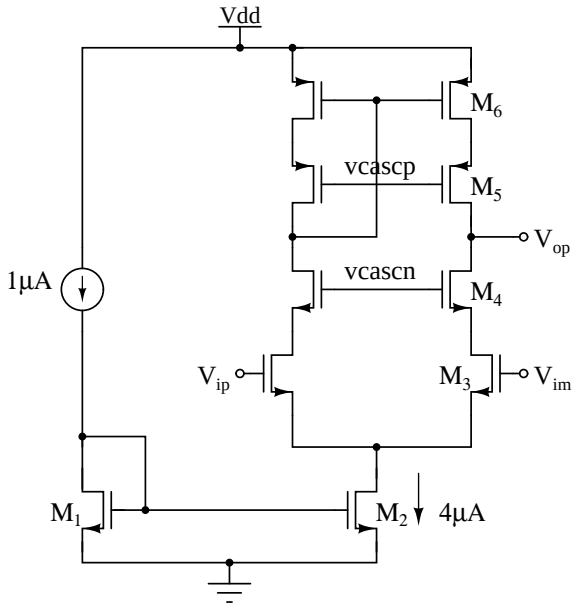


Figure 6.14: Switched Capacitor Subtractor

cascode used is shown in Fig. 6.15.



M_1–2(0.5/1)	M_3–2(0.5/0.5)
M_2–8(0.5/1)	$M_{4,5,6}$–2(0.5/0.3)

Figure 6.15: Telescopic cascode opamp

6.4.5 Reference Generator

The T&H gain and output quiescent voltage are process dependent. The opamp in the subtractor also generates a systematic offset which is also process dependent. To overcome this problem, the reference voltage is passed through a reference pre-distortion circuit, which introduces same type of offset and nonlinearities. To incorporate the effect of subtractor offset also, we assume the reference voltage to be available in differential form $V_{cm} \pm V_{ref}$. After passing through replica T&H-s the two reference voltage are subtracted through a replica subtractor to generate final reference voltage, which takes systematic offset and process variation in account. Along 'ss' to 'ff' corner the reference tracks the peak to peak detector output voltage for a fixed RC, within an accuracy of 1.8 mV. The strategy is shown in Fig. 6.16.

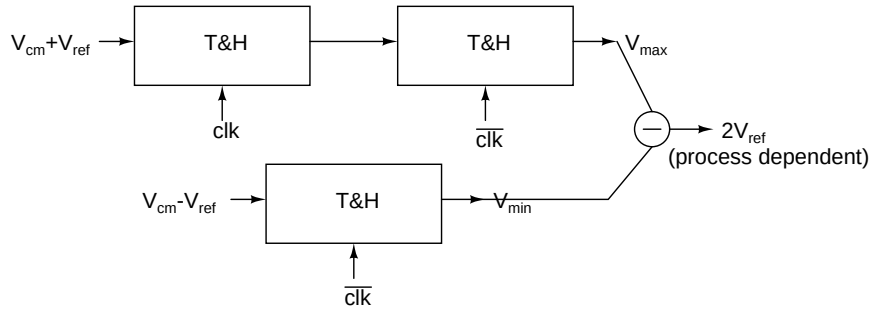


Figure 6.16: Reference pre-distortion circuit

6.4.6 Comparator

A standard comparator with in built amplifying stage is used [13; 14]. This circuit has a very low systematic offset voltage(< 1 mV). The comparator circuit is shown in Fig. 6.17.

Preamplifier Circuit

The single stage differential amplifier in Fig. 6.18 is used as preamplifier of comparator to reduce offset.

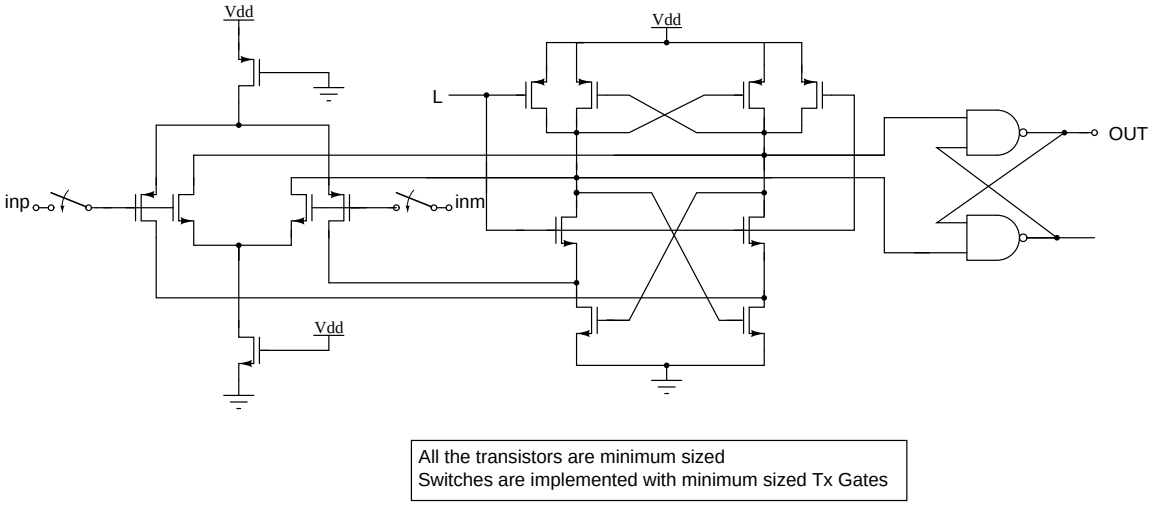


Figure 6.17: comparator circuit

Offset Calculation

The random offset introduced by preamp itself is obtained by the following formula:

$$\sigma^2_{\text{preamp}} = \sigma^2_{\text{M}_1} + \frac{\text{g}_{\text{M5}}}{\text{g}_{\text{M1}}}^2 . \sigma^2_{\text{M}_5} \tag{6.16}$$

$$\text{Where, } \sigma^2_{\text{M}_\text{i}} = \frac{\text{A}^2_{\text{VT}}}{\text{WL}} + \text{C}_0 \tag{6.17}$$

$A_{VT} = 4.787\,\text{mV}\mu$, $C_0 = 0.5827\,\mu\text{V}^2$

$g_{M1} = 36.7\,\mu\text{S}$, $g_{M5} = 28.43\,\mu\text{S}$.

i.e. $\sigma_{\text{preamp}} = 5.06\,\text{mV}$.

To reduce offset of the preamplifier the configuration as shown in Fig. 6.19 is used. The circuit has two modes. During 'Auto Zero' (AZ) mode the preamplifier offset is stored across the input capacitors. During '$\overline{\text{AZ}}$' mode the input voltages reach the input of preamplifier via the capacitors. The offset of preamplifier is removed by this method.

Switches are implemented with minimum sized transmission gates.

With this configuration, a small increasing ramp voltage was applied at the positive

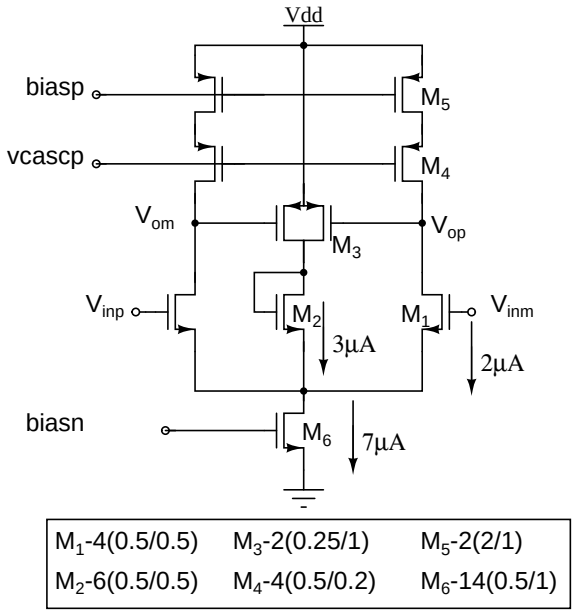


Figure 6.18: Preamplifier circuit

input and the position of comparator switching was observed. This experiment was repeated for an explicit $\pm 5.06\,\mathrm{mV}$ offset voltage. It was observed that for input voltage difference more than $500\,\mu\mathrm{V}$, in all cases the comparator changed its output state.

Offset (mV)	input voltage difference to cause transition (μ V)
0	279
-5	47.44
5	498

Table 6.2: Offset correction by auto-zeroing

6.4.7 SAR Logic Circuit

The SAR logic circuit implements the SAR algorithm described earlier. The basic block diagram of SAR logic circuit is shown in Fig. 6.20. Here, the DAC block is the parallel RC circuit with capacitor bank, driven by a square wave current of amplitude $\pm$I. The DAC output for a particular input code is compared with the reference value and the next code is generated accordingly following the SAR algorithm.

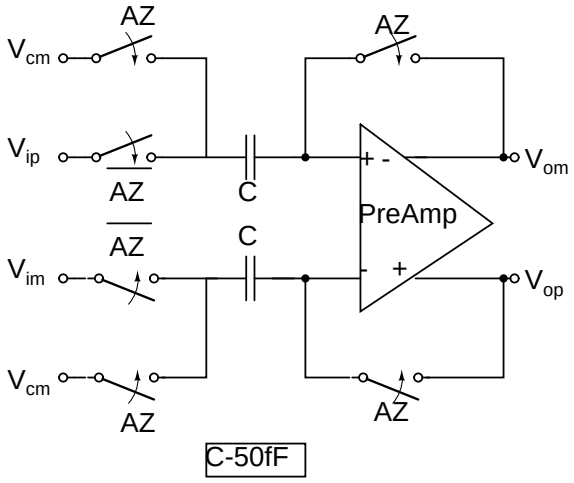


Figure 6.19: Offset correction by auto zeroing

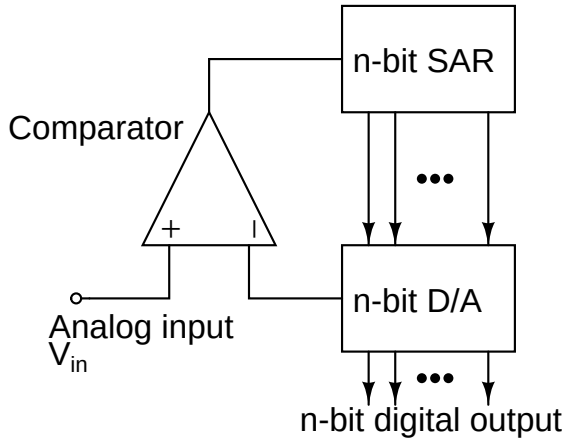


Figure 6.20: SAR logic circuit

The SAR controller block is implemented by 'verilog' and synthesized using 'Synopsys'.

6.4.8 Clock Generator Circuit

We have output of two switched capacitor subtractors which have to be compared. From transient analysis of output, following observations were made:

1. Outputs are available at same clock cycle.
2. Each subtractor outputs take some time to settle to the final value.
3. Towards end of the clock there is some switching glitch

Therefore, the comparator clock should be enabled within the subtractor clock

such that it goes ‘high’ after subtractor clock goes ‘high’ and fall to‘low’ value before subtractor clock goes ‘low’, as shown in Fig. 6.21.

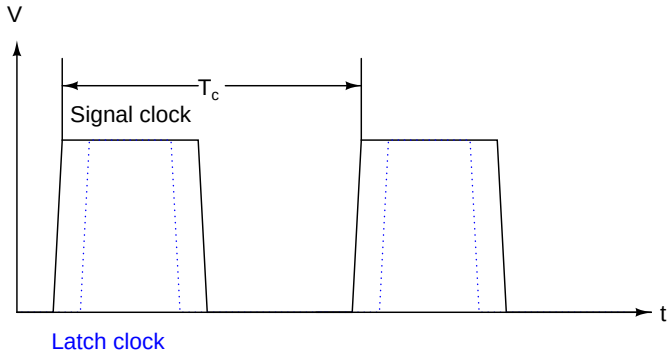


Figure 6.21: Clock generator output

The clock generator was implemented by means of slow inverters and non overlapping clock generator.

CHAPTER 7

Layout, Simulation Results and Conclusions

7.1 Layout

The designed third order CT $\Delta\Sigma$ modulator was laid out in CADENCE. Layout of the design is shown in Fig. 7.1. It occupies an area of $0.7\,\mathrm{mm}^2$.

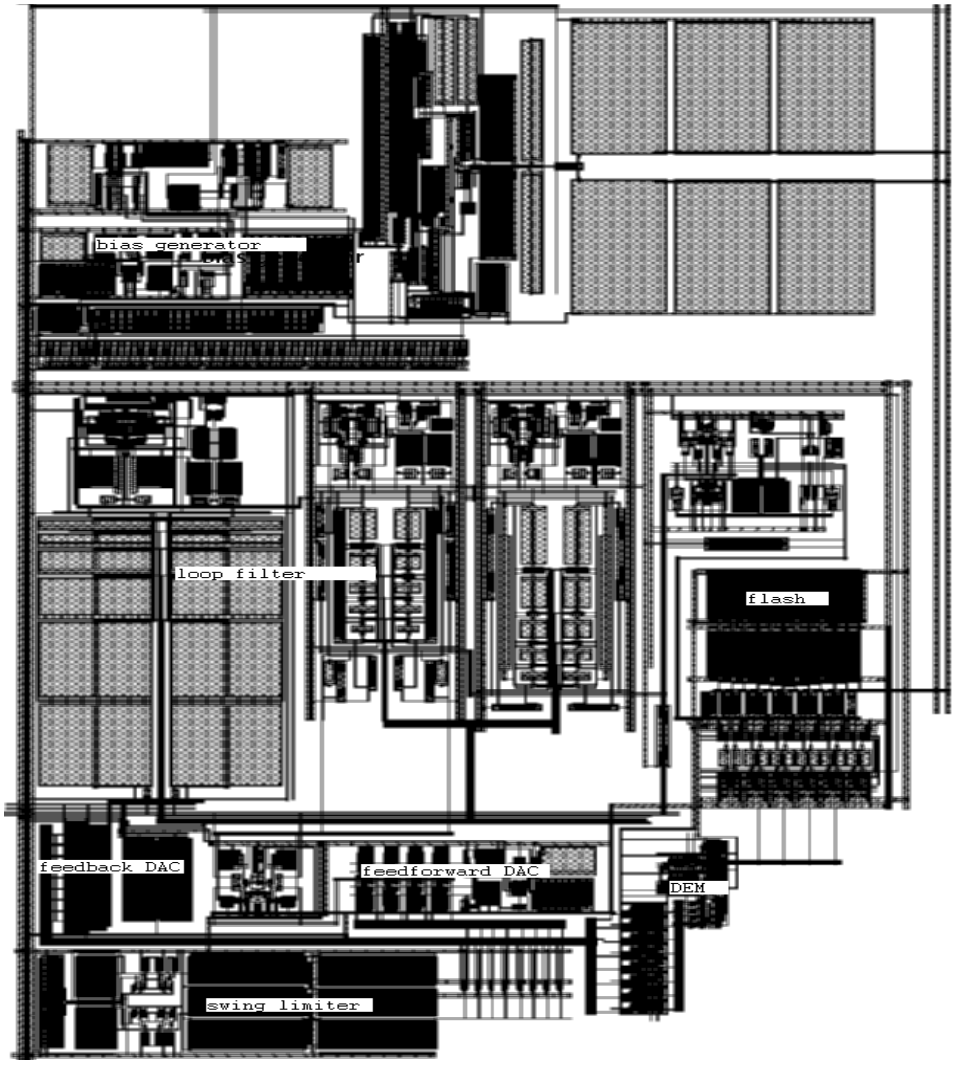


Figure 7.1: Chip layout

7.2 Simulation Results

Each of the building blocks have an associated verilog-A view or an ideal view where, the functionality of the block is realized using ideal elements. Thus while checking any block's performance, other blocks can be realized using ideal or verilog-A module. This reduces the simulation time.

The results of the various simulations run on the design is tabulated below. The input signal to the modulator is a 2.2 $V_{pp,diff}$ sinusoid at a frequency of 43.75 kHz.

Loop filter	**Flash ADC**	**DEM**	**Feedback** DAC	SNDR **(dB)**
Ideal	Ideal	VerilogA	Ideal	107
Ideal	Schematic	Schematic	Schematic	107
Schematic	Ideal	VerilogA	Ideal	105
Extracted	Ideal	VerilogA	Ideal	100
Schematic	Extracted	Extracted	Extracted	101

Table 7.1: Simulation Results

The SNR in each of the above simulation setups was found to be in excess of 90 dB. The designed ADC hence, has a resolution of 15-bits. The output PSD of the modulator when extracted views are used for loop filter and ideal views for flash, DEM, bias and reference generator for which ideal view is used is shown in Fig. 7.2.

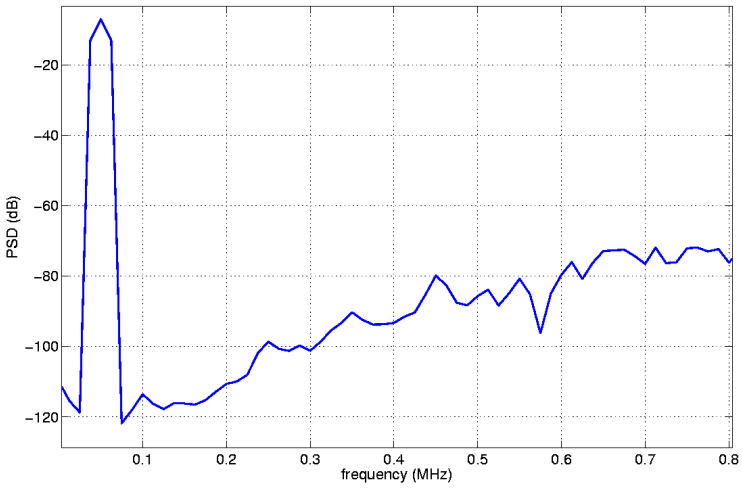


Figure 7.2: PSD of modulator output after layout

The achieved specifications of the ADC are tabulated below:

Feature	Achieved Specification
Resolution	15-bits
SNR	100 dB
Sampling rate	25.6 MHz
Signal bandwidth	200 kHz
Static power dissipation	550 μW

Table 7.2: Achieved ADC specifications

7.3 Conclusions

A third order 15 bit resolution CT $\Delta\Sigma$ modulator with 200 kHz has been designed. Feed forward architecture is used for the loop filter to reduce the power consumption. Moreover, the flash ADC consumes almost zero static power. The integrating capacitors of the loop filter can be tuned both internally and externally to make the modulator work across all process corners and temperature variations. The DWA algorithm has been implemented in the design of the feedback DAC which reduces the matching requirements across the various DAC levels and provides first-order noise shaping of the DAC mismatch.

7.4 Future Work

Certain improvements can be done in this design. Firstly, the total power consumed by the modulator can be reduced by minimizing the power consumed by the analog loop filter and feedforward DAC. Secondly, on chip tuning of resistors can be implemented that will further compensate the change in NTF due to process variation.

REFERENCES

[1] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters.* John Wiley & Sons, Inc , Hoboken, New Jersey, 2005.

[2] F. M. Gardner, "A transformation for digital simulation of analog filters," in *IEEE Trans. on Communications*, July 1986, pp. 676–680.

[3] R. Gregorian and G. C. Temes, *Analog MOS Integrated Circuits for Signal Processing.* John Wiley & Sons, Inc , Hoboken, New York, 1986.

[4] J. A. Cherry, "Theory, Practice, and Fundamental Performance Limits of High-Speed Data Conversion Using Continuous-Time Delta-Sigma Modulators," Ph.D. dissertation, Carleton University, Canada, November 1998.

[5] S. Pavan, "Excess Loop Delay Compensation in Continuous-Time Delta-Sigma Modulators," in *IEEE Transaction on Circuits and Systems*, November 2008.

[6] S. R. Norsworthy, R. Schreier, and E. G. C. Temes, *Delta-Sigma Data Converters: Theory, Design, and Simulation.* New York: IEEE Press, 1997.

[7] R. Pandarinathan, "Design of a 16-bit Continuous Time Delta-Sigma Modulator for Digital Audio," Master's thesis, IIT Madras, Chennai, June 2006.

[8] S. Pavan, N. Krishnapura, R. Pandarinathan, and P. Sankar, "A Power Optimized Continuous-Time Delta- Sigma ADC for Audio Applications," in *IEEE Journal of Solid State Circuits*, February 2008.

[9] S. Pavan and P. Sankar, "A 100 μW Single Bit Audio Continuous-time Delta-Sigma modulator with 92.5 dB dynamic range," in *Proceedings of European Solid State Circuits Conference*, September 2009.

[10] R. T. Baird and T. S. Fiez, "Linearity enhancement of multibit $\Delta\Sigma$ A/D and D/A converters using Data Weighted Averaging," in *IEEE Trans. on Circuits and Systems-II*, December 1995, pp. 753–762.

[11] A. M. Durham, W. Redman-White, and J. Hughes, "High-linearity continuous-time filter in 5-V VLSI CMOS," in *IEEE JSSC*, September 1992, pp. 1270–1276.

[12] J. Lim, Y. Cho, K. Jung, J. Park, J. Choi, and J. Kim, "A Wide-Band Active RC Filter with a Fast Tuning Scheme for Wireless Communication Receivers," in *IEEE Custom Integrated Circuits Conference*, 2005.

[13] R. J. Baker, *CMOS: Circuit Design, Layout and Simulation*, 2nd ed. Wiley Interscience, IEEE Press , Piscataway, NJ, 2007.

[14] R. J. Baker, *CMOS: Mixed Signal Circuit Design*, 1st ed. Wiley Interscience, IEEE Press , Piscataway, NJ, 2003.