Design of a Low Power Class-D Amplifier for Hearing Aids

A THESIS

submitted by

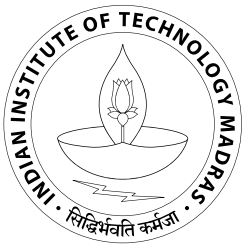
AMRITH SUKUMARAN

for the award of the degree

of

MASTER OF SCIENCE

(by Research)



Department Of Electrical Engineering

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CERTIFICATE

This is to certify that the thesis titled **Design of a Low Power Class-D Amplifier for Hearing Aids**, submitted by **Amrith Sukumaran**, to the Indian Institute of Technology Madras, for the award of the degree of **Master of Science**, is a bonafide record of the work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

Ipods, mobile phones, computers and scores of modern gadgets store data digitally. Here, core analog information such as video and audio are encoded in digital bits. Personal assistant devices such as hearing aids is another example where the analog audio is encoded digitally. Encoding audio digitally makes signal processing and conditioning easy. There are a number of powerful Digital Signal Processors(DSP) available in the market that can process digital signals accurately and reliably . This digitally processed data must then be converted back into analog sound waves for human reception. This work deals with the design of the digital to analog converter for a digital hearing aid.

The primary difficulty in converting high resolution(sixteen bits and greater) digital signals into analog is in maintaining the quality of the signal. The converter must not distort the signal and must not add it's own noise. The most important requirement for all portable and body worn devices is battery life. Therefore, the digital to analog converter should be highly efficient to extend the battery life and also to avoid frequent recharging of the batteries. The concept of class-D amplification comes as a natural choice where high efficiency is required. The design and implementation of digital input class-D amplifiers has been discussed in detail in this work. The advantages and disadvantages of various digital input class-D topologies have also been detailed out. It is seen that direct conversion of high resolution digital to analog is wasteful of power and degrades signal quality and hence a two step approach has been adopted. The first step is to convert the high resolution digital input into a 1 bit digital signal. In the second step, this digital signal is converted into analog. The various problems associated with using the digital output to directly drive the speaker are that of insufficient supply regula-

tion and other driver non-idealities. It is seen that adopting a negative feedback loop around the class-D driver stage mitigates all the above mentioned problems to a great extent. Yet another problem is the effect of clock jitter at the digital to analog interface. This is a critical problem and has been suppressed by adopting a Finite Impulse Response DAC(FIR-DAC). The design and implementation of the FIR-DAC has been detailed out in this thesis. The dominant source of nonlinearity in closed loop class-D driver stages and ways of improving the linearity using the assisted opamp technique has also been discussed. The design of comparator with inbuilt non overlap generator has also been proposed.

Miscellaneous blocks such as Serial Peripheral Interface(SPI), Bandgap Voltage reference and Low Battery Monitor(LBM) has been discussed. A test board has been designed to aid the testing of the chip. The issues that are to be considered while designing a test board for this sort of an application has been discussed briefly. The thesis concludes with measurement results.

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ABBREVIATIONS

ADC	Analog to Digital Converter
BGR	Bandgap Reference
CMFB	Common Mode Feedback
DAC	Digital to Analog Converter
DSM	Delta Sigma Modulator
DSP	Digital Signal Processor
FIR	Finite Impulse Response
MSA	Maximum Stable Amplitude
NPWM	Natural Pulse Width Modulation
NTF	Noise Transfer Function
OBG	Out of Band Gain
OSR	Oversampling Ratio
PGA	Programmable Gain Amplifier
PSD	Power Spectral Density
PVT	Process Voltage Temperature
PWM	Pulse Width Modulation
SNDR	Signal to Noise and Distortion Ratio
SPI	Serial Peripheral Interface
STF	Signal Transfer Function
THD	Total Harmonic Distortion
UGB	Unity Gain Bandwidth
UPWM	Uniform Pulse Width Modulation

CHAPTER 1

Introduction

1.1 Motivation

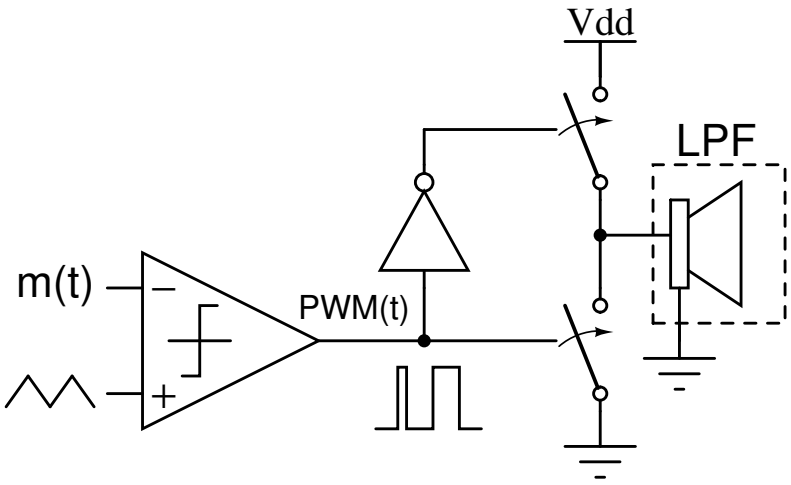

Figure 1.1: Principle of Class-D amplification.

The idea of class-D amplification was proposed more than fifty years ago. The idea is to encode the amplitude information in pulse widths by a coding scheme called pulse width modulation(PWM). The PWM signal is represented using only two amplitude levels and a switch arrangement as shown in Fig.1.1 is used to drive the speaker load. Class-D amplification is still a widely researched topic. The property that makes class-D amplification extremely attractive is efficiency. It is theoretically 100% efficient. This property has made it a formidable competitor to the traditional class-AB audio amplifiers. Distortion and MOSFET technology had been the primary bottlenecks which had restricted class-D amplifiers till the last two decades from making deep inroads into the high-end audio market. With advancements in transistor technology, switches were capable of operating at higher speeds and offered more reliability and these properties proved extremely

favorable for class-D operation. The linearity problem in class-D has also been addressed widely over the past two decades. Solutions range from adopting careful open loop design practices, adopting negative feedback. Since class-D amplifiers are highly efficient it has now become the preffered choice for portable audio. They generate lesser heat than traditional class-A or class-AB amplifiers. This avoids heat sinks almost completely and has led to reduction in size and weight. Another advantage is in its demodulation. The demodulator is just a conventional low pass filter. [1] gives a good overview of the applications where class-D amplifiers have been employed.

An important area where class-D amplifiers are dominating are in hearing aids. The basic components of a modern hearing aid is shown in Fig.1.2. The typical power budgetting in a state of the art digital hearing aid is shown in Fig.1.2[2]. Signal processing requirements will be increasing further in future hearing aids which implies that the DSP would be working at higher power levels. However on the other hand, the overall power consumption cannot be increased further, else the battery life would come down drastically. Therefore, the power consumed by other blocks need to be reduced. Taking the signal chain in Fig.1.2 as a specific example, it can be seen that the backend driver consumes about 33% of the total system's power of 1 mW. By adopting a class-D driver stage for the backend, the power consumption can be easily brought down to less than 10% of the total power. This would enable us to allocate higher power to the DSP for providing advanced functionalities.

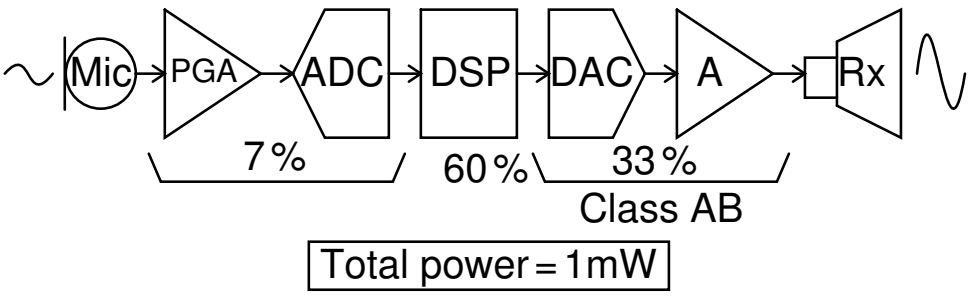

Figure 1.2: Digital hearing aid.

1.2 Design objective

The main objective of this work was to design and fabricate the backend section of a digital hearing aid. A class-D backend driver stage was designed for this purpose. The specifications targetted was in accordance with a commercial product-AIC111. It is a hearing aid chip designed by Texas Instruments.

1.3 Basics of class-D operation

The efficiency advantage of class-D amplifiers is mainly due to the way the signal is encoded. The audio signal which is continuous in amplitude and time can be encoded into pulse widths by comparing it with a relatively higher frequency carrier waveform[3]. The implementation of this coding is shown in Fig.1.3. The output $pwm(t)$ is a two level signal containing the required audio information in its pulse widths.

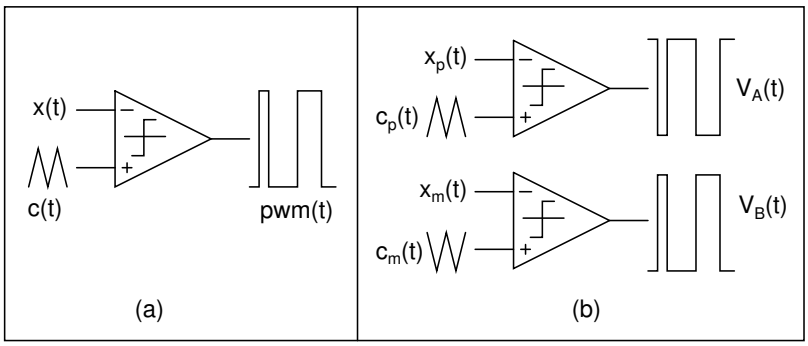

Figure 1.3: (a)Single-ended PWM coding, (b)Differential PWM coding.

This two level differential signal is given to the structure in Fig.1.4.

Let R_L represent the speaker load. When V_A is high, V_B is low and M_3 and M_2 are switched on. This causes the load current to flow from V_{om} to V_{op}. During this state the voltage across M_3 and M_2 is zero and the current through them is $\frac{V_{dd}}{R_L}$. During the state when V_A is low, M_1 and M_4 are on, causing the load current to flow from V_{op} to V_{om}. During this state the voltage across M_1 and M_4

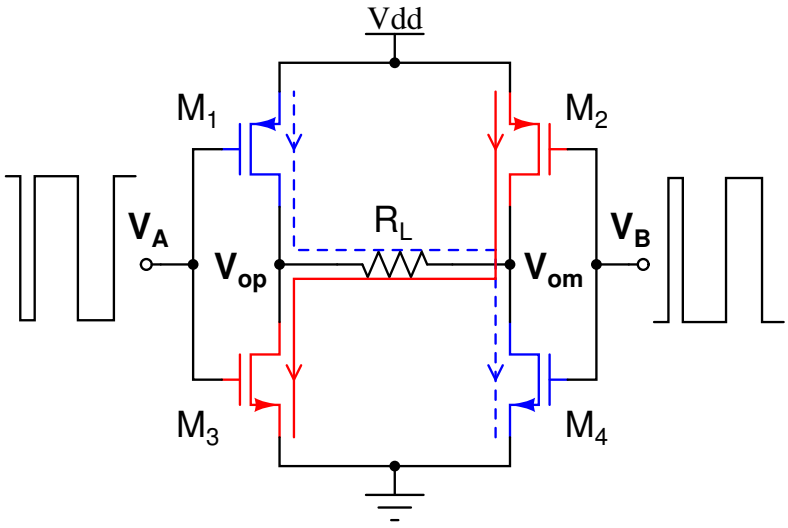

Figure 1.4: Class-D amplification- Principle of operation.

is zero and the current through them is $\frac{V_{dd}}{R_L}$. Therefore at any instant, either the voltage across a pair of transistors are zero or the current through them is zero. This implies that no power is dissipated by the transistors and therefore all the power taken from the supply is transferred to the load resulting in a theoretically hundred percent efficiency.

An advantageous property of the class-D technique is its very simple demodulation. Eventhough the audio information is encoded in pulse widths, recovering the information back is as simple as low pass filtering the PWM waveform. Therefore, the demodulator is just a low pass filter. In the case of speaker loads, the physical construction of the speaker can be electrically modelled as a low pass filter depicted in Fig.1.5 Apart from this low pass filtering, the human ear accounts for further low pass filtering, therefore an explicit low pass filter can be avoided. These properties have made class-D amplifiers an ideal choice for ultra low power audio applications. However, one has also to give importance to practical issues that degrade efficiency in class-D amplifiers. These issues are discussed in Appendix. A.

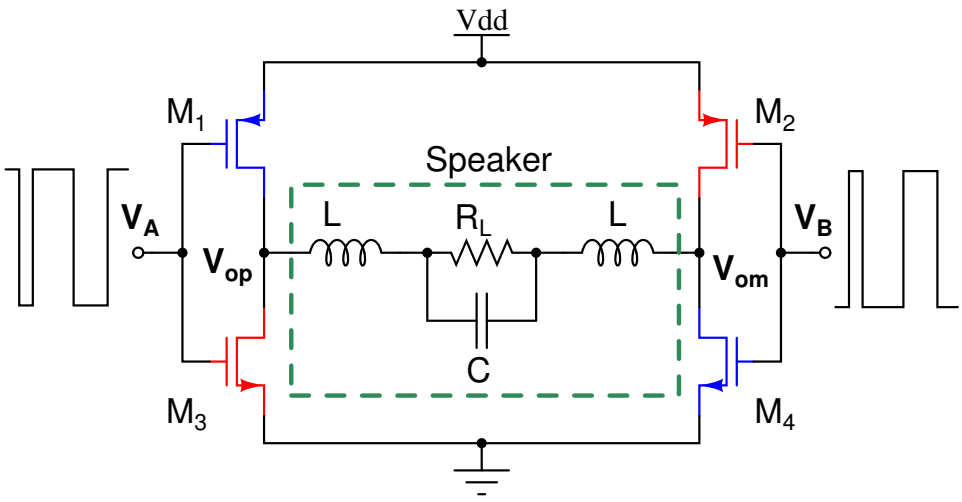

Figure 1.5: Class-D amplification- Speaker load.

1.4 Class-D amplifiers in hearing aids

As already seen in chapter.1.1, digital hearing aids have a driver stage which can adopt the principle of class-D amplification. The DSP might output a 16-bit word stream or even a 24-bit word stream in the case of very high-end audio applications. The problem now is faithfully transforming the 16-bit/24-bit digital signal into analog without any increase in the noise floor and without distorting the input. For converting such high word lengths, it would be almost impossible with conventional Nyquist DACs due to the required component tolerances. Component trimming or other special techniques might be required to achieve good linearity with a considerable increase in the cost of fabrication. Typically for word lengths greater than 12 bits, oversampling digital to analog converters are used. Here, the quantization error noise floor is made to spread out in frequency while maintaining the overall quantization error power. In addition to that, the quantization error in the signal band is shaped out for further improvement in performance. This is finally followed by filtering off the high frequency contents outside the signal bandwidth. The system which performs the above operations is popularly called as Delta Sigma converters or Delta Sigma Modulators(DSM). Delta Sigma converters which accept digital inputs and provide digital outputs are called digital to digital Delta Sigma converters. Those that accept digital inputs and provide analog

outputs are called Delta Sigma DACs(Fig.1.6).

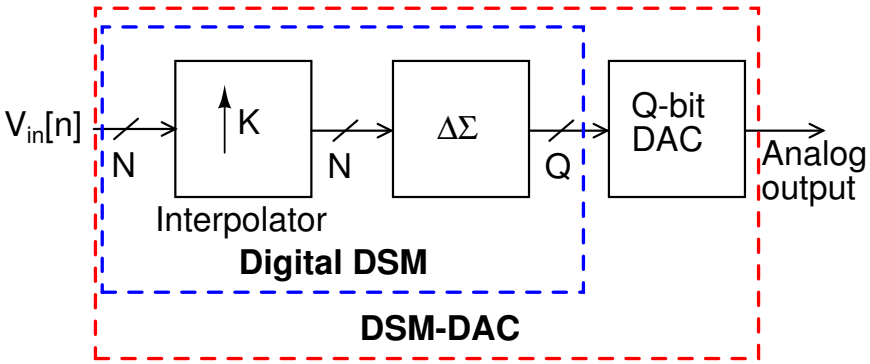

Figure 1.6: Digital input digital output DSM and Delta Sigma DAC.

Both these types of systems are used in digital hearing aids. In hearing aids which has a digital to digital delta sigma, the digital output is converted into analog by means of a conventional Nyquist DAC and then converted into PWM waveform for achieving high efficiency. The advantages and disadvantages of the above techniques are discussed in Chapter.2. This thesis focuses on the analysis, design and measurement of a class-D amplifier for hearing aids.

1.5 Thesis organization

The rest of the thesis is organized as follows;

Chapter 2 discusses how a sixteen bit digital input signal can be converted into a single bit digital signal without distorting the signal.

Chapter 3 discusses why using the above signal directly to drive the speakers is disadvantageous. Further, design of a closed loop driver stage has been proposed as a solution to overcome the disadvantages of directly driving the speakers.

Chapter 4 discusses about other blocks like Serial Peripheral Interface(SPI), Bandgap

Reference(BGR), Low Battery Monitor(LBM) and on-chip current generator. It also discusses chip layout.

Chapter 5 deals with board design, testing and measurement results.

Chapter 6 concludes the thesis and puts forth possible improvements to the existing design.

CHAPTER 2

Digital Input Class-D Amplifiers

2.1 Choice of architecture

In a digital hearing aid, the class-D driver must accept a high resolution(say 16 bits) digital input word that must drive the speakers. Implementation of Nyquist DACs for resolutions greater than 16 bits becomes very non-economical. Practical issues like component mismatches come into picture that makes trimming of elements a must. Therefore, other methods have to be adopted to achieve this digital to analog conversion. A commonly used approach is to convert the higher bit digital signal into a lower bit one and then employ a conventional Nyquist DAC. An important requirement for these DACs is that the output signal must be a 1-bit signal so that the principle of class-D amplification can be employed. This chapter discusses in detail as to how this connversion can be achieved.

2.1.1 Delta Sigma approach

Here the principles of oversampling and noise shaping is used to encode sixteen bits of information in just one bit. The sixteen bit input word is interpolated and fed into a digital delta sigma modulator as shown in Fig.2.1. This 1-bit signal can be used to drive the H-Bridge which further drives the speakers. This method is popularly known as digital input delta-sigma class-D amplifiers[4].

However this approach suffers from the following disadvantages;

- Requires a high carrier frequency to yield the required performance. This leads to a high average switching frequency and thus leads to efficiency degradation.

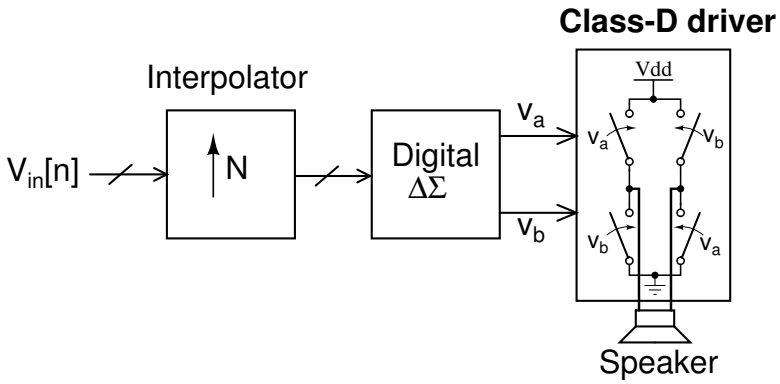

Figure 2.1: Direct Delta Sigma modulation.

- Relatively low maximum stable input amplitude that can be applied to the system. Reduces dynamic range.
- Modulation of clock-jitter and supply noise with data. This will cause an increase in the inband noise floor.

The high average switching frequency can be reduced by using a bit-flipping technique as described in [4]. Another approach is to convert the sixteen bit digital word into an intermediate bit-width using delta-sigma modulation[5]. This is followed by a conventional multi-bit Nyquist DAC. However, the conversion does not stop here. This analog signal should be then encoded into pulse widths to be able to use the concept of class-D amplification. This PWM signal is then used to drive the speakers through a H-Bridge. This technique is illustrated in Fig.2.2.

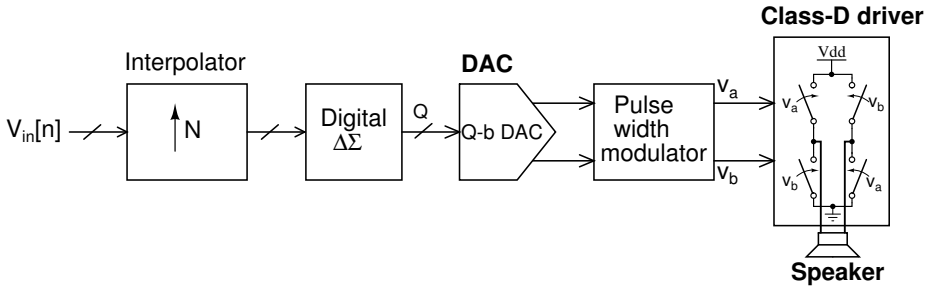

Figure 2.2: Two stage approach- Delta sigma modulation + Analog PWM modulation.

To achieve the same performance, this method requires a lower carrier frequency. This will decrease the average switching frequency and hence the switching losses in the driver stage. This improves the system efficiency. Another benefit is that the maximum stable input amplitude is also higher than that in the previous

method. The above benefits are due to the fact that the quantization noise has been considerably reduced. However, to adopt the principle of class-D amplification one must initially convert the analog signal into a PWM signal. Pulse width modulation can be done by comparing the analog signal with a triangular or a sawtooth carrier. The PWM signal is then given to the H-Bridge which drives the speakers.

Even this approach suffers from quite a few disadvantages;

- The thermal noise and linearity of the multibit-DAC determines the overall dynamic range and linearity of the system respectively.
- Multi-bit DAC requires higher power to satisfy dynamic range and linearity requirements and thus reduces the overall system efficiency.
- To avoid aliasing, the carrier frequency used in the PWM modulator must be greater than the digital DSM's clock frequency. To mitigate this problem an anti-aliasing low-pass filter must be used before the PWM modulator. Again, the linearity and the noise introduced by this filter will be a problem.
- The other non-linearities associated with the PWM generation will also affect the performance of the system.

There are another class of converters which uses pulse width modulation and are described next.

2.1.2 PWM approach

Theoretically, the sixteen bit digital input signal can be mapped to 2^{16} pulse widths. This process of mapping a discrete-time input into pulse widths is known as UPWM- Uniform pulse width modulation. The resulting PWM waveform can be given as input to H-Bridge which then drives the speakers as illustrated in Fig.2.3. Though the idea is simple, there are practical difficulties in its implementation. If the 16-bit digital input comes at a rate of, say 40 kHz, then the clock required for UPWM conversion would be $2^{16} \cdot 40\,\text{kHz}$, i.e. 2.56 GHz. Clocks of this frequency are difficult to generate and would cause the PWM generator block to

consume considerable power. Another disadvantage with the above approach is the inherent non-linearity in direct PCM to PWM conversion. In other words, UPWM is a non-linear modulation scheme[6].

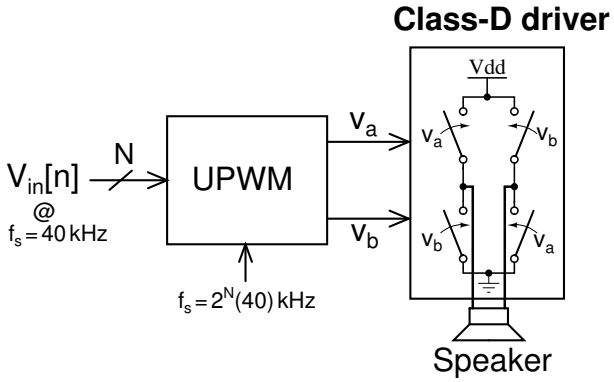

Figure 2.3: Direct PWM modulation.

An elegant approach has been proposed[7, 8] to address the problems encountered by the above system. The idea is to reduce the word length of the input signal (to say, Q) by using delta sigma modulation and then performing UPWM modulation on this reduced word length. The advantage with this approach is that the operating frequency of the pulse generator block is drastically reduced. This system is shown in Fig.2.4. In short, the delta-sigma modulator helps to drastically reduce

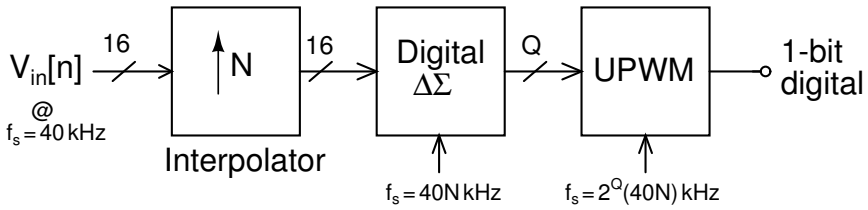

Figure 2.4: Hybrid approach- Essentially PWM modulation.

the frequency of operation of the pulse generator block. However, there is one fundamental disadvantage associated with this system and that is non-linearity. The process of directly mapping a uniformly sampled signal into pulse widths(UPWM) is a non-linear operation in itself[6]. This operation leads to high levels of signal distortion. The distortion causing mechanism is described in Appendix. B. The solution to this problem is to mimic naturally-sampled PWM(NPWM).

Natural PWM refers to the process of converting naturally sampled points into pulse widths. Naturally sampled points refer to those points that are got as the intersection between an equivalent analog signal and an analog carrier. From a different perspective, the naturally sampled points can lie anywhere in the amplitude-time plane. The reason that one strives to approach towards NPWM is that it does not give rise to base-band distortion[3], eventhough there can be harmonic/non-harmonic distortion due to the spilling of sidebands. However in digital systems, the sampling is uniform and the amplitude is quantized. Converting this type of a signal into pulse widths leads to direct base-band distortion. Therefore, the input signal must not be directly noise-shaped and converted into pulse widths. Instead, the cross points of the input signal with a sawtooth/triangular carrier (both hypothetically assumed to be continuous in time and amplitude)has to be estimated. This cross-point information can be given to a delta-sigma converter and then converted into pulse widths. This method essentially performs the NPWM operation. Therefore, it is also called Pseudo NPWM or algorithmic PWM[8]. This system is illustrated in Fig.2.5.

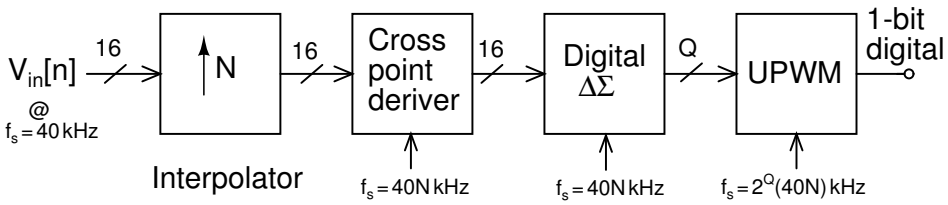

Figure 2.5: Hybrid approach- Approximating NPWM modulation.

The PWM-based approach has several advantages when compared with the delta-sigma-based approach.

- The pulse repetition frequency is lower.
- The achievable dynamic range is higher. (Larger amplitude inputs can be applied without causing stability issues)
- If the cross-points are accurately calculated, the PWM-approach would theoretically be extremely linear, since it approaches NPWM.
- The output of the pulse generator block is always one bit in amplitude and thereby lends itself directly to class-D amplification.

Considering the advantages of the PWM-approach, the system in Fig.2.5 has been adopted for this work.

2.2 Implementation

The targeted performance is shown in Table 2.1

Table 2.1: Design specifications for the class-D backend driver section

Signal bandwidth	100 Hz to 10 kHz
Input bit-width	16 bits at 40 kHz
SNR	>96 dB
THD	better than -85 dB
Supply voltage	1.2 V
Technology	130 nm standard process

The design of each block of Fig.2.5 is described in detail in the following subsections.

2.2.1 Cross-point deriver

The reason cross-point deriver is being discussed first is that the PWM modulation scheme is decided at this stage. Depending on the modulation scheme, the sampling frequency of the delta-sigma converter would be fixed. System-wise, the interpolator and the delta-sigma modulator comprise closely related blocks and would be discussed together. However, it is to be kept in mind that the input to this block is the output of the interpolator.

The main aim of the cross-point deriver block is to estimate what would have been the cross-points if a continuous-time version of the input signal was compared with a continuous-time carrier. An important design parameter to be chosen here is the type of carrier that is to be assumed. The carrier waveform can either be leading-edge or trailing-edge sawtooth(NADS) or a triangular waveform(NADD) as shown in Fig.2.6.

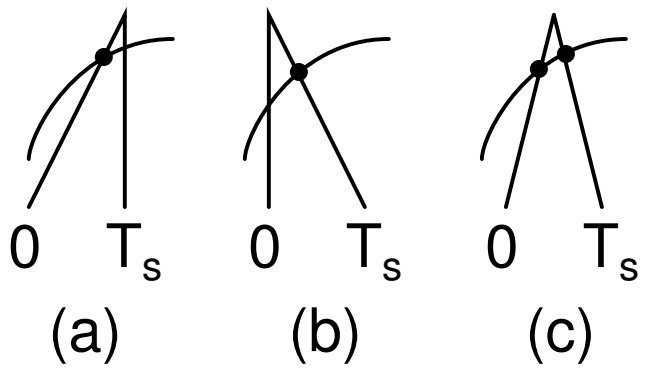

Figure 2.6: (a)Leading edge modulation, (b)Trailing edge modulation, (c)Double-edge modulation.

The benefit of double sided modulation is that the even components of the carrier and the intermodulation components cancel out [6]. However, now two cross-points would be required for every pulse. Therefore, the pulse generator must employ two counters one for counting the delay and the other for generating the width[7]. Therefore, this scheme requires more hardware and is complicated in implementation. If the carrier is a sawtooth only one cross-point information is required for every pulse and thus the delay for the pulse to start would always be zero(in trailing edge modulation). This means that a single counter would be sufficient. It would be an up-counter if the modulation was trailing edge PWM and a down-counter if it was a leading edge modulation or vice versa depending on implementation. Therefore, single-sided, leading edge sawtooth was chosen as the carrier.

Now that the modulation scheme has been fixed, the next design parameter to choose is the carrier frequency. If the cross-point deriver block works exactly as required, then the modulation can be considered to be NPWM. Ideally, the output spectrum should look like that in Fig.2.7. The noise floor is limited by the simulation accuracy only.

From Fig.2.7 it can be seen that there is no base-band distortion but there are lot of side-bands for the carrier. If the carrier frequency is small, these sidebands can extend all the way down into the signal band. This could either lead to harmonic

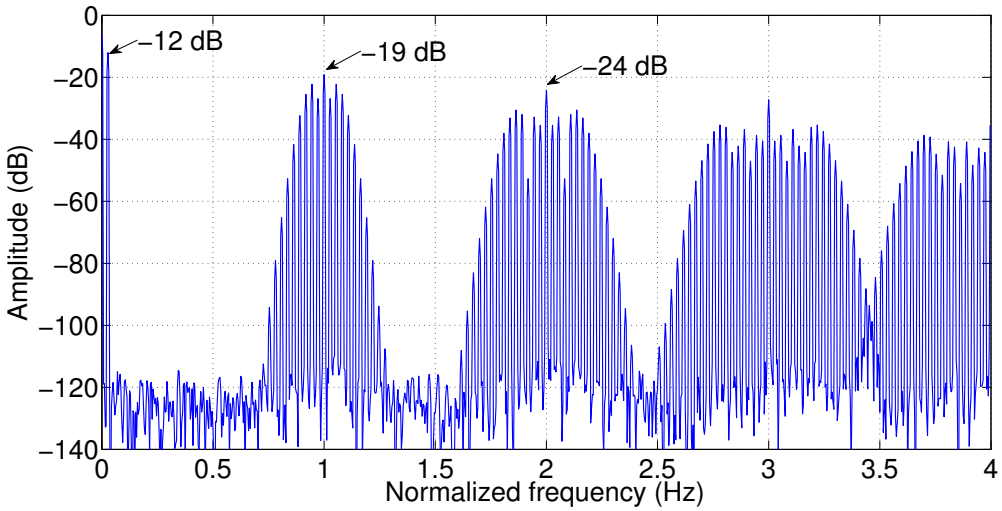

Figure 2.7: PSD of ideal NADS modulation.

or non-harmonic distortion. From Fig.2.7, it is seen that atleast 10 sidebands of the carrier are visible above the noise floor. Infact, taking more number points for calculating the PSD would reveal the buried harmonics. Therefore, there is a lower limit to the carrier frequency. In addition to the above, the cross-point deriver block would not be able to approach the NPWM cross-points precisely in practice. This would lead to direct signal-distortion. Another issue is that the carrier frequency has to be chosen such that the delta sigma modulator would be able to faithfully encode the cross-point information. Taking into account these practical issues, the carrier frequency has been fixed to be 64 times the signal band-edge frequency so that the design requirements are met.

The next step is to implement an algorithm that estimates the naturally sampled cross-points. The idea is illustrated in Fig.2.8.

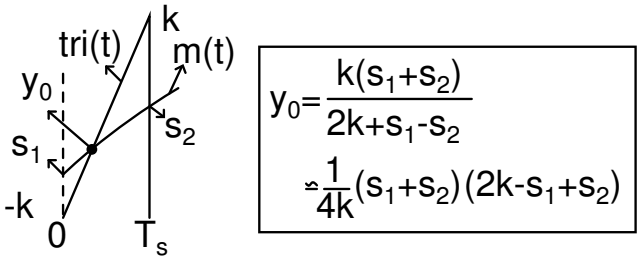

Figure 2.8: Cross-point deriver- Estimating naturally sampled points.

Consider a single period of the carrier as shown in Fig.2.8. Let s_1 and s_2 be two adjacent samples of the digital message. Let $tri(t)$ be the hypothetical continuous-time, leading-edged sawtooth carrier. If the hypothetical equivalent analog message is m(t), then the cross-point is Y_0 as shown. Since the carrier frequency is many times higher than the message frequency, m(t) can be assumed to be piecewise linear within each carrier cycle. This gives ;

$$\mathrm{m(t)} = \frac{s_2 - s_1}{T_s} t + s_1 \tag{2.1}$$

and

$$\mathrm{tri(t)} = \frac{2k}{T_s} t - k \tag{2.2}$$

Equating the above two gives the instant at which both curves meet. This instant is mapped into amplitude and the resulting solution can be calculated to be

$$Y_0 \approx \frac{k(s_1 + s_2)}{2k + s_1 - s_2} \tag{2.3}$$

The above equation has a division operator. In digital implementations, division operations are power hungry and would require extra hardware. Therefore, binomial theorem was applied to bring the denominator into the numerator. 2k can be taken out as a common factor and since $\frac{s_1 - s_2}{2k}$ is very small due to oversampling, the binomial approximation would be relatively accurate even with only the first order term. The final equation is

$$Y_0 \approx \frac{1}{4k}(s_1 + s_2)(2k - s_1 + s_2) \tag{2.4}$$

The above equation is coded in verilog and is synthesized using Design Vision. A point to note is that the word-length of each cross-point need not be higher than that of the interpolated digital input signal. In other words, the number of digital codes between any s_1 and s_2 is very large. Since the value of the cross-point will be somewhere between s_1 and s_2, extra resolution need not be allocated for the

resultant cross-points.

2.2.2 Digital Delta Sigma modulator

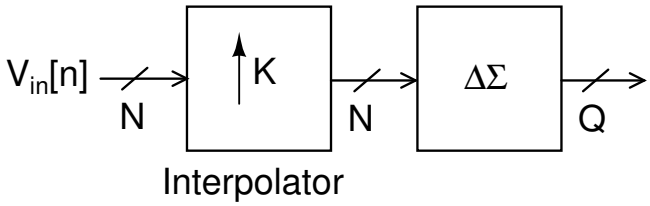

Figure 2.9: Digital Delta-Sigma modulator.

The requirement of this block is to faithfully encode the sixteen bit cross-point information in a smaller number of bits. The oversampling ratio(OSR) for this modulator has already been fixed by choosing the carrier frequency of the sawtooth in the previous block. Therefore, the OSR is 32. Now, the design choices to be made are the number of quantizer bits and the order of the loop filter. It is a well known fact that the output of the delta sigma not only contains the cross-point information but also considerable high-frequency shaped quantization noise power. Therefore, both the signal and the high-frequency noise gets pulse-width-modulated and would cause fold-back into the signal band. The amount of fold-back can be reduced by reducing the amount of high frequency content at the output of the DSM. This can be done by increasing the number of quantizer bits or reducing the out-of-band-gain(OBG). However, reducing the OBG would increase the in-band noise floor and thus degrade the accuracy with which the cross-points are encoded. Therefore the option is to choose a higher number of quantizer bits that would satisfy the requirements both in the signal band and in the high-frequency band. However, the number of bits in the quantizer must not be chosen too high, as it means the clock frequency required for pulse generator(UPWM) block would also be high. Considering these factors and through simulations it was decided to use a five bit quantizer for the DSM.

The architecture of the DSM is chosen to be of the error-feedback type as shown

in Fig.2.10.

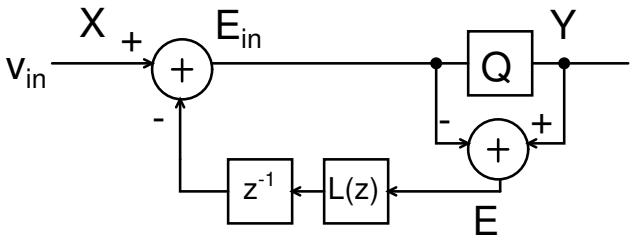

Figure 2.10: Error feedback digital Delta Sigma modulator.

The advantage with this architecture is that if the noise transfer function(NTF) is FIR then the loop filter can also have an FIR structure. This fact can be confirmed from the below equations.

$$E_{in}(z) = X(z) - E(z)L(z)z^{-1} \tag{2.5}$$

$$E(z) = Y(z) - E_{in}(z) \tag{2.6}$$

$$Y(z) = E(z) + X(z) - E(z)L(z)z^{-1} \tag{2.7}$$

$$= X(z) + E(z)[1 - L(z)z^{-1}] \tag{2.8}$$

This equation is of the form

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \tag{2.9}$$

Therefore,

$$STF = 1 \tag{2.10}$$

$$NTF = 1 - L(z)z^{-1} \tag{2.11}$$

$$L(z) = z[1 - NTF(z)] \tag{2.12}$$

Therefore, if NTF is FIR, the loop filter transfer function is also FIR. An FIR implementation is advantageous because the word-lengths for all the internal nodes can be pre-determined exactly and it does not give rise to stability issues if properly

designed [9].

The condition for stability of an error feedback digital delta sigma modulator is that the maximum gain of the loop filter should be less than 2^{Q-1}. Here, Q is the number of quantizer bits. In order to prove this, consider Fig.2.11. Assume that

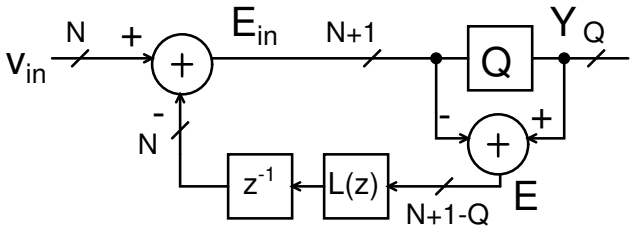

Figure 2.11: Allowed word lengths for stable operation.

initially both the input and fedback signal has a word length of N bits. Then, E_{in} will have N+1 bits. Since the digital quantizer is just a word truncator, E will have N+1-Q bits. Now if a loop filter with a worst case gain of 2^Q is chosen then, the output of the loop will have N+1 bits. Therefore, in the next cycle, E_{in} will have N+2 bits and so on. Two cycles later, E_{in} will have N+3 bits. Therefore, ultimately the system blows up and saturates. This proves that the maximum gain the loop filter can have for stable operation is 2^{Q-1}.

Next, the procedure for designing the loop filter is discussed. MATLAB has a toolbox named the delta sigma toolbox which can aid in the design of delta sigma modulators. However, if both Out of Band Gain(OBG) and order are fixed, it can give only IIR-NTFs. Therefore, the IIR-NTF has to be converted into FIR-NTF through custom design. This IIR-NTF is chosen so that it conforms to the stability criteria as discussed in the previous subsection. From the stability criteria it can be deduced that the worst case gain(OBG) of the NTF can be one greater than that of the loop filter's. Since a five bit quantizer is to be used, the maximum loop filter gain is restricted to be 16 and therefore that of the NTF can be 17. From simulations, a fifteenth order FIR-NTF was designed to give approximately the

same frequency response as that of the IIR-NTF. The NTF obtained was,

$$\begin{aligned} NTF(z) = 1.0000 &- 1.3945z^{-1} - 0.3906z^{-2} + 0.2822z^{-3} + 0.4072z^{-4} \\ &+ 0.2979z^{-5} + 0.1514z^{-6} - 0.0645z^{-7} - 0.1611z^{-8} - 0.0752z^{-9} \\ &- 0.0664z^{-10} - 0.0460z^{-11} + 0.0254z^{-12} - 0.1064z^{-13} + 0.1406z^{-14} \end{aligned} \tag{2.13}$$

The NTF frequency response is shown in Fig.2.12. This NTF response is after the coefficients were quantized. It is due to this coefficient quantization that the complex zeros are not exactly on the imaginary and thus have a relatively lower quality factor.

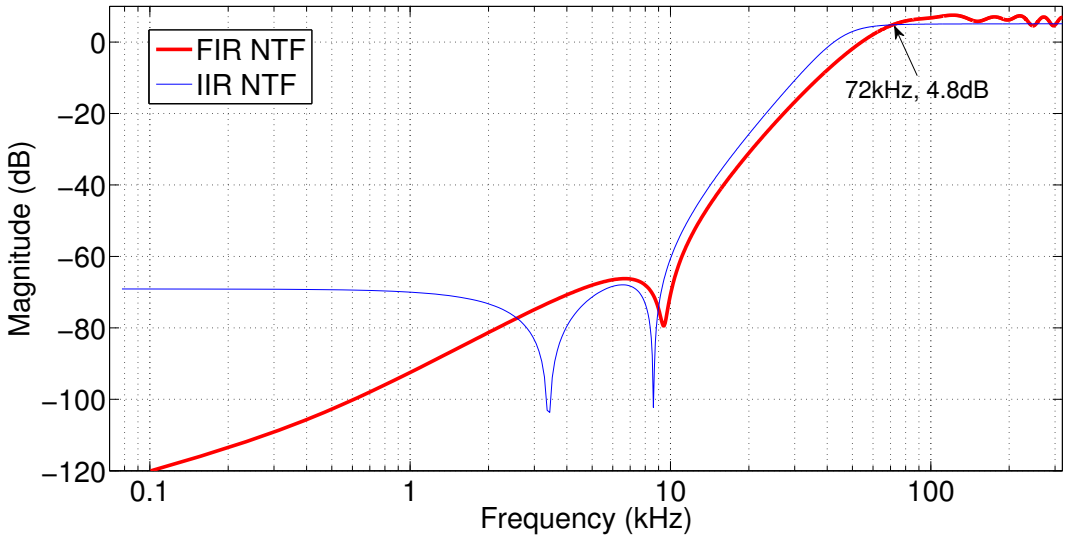

Figure 2.12: Matching IIR-NTF with FIR-NTF.

The loop filter transfer function is obtained as,

$$\begin{aligned} L(z) = 1.3945 &+ 0.3906z^{-1} - 0.2822z^{-2} - 0.4072z^{-3} \\ &- 0.2979z^{-4} - 0.1514z^{-5} + 0.0645z^{-6} + 0.1611z^{-7} + 0.0752z^{-8} \\ &+ 0.0664z^{-9} + 0.0460z^{-10} - 0.0254z^{-11} + 0.1064z^{-12} - 0.1406z^{-13} \end{aligned} \tag{2.14}$$

The FIR structure of the loop-filter L(z) is shown in Fig.2.13. Here, a_k refers to

the k^{th} coefficient of the NTF(Eq.2.13).

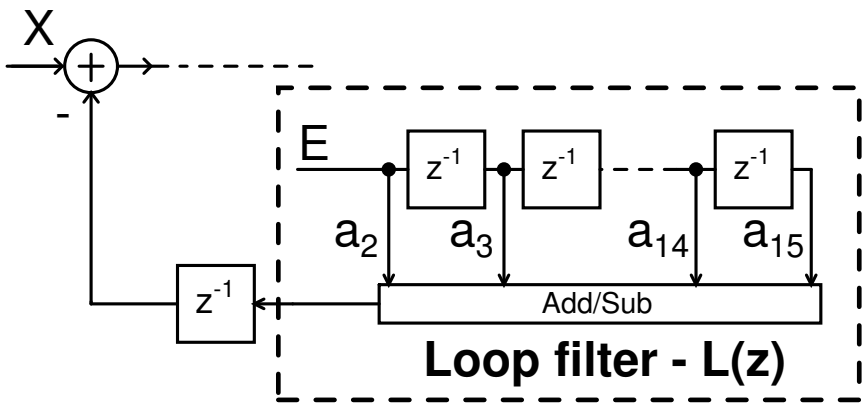

Figure 2.13: Architecture of the FIR loop filter.

The overall digital delta sigma modulator with word lengths is shown in Fig.2.14 This architecture was coded in verilog and synthesised using Design Vision.

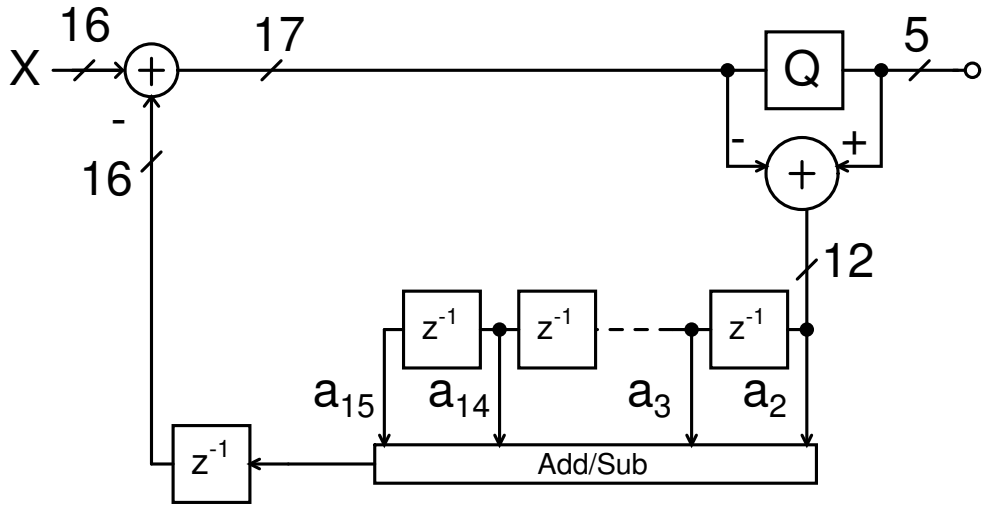

Figure 2.14: Overall architecture of digital Delta Sigma modulator.

2.2.3 Interpolator

The input to the DSM block must be at the frequency of operation of the DSM. However, the input signal is a sixteen bit signal coming at 40 kHz. Therefore, the incoming signal has to be upsampled without distorting the signal band. The signal band-edge is 10 kHz and the OSR of the DSM is 32. Therefore, the DSM works at 640 kHz. Hence, the interpolator must interpolate by a factor of sixteen.

Interpolating by a factor of 16 at one shot would make its design very complicated and would waste considerable power. Instead, the interpolation can be split into multiple stages. There are multiple options to interpolate by a factor of 16. They are, 2x2x2x2, 2x4x2,4x4,2x8 and 8x2. It turns out that after every stage of interpolation a Low Pass Filter(LPF) is required to attenuate the images at the multiples of the carrier frequency. Therefore in the case of an 8x2 interpolator, the LPF would be operating at a very high frequency and hence its wasteful on power. Another reason is that the normalized cut-off frequency of the LPF would be very small leading to difficulties in its design. In the case of 2x8 interpolator, the design of the first LPF would be optimal but that of the final LPF would be more difficult because of lower normalized cut-off frequencies. 2x2x2x2 and 2x4x2 interpolators would require more low pass filters than the others and hence use more power and may lead to more in-band signal droop. The 4x4 interpolator is optimal in the sense that only two LPFs are needed, with the design complexity distributed evenly between the two stages. Hence a 4x4 interpolator has been adopted. The structure of the 4x4 interpolator along with the LPF H(z) is shown in Fig.2.15. It is to be noted that all the coefficients were chosen as a power of two as the multiplication can be easily done by just bit-shifts. However choosing such integer coefficients makes the DC gain greater than unity and specifically eight in this particular design. This filtered output is again upsampled by four. However this does not cause an increase in word length. Therefore, the output signal of the interpolator (which is the input to the cross-point deriver) is nineteen bits wide.

Upsampling by 4 is just repeating the same sample 4 times, but at a faster rate. B[n] is obtained from A[n] as shown in Fig.2.16.

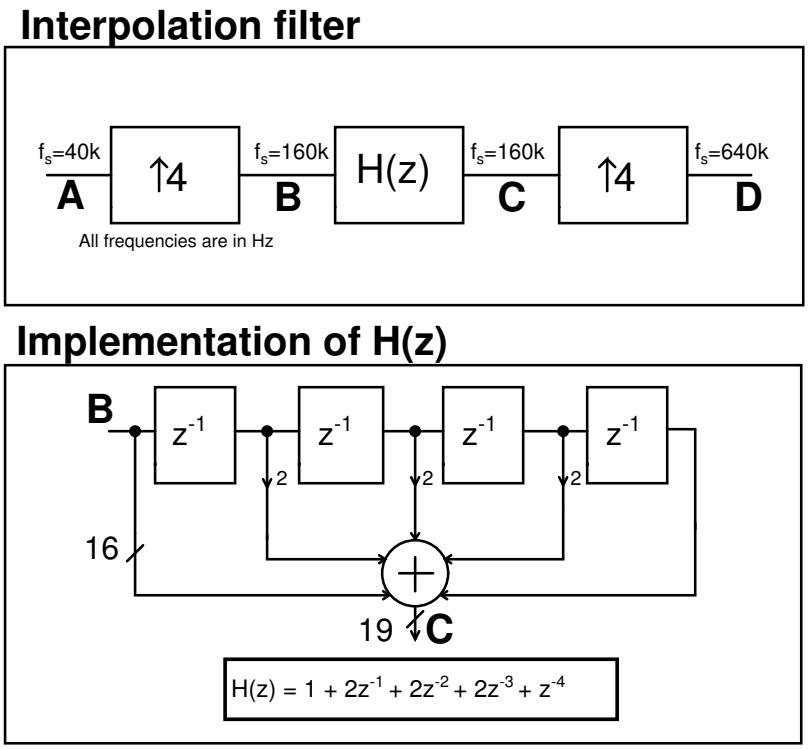

Figure 2.15: Interpolation filter and the explicit low pass FIR filter.

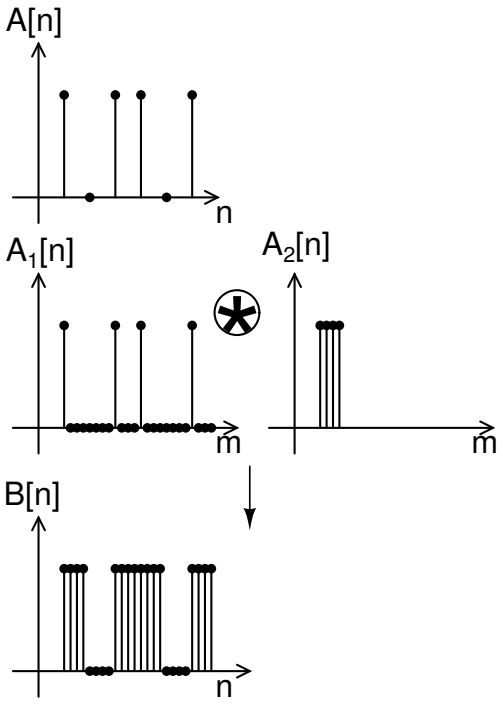

Figure 2.16: Operation of repeating the same value at a higher rate.

Let the discrete-time Fourier transforms of the signals can be written as,

$$A[n] \leftrightarrow A(e^{j\omega}) \tag{2.15}$$

$$A_1[n] \leftrightarrow A(e^{j4\omega}) \tag{2.16}$$

$$A_2[n] \leftrightarrow 1 + e^{-j\omega} + e^{-2j\omega} + e^{-3j\omega} \tag{2.17}$$

$$= 4e^{-j\frac{3\omega}{2}} cos\left(\frac{\omega}{2}\right) cos(\omega) \tag{2.18}$$

$$B[n] \leftrightarrow A_1(e^{j\omega})A_2(e^{j\omega}) \tag{2.19}$$

The above equation has nulls at $\frac{f_s}{4}$ and $\frac{f_s}{2}$ and therefore repeating the same value does inherent filtering as shown in Fig.2.17.

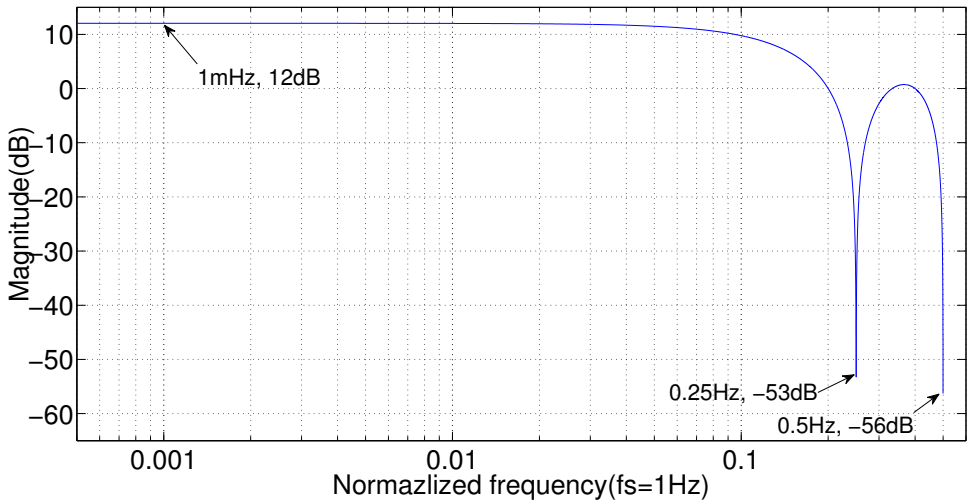

Figure 2.17: Frequency response of the inherent filtering.

The second stage of interpolation by four is similar to that of the first stage. Therefore, there are three stages of filtering in all, where one is an explicit filter H(z) and the other two are the inherent filtering got by repeating the same value four times. From simulations it was found that another stage of explicit filtering is not required. Overall frequency response of the interpolator is shown in Fig.2.18.

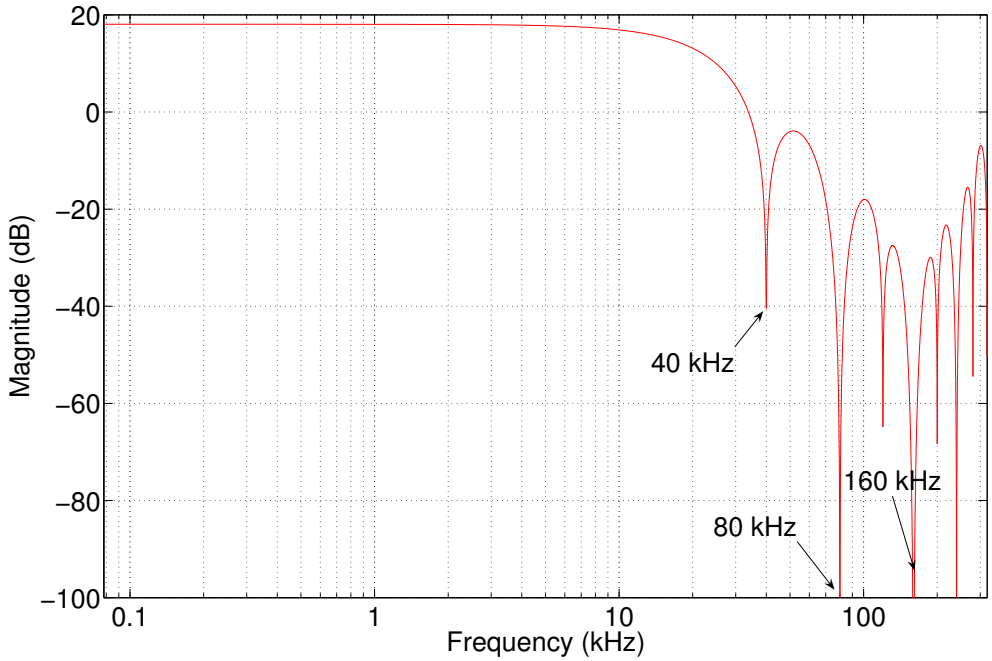

Figure 2.18: Overall frequency response of the interpolator (320 kHz corresponds to $\frac{f_s}{2}$).

2.2.4 UPWM

This forms the final block of the sixteen bit digital to one bit digital converter. This block takes in DSM's five bit output and maps it into pulse widths. This is nothing but a counter which gets a start pulse based on the input amplitude it receives from the DSM. It receives the stop bit at the beginning of every carrier cycle. This block needs to work at $2^5 \cdot 640$ kHz, i.e, 20.48 MHz. This block needs the highest frequency sampling clock in the whole system and hence the power consumed by this block would be significant. Thanks to the DSM block this highest frequency was restricted to 20.48 MHz.

All the above blocks were coded in verilog and the functionality was tested using MODELSIM. Once the design requirements were met, the gate-level synthesis was done using DESIGN VISION. The synthesized block was laid out using ENCOUNTER.

2.2.5 Performance summary

The layout-extracted netlist was simulated and the PSD of the signals at various nodes were plotted. The input signal is a single-tone sinusoid having an amplitude 0.95 times the maximum stable amplitude and a frequency of 625 Hz. The output spectrum was calculated after applying a Hanning window and averaging the PSDs over two cycles. This is shown in Fig.2.19

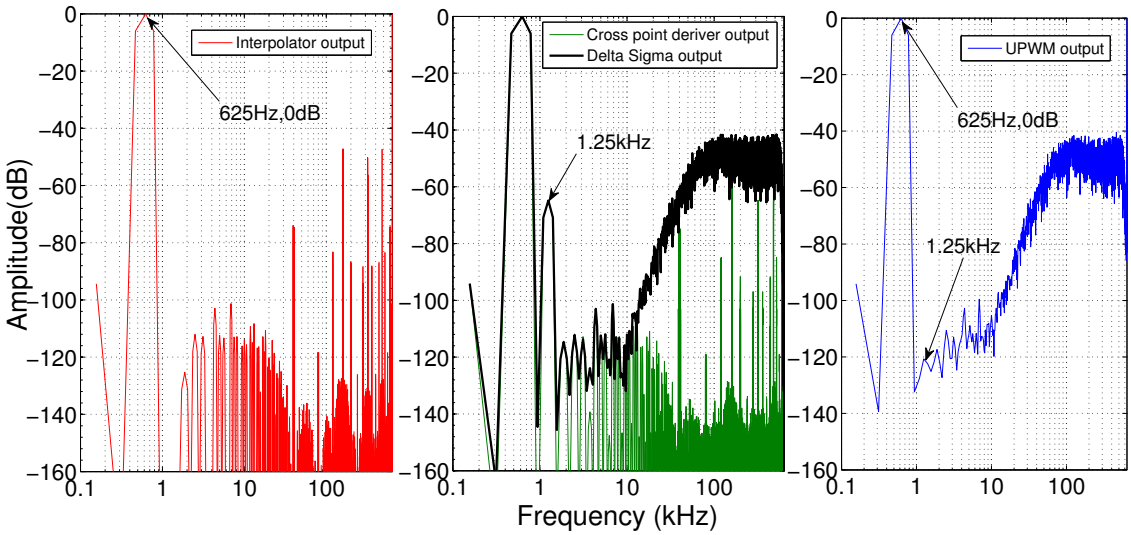

Figure 2.19: PSD of the signals at the output of various blocks.

With reference to Fig.2.19, it is clear that the final UPWM output is distortion free eventhough the output of the delta sigma modulator and the cross-point deriver are distorted. However, these should not be considered as distortion but instead as pre-distortion. This predistortion gets cancelled by the distortion of the UPWM block. Hence, the output will be free of distortion as shown in Fig.2.19.

The input amplitude was swept and the SNDR, SNR and THD was calculated for each input amplitude. This curve is plotted in Fig.2.20. From Fig.2.20, it is clear that the dynamic range specifications are also met.

The performance achieved from the sixteen bit to one bit converter is tabulated in Table 2.2.

The UPWM block consumes the maximum power as it operates at the maximum

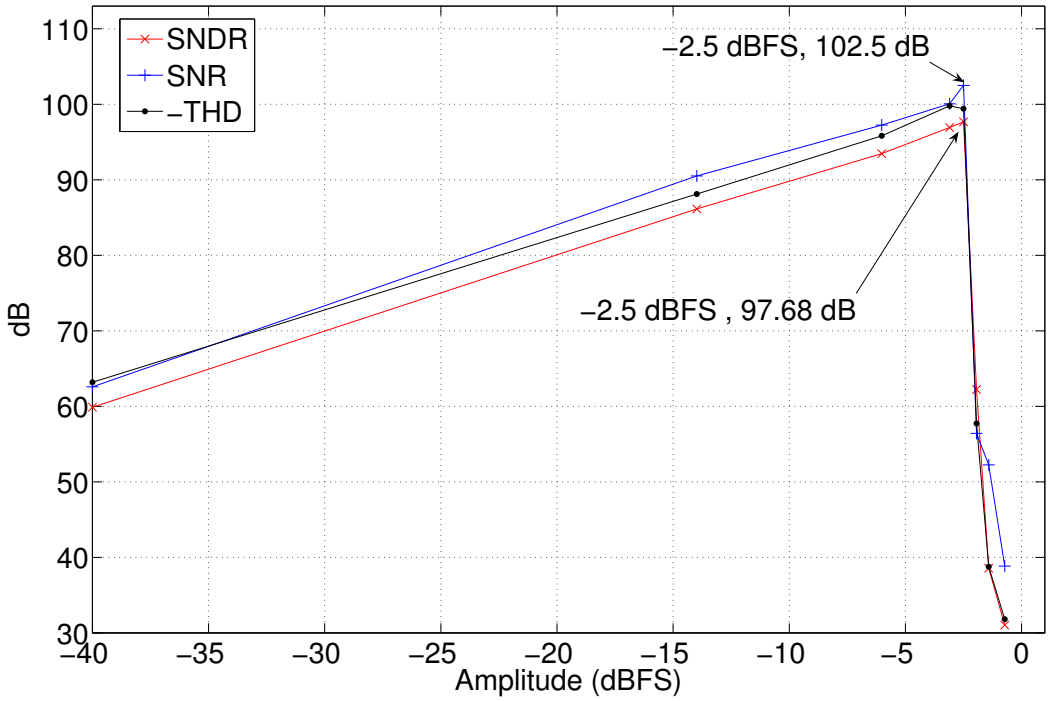

Figure 2.20: Amplitude sweep

Table 2.2: Performance summary of the digital section of the class-D backend driver

Area	250 μm x 250 μm
Power	33 μW
Interpolator	17 %
Cross-point deriver	7 %
Digital DSM	32 %
UPWM block	38 %
SNDR	97.662 dB
THD	-102.225 dB

clock frequency of $2^5 \cdot 640\,\text{kHz} = 20.48\,\text{MHz}$. From Table.2.2 it is clear that the required specifications were met. The next step is to use this one bit signal to drive the speakers. This is discussed in the next chapter.

CHAPTER 3

Analog section of class-D amplifier

3.1 Introduction

The procedure to convert a sixteen bit signal into a one bit signal without losing any information was discussed in Chapter 2. Now, this one bit signal should be applied to the speakers without any further loss in the signal quality. Apart from that, it must also be able to efficiently drive the speakers.

If the one bit digital signal is directly applied to class-D power stage, there are several issues that degrade the quality of the signal. The most important issue is clock jitter-data modulation. The problem of jitter occurs at the digital to analog interface and is especially severe for systems whose output has a large amount of high frequency content. A typical example is the DSM. The clock used for the digital system will usually have jittery edges and therefore the DAC's output will also have jittery edges. This causes the charge transferred into the speaker also to be jittery. This phenomenon causes the clock jitter spectrum to modulate with the data spectrum and increases the noise floor within the signal band. In the case of oversampled converters, the high frequency regions(around $\frac{f_s}{2}$ contribute to much of the increase in the inband noise floor. This is depicted in Fig.3.1

One way to mitigate this problem is to retime the data using a low-jitter clock and then give it to the H-Bridge. However, getting a low jitter clock might be expensive and/or power hungry. Another way to mitigate this problem is using a one bit switched capacitor DAC(SC-DAC). Here the amount of charge transferred is independent of the clock and is ideally limited only by the noise on the references used for the charge-transfer. Therefore, the jitter suppression can be ideally very

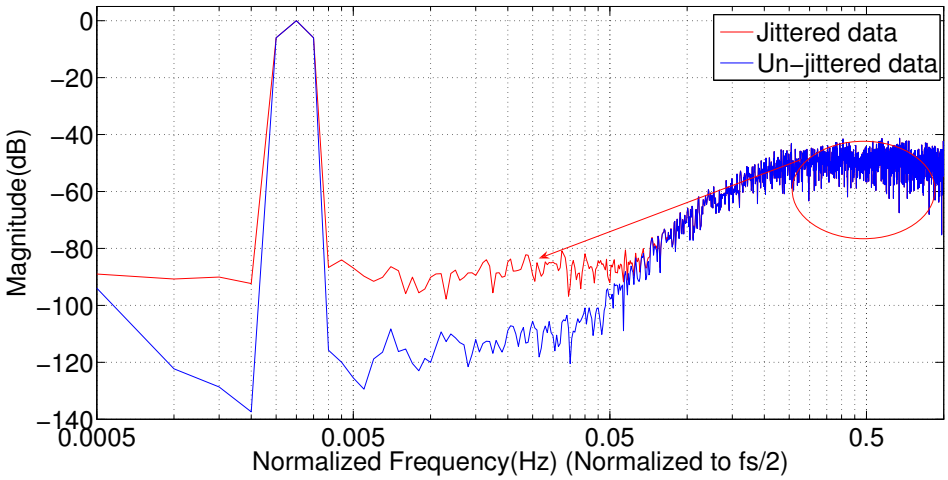

Figure 3.1: Clock jitter modulating with data and raising the inband.

good. Other types of DAC pulses can also be chosen to reduce jitter-sensitivity. However, there is an important issue with using DAC pulses that are not rectangular. Non-rectangular pulses do not lend themselves directly to adopt the principle of class-D amplification. Another stage of PWM would be required to convert the signal back into rectangular shape. This was illustrated in Chapter.2 in Fig.2.2. Since now the final PWM stage requires generation of an analog carrier and uses an analog comparator, there are many sources of non-linearities and errors which can counter the advantage of reducing jitter.

Since jitter should definitely be suppressed to be able to meet the design requirements, changes must be made in the DAC pulse shape even at the expense of using an analog PWM block. However, a negative feedback loop would have to be built around the PWM driver stage to suppress the non-idealities encountered there. It turns out that, using a closed-loop analog class-D stage does not only help in choosing an arbitrary pulse shape to keep jitter under control, but also is very beneficial to suppress other non-idealities in the driver stage.

Another important reason why a closed loop solution is much better than an open loop one is that of PSRR. Any noise or stray signal on the supply or ground modulates with the data. If data is represented as D(t) and the output voltage

across the load as $V_L(t)$ then,

$$V_L(t) = [V_{dd}(t) - V_{gnd}(t)] \cdot D(t) \tag{3.1}$$

The data is either +1 or -1. Therefore, the supply spectrum convolves with the data spectrum giving rise to problems similar to that of jitter data modulation. This issue is severe at high input amplitudes. A proven approach to improve the PSRR is to build a feedback loop around the H-Bridge. This solves many problems at one go. It helps improve the PSRR considerably, attenuates non-linearities arising due to dead-time and finite rise and fall times of the PWM signal. The dead-time nonlinearity is particularly severe in class-D amplifiers and hence a closed loop solution is a must for hi-fidelity and large dynamic range audio amplifiers. Therefore, a closed loop analog solution has been adopted in this work.

Since a closed-loop analog class-D driver stage is going to be employed, it is advantageous in many aspects to make the loop fully differential. A fundamental advantage is that the H-Bridge can output four times higher power than that of a single ended structure. The other benefits are that all even harmonics gets cancelled out and the disturbances that are common-mode to the loop is rejected. Another important advantage specific to audio applications is that the DC component across the load can be removed without using a negative supply. DC across the speaker can potentially damage it. If a negative supply is not available, huge DC blocking capacitors which occupy excessive area would need to be used. On the other hand, going for a fully differential structure would mean double the number of components and hence four times the area(all the four switches must have twice the width of the single-ended version to maintain the same on-resistance).

3.2 Target specifications

The targetted performance is shown in Table 3.1

Table 3.1: Target specifications for the analog section of the class-D driver

Signal bandwidth	100 Hz to 10 kHz
Dynamic range	>94.50 dB
THD	better than -70.00 dB
Thermal noise	$12\,\mu V_{rms}$
PSRR	>55 dB
Output impedance	$20\,\Omega/40\,\Omega$

3.3 Loop filter Design

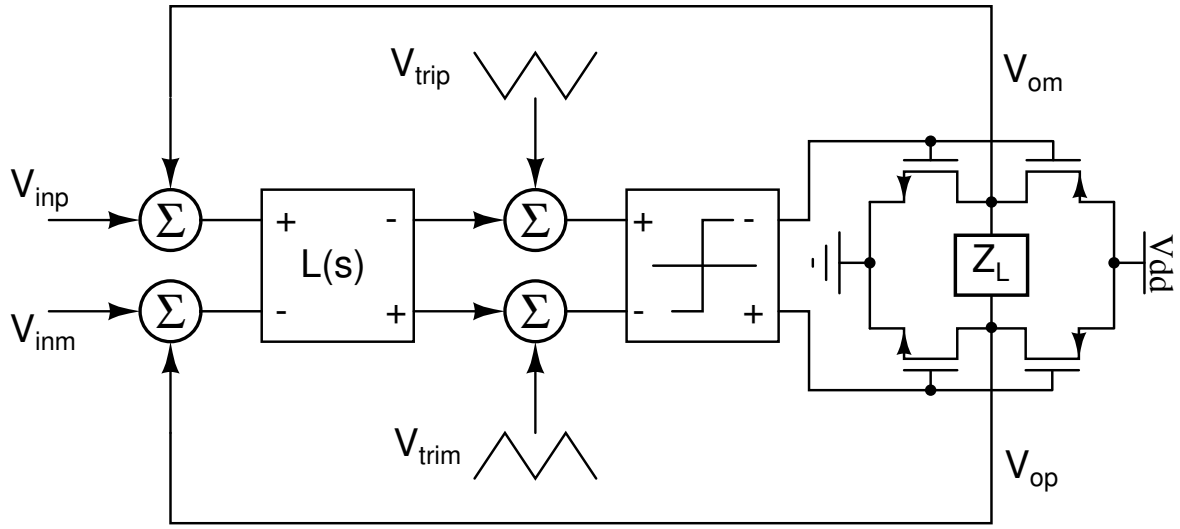

Figure 3.2: Architecture of closed-loop Class-D amplifier.

Fig.3.2 shows the architecture of a closed-loop class-D amplifier. The first summer calculates the error between the input signal and the fedback signal within the unity gain bandwidth of the loop. This error signal is applied as input to the loop filter, L. The loop filter is generally an integrator or a cascade of integrators. Effectively, the differential output of the loop filter is compared with a differential triangular carrier to generate the PWM signal. This PWM signal is given as input to the H-Bridge which drives the speakers. This type of modulation is known as NADD modulation(where both the message and carrier are out of phase across the differential arms) and is well suited for fully differential circuits because it has no common-mode component at its output. Another advantage is that the radiation from the output wires that carry the PWM is minimum because of no common-mode components (only common-mode components radiate).

The design choices that are to be made are, the loop filter's order and bandwidth and the triangular carrier's amplitude and frequency. All the above parameters cannot be chosen in a single-shot and some iteration is required. The frequency of the triangular carrier is chosen based on the allowable switching loss, inband performance and the type of demodulation filter. Too high a switching frequency would cause efficiency degradation due to higher switching losses but would lead to a lower order demodulation filter and a better inband performance. On the other hand, a lower carrier frequency would lead to lower switching losses but at the expense of a poorer inband performance and a higher order demodulation filter. A compromise has to be arrived on the carrier frequency, weighing the requirements of the above three issues. From simulations, 640 kHz was chosen to be the carrier frequency.

The next design choice to make is the order of the loop filter. As a starting point, the Unity Gain Bandwidth(UGB) of the loop can be assumed to be 300 kHz, which is atleast two times lower than the carrier frequency. If it is desired to have atleast 50 dB loop gain at the signal band-edge frequency of 10 kHz, a second order loop filter would be required. The architecture of the second order loop filter is shown in Fig.3.3. The reason for choosing such an architecture and the reason for using FIR-DAC will become clear later in this chapter.

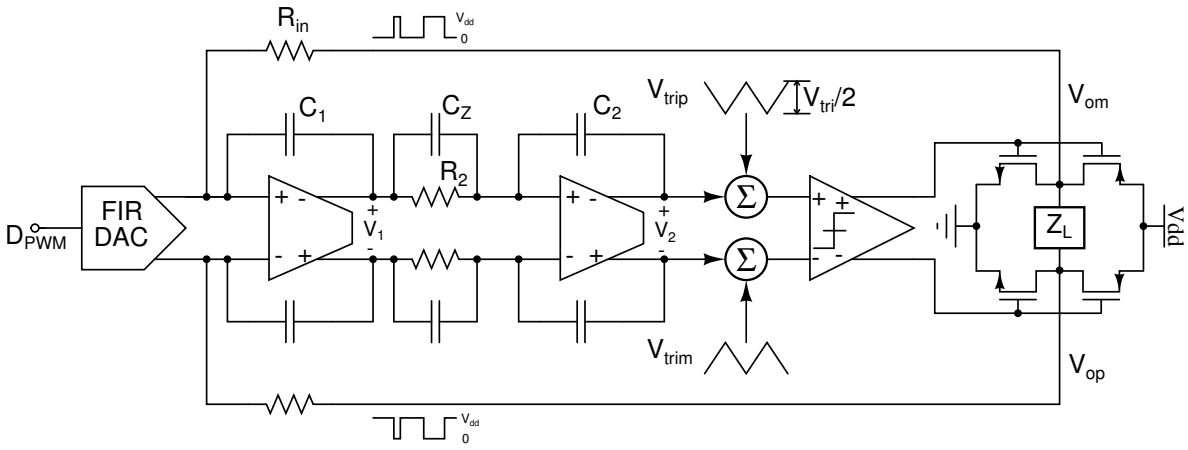

Figure 3.3: Second order closed-loop Class-D amplifier.

It should be noted that implementing the system in Fig.3.3 would require a triangle

wave generator and a summer. A better implementation of this system is shown in Fig.3.4. In this modified version, a pulse voltage waveform having fifty percent

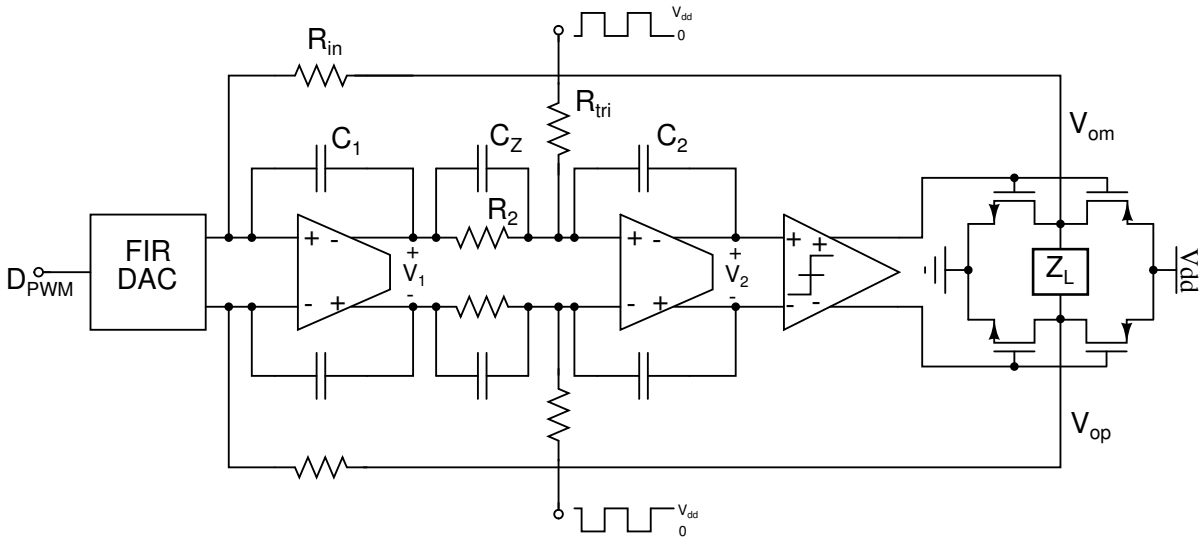

Figure 3.4: Second order closed-loop Class-D amplifier with triangular carrier generator.

duty cycle is integrated by the second integrator. Therefore, the output of the second integrator is the sum of the triangular carrier and the output of the second order loop filter. Therefore, the second integrator is used to advantage as it acts both to increase low-frequency loop gain and as a triangle wave generator. This architecture is advantageous in the sense that, the system-clock or its sub-multiple can be directly used as the square wave that gets integrated to form the triangular carrier. Another advantage is that the high-frequency jitter in the square-wave clock is attenuated by the second integrator before getting shaped by the feedback loop [10].

The next important thing to be considered is stability. There are two main reasons that cause instability in closed-loop PWM class-D amplifiers. They are;

1. Ripple stability criteria[6]- High loop-UGB, or in other words, the slope of the loop-filter's output being greater than the slope of the triangular carrier.
2. Excessive delay in the loop or phase margin problem.

The first requirement is fundamental to PWM loops whereas the second is a general design issue in all negative feedback loops. To state the first stability problem

differently, if the amplitude of the signal that is to be compared with the triangular carrier is greater than the amplitude of the triangular carrier itself, then PWM output is saturated and no natural sampling occurs. This condition is illustrated in Fig.3.5. In principle, the dotted pulse should have been generated but it was missed due to overloading.

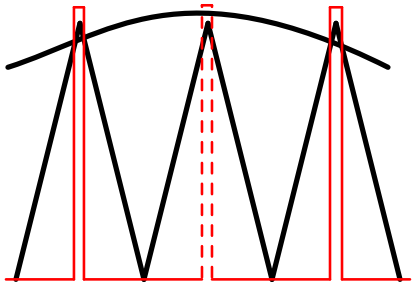

Figure 3.5: Ripple stability criteria being violated.

This is similar to the overloading of quantizers in a delta sigma modulator. When this condition occurs the pulse width becomes greater than one sampling period. This will cause the integrator's output to saturate. It might happen that the modulator will never be able to come out of this saturated state, since the feedback is broken. This is a large signal phenomenon and it depends on the system architecture. For converting the above stability criteria in terms of system parameters, consider Fig.3.3. Fig.3.3 is chosen instead of Fig.3.4 for a more visually intuitive analysis. Let's initially restrict the input to be only DC having an amplitude of V_{cm} which is equal to $\frac{V_{dd}}{2}$. This is the amplitude that gives the maximum worst-case ripple and it corresponds to a duty cycle(D) of 0.5. Ideally, by virtue of negative feedback, one would expect the second integrator's differential output to also be just a DC voltage of value V_{cm}. However, due to the high-frequency components in the fedback signal, additional ripple is introduced over the DC waveform as shown in Fig.3.6.

The swing at V_1 is mainly due to the ripple caused by the fedback PWM voltage and the swing at V_2 is sum of the scaled ripple at V_1 and the wanted signal. The second order path does not contribute much to the ripple at V_2 because of its very

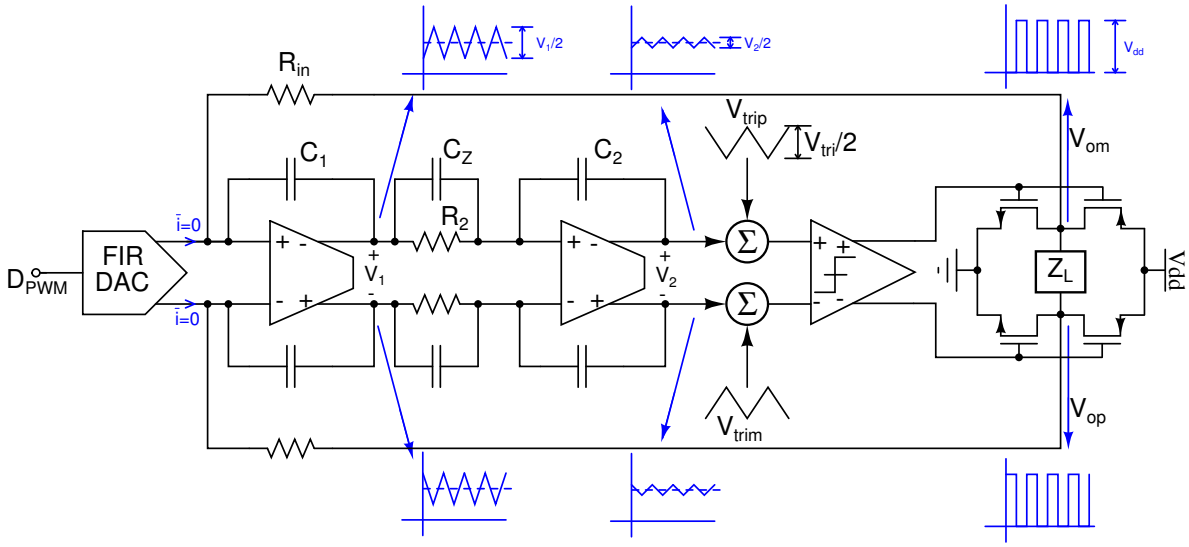

Figure 3.6: Waveforms at required nodes for calculating stability requirements.

low gain at the carrier frequency($\frac{1}{T_s}$). Therefore;

$$|V_1| = \frac{V_{dd}}{R_{in}C_1}\frac{T_s}{2} \tag{3.2}$$

$$|V_2| \approx \frac{V_{dd}}{R_{in}C_1}\frac{T_s}{2}\frac{C_Z}{C_2} \tag{3.3}$$

The condition for stability is;

$$V_2 < V_{tri} \tag{3.4}$$

$$\frac{V_{dd}}{R_{in}C_1}\frac{T_s}{2}\frac{C_Z}{C_2} < V_{tri} \tag{3.5}$$

From Fig.3.4,

$$V_{tri} = \frac{V_{dd}}{R_{tri}}\frac{T_s}{2C_2} \tag{3.6}$$

therefore from Eq.3.5,

$$\frac{V_{dd}}{R_{in}C_1}\frac{T_s}{2}\frac{C_Z}{C_2} < \frac{V_{dd}}{R_{tri}}\frac{T_s}{2C_2}$$

$$R_{tri} < R_{in}\frac{C_1}{C_Z} \tag{3.7}$$

The above equation shows that there is a minimum required triangular carrier

amplitude below which the modulator becomes unstable. Another point to take away from this derivation is in Eq.3.7. From it, it is clear that changing the supply or f_s does not change the stability of the loop(in this particular architecture). Therefore, this loop's stability is supply and clock-frequency independent.

It is also possible to derive a relation between the UGB of the loop and the carrier frequency that ensures that the loop remains stable. To calculate the UGB of the loop, consider the linearized version of the open loop of the corresponding closed-loop class-D amplifier which is shown in Fig.3.7.

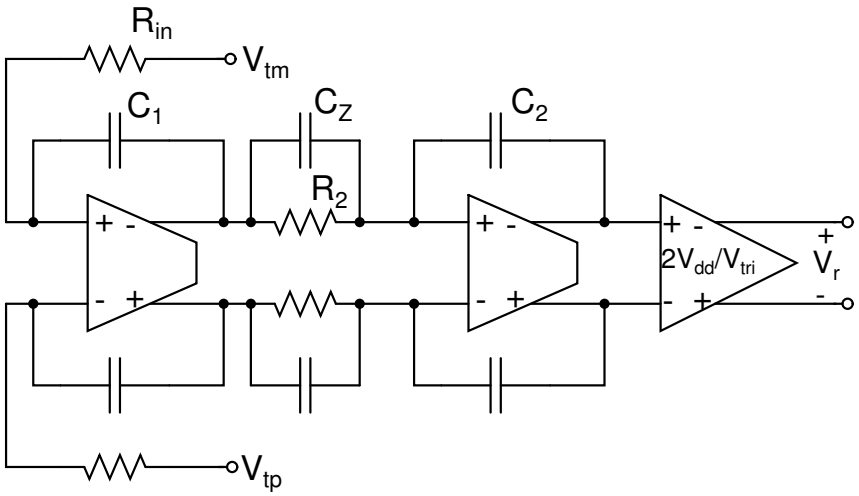

Figure 3.7: Linearized Class-D loop.

Note that the FIR-DAC does not come into picture as it is across a low-impedance node and ground. From Fig.3.3, the nonlinear block is the PWM generator which includes the comparator and the H-Bridge driver. The low-frequency linear model of these two blocks put together is a simple gain stage having a gain $\frac{2V_{dd}}{V_{tri}}$ as explained in Appendix. C.

The UGB of the open-loop is derived below;

$$V_r(s) = -V_{td}\frac{1}{sR_{in}C_1}\left[\frac{C_Z}{C_2} + \frac{1}{sR_2C_2}\right]\frac{2V_{dd}}{V_{tri}} \tag{3.8}$$

where V_{td} is $V_{tm} - V_{tp}$

For the loop to remain stable, the loop-gain must cross the UGB with a slope of

-20 dB/decade. In other words, the system should be first order around the loop's UGB. Therefore, the zero frequency is chosen to be well within the UGB. This implies that the system is asymptotically first order around UGB and hence we can neglect the second order path for calculating the UGB. Therefore,

$$\text{UGB} = \frac{C_Z}{R_{in}C_1C_2}\frac{2V_{dd}}{V_{tri}} \tag{3.9}$$

Combining Eq.3.5 and Eq.3.9;

$$\text{UGB} < \frac{2f_c}{\pi} \tag{3.10}$$

Here, f_c is the triangular carrier frequency. However, if the input is a signal, then the ripple is superimposed on a scaled version of the input signal at the input of the comparator. Therefore, in practice, the carrier frequency is chosen atleast two to five times the required loop bandwidth.

To tackle the second problem of excessive delay around a loop, a fast path/bypass path is provided around one of the delay causing blocks. In other words a zero is introduced into the loop. From Fig.3.3, 3.4, the capacitor C_Z is the compensation capacitor which provides a bypass path around the second integrator at high frequencies. This can also be thought of as adding a zero to the loop, with the zero frequency being $\frac{1}{R_2C_Z}$. Therefore, correctly choosing the value of capacitor C_Z solves the phase margin problem.

The next design step is to choose components such that the noise-power constraints are met. The maximum allowed noise power is 144 pW (Table.3.1). The major contributors of noise in this system are the feedback resistors, input resistors(FIR-DAC) and the amplifier of the first integrator. For now, the FIR-DAC can be assumed to be a simple resistor of value R_{in} within the range of analysis, that is, the signal band. Let $S_{R_{in,n}}$ and $S_{amp1,n}$ denote the input-referred noise power spectral density of the resistors(and also for the FIR-DAC) and the amplifier of

the first integrator, respectively. It is also assumed for now that, the amplifier is a simple two-stage, Miller-compensated structure. Then the contribution of thermal noise at the output is;

$$S_{out,n} = 4S_{R_{in,n}} + 4S_{amp1,n} \tag{3.11}$$

where, $S_{R_{in,n}}$=4kTBR_{in}+flicker noise, where k=Boltzman's constant, B=signal bandwidth(10 kHz), T_{max}=343 K and $S_{amp1,n} = \frac{16kT}{3g_m}$+ flicker noise, where g_m is the transconductance of the input pair of the amplifier of the first integrator. The load transistors of the first stage also contributes to noise but however the noise power is divided by the g_m^2 of the input pair. Therefore, if the g_m of the input pair is chosen much higher than the load transistor's g_m, its noise contribution would be relatively less. It should be noted that the flicker noise is also a dominant contributor to the inband noise power. The bulk of the noise contribution comes from the lower frequencies. However, this noise can be easily reduced by increasing the device sizes and does not cause a direct power penalty as in the case of reducing thermal noise. However, since now the devices are larger, the parasitics also increase and one might be required to burn more power to meet the required specifications.

R_{in} is mainly chosen based on noise(Eq.3.11) and linearity constraints. Therefore, the input resistors cannot be very large in value. The input resistors cannot also be too small because it would then demand huge currents from the non-linear amplifiers of the integrators. This might give rise to linearity issues depending upon the architecture adopted for the amplifier. This is also wasteful of power as a larger quiescent current is required in the driving stage of the amplifier in the first integrator in order to keep the distortion at respectable levels. From the allowed noise budget, it is advantageous to make the resistor contribute more to noise than the amplifier. Since now, to reduce the noise contribution from the amplifier, more power will be burnt to increase the g_m of the input pair and always increasing the g_m of the amplifier would have other benefits namely, reducing problems due

to transistor mismatch, random offsets and any error at the output of the first stage. Therefore it was decided to make the resistor contribute 60% of the 144 pW budget. This corresponds to a typical resistance value of 100 kΩ after accounting for process and temperature variations of the resistance.

The components C_1, R_2, C_Z, C_2 and V_{tri} were chosen based on the stability constraints(Eq.3.10) and the required loop-UGB(300 kHz). Through simulations, the system parameters decided upon is shown in Fig.3.8. (Note: V_{dd}=1.2 V). The values arrived at is after node-scaling.

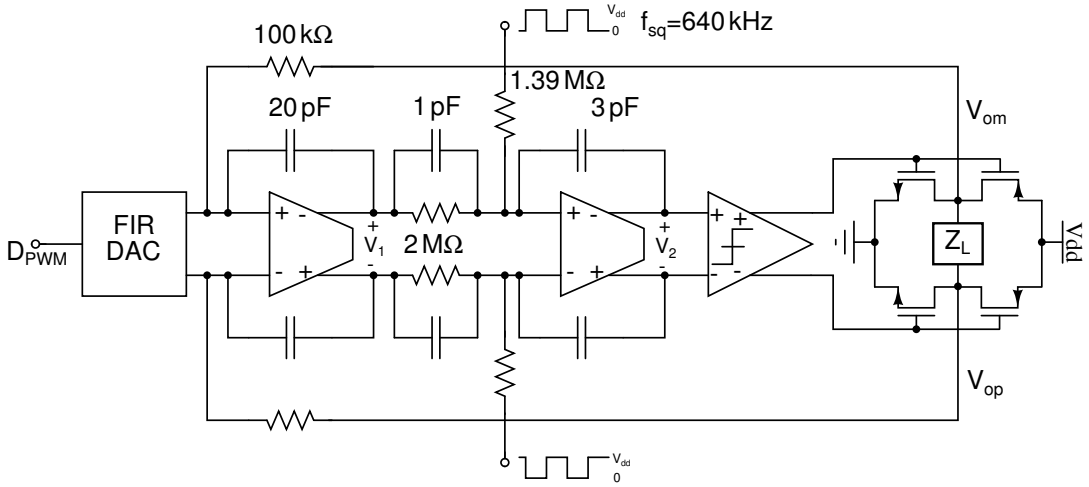

Figure 3.8: Closed loop class-D amplifier with component values indicated.

The loop gain and the phase margin plots vs frequency is shown in Fig.3.9.

3.3.1 Finite Impulse Response DAC (FIR-DAC)

The problem of clock-jitter modulating with the data surfaces at the digital to analog interface. The reason is that the charge transferred in each cycle into the analog blocks is itself jittery due to the jittery clock. One solution is to use a switched capacitor DAC(SC-DAC). Here, the amount of charge transferred is independent of the clock as long as the capacitor charges/discharges to the final value. However, it draws huge spiky currents during clock transitions which will cause the amplifier in the first integrator to slew. This slewing causes the amplifier

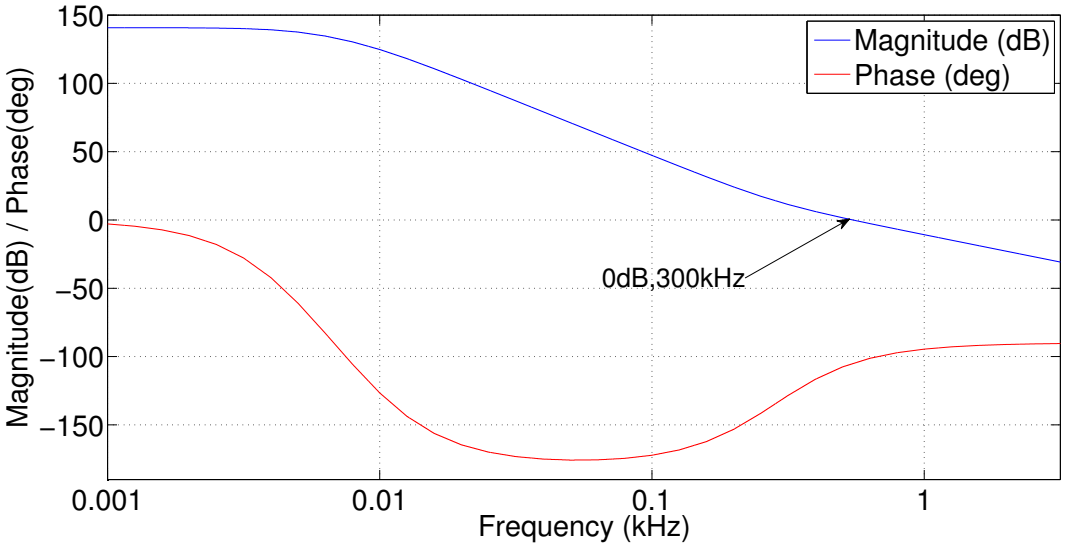

Figure 3.9: Magnitude and phase response of the Class-D loop.

to become non-linear and causes distortion. Another way is to retime the 1-bit digital output using a low-jitter clock. The disadvantage in this approach is the requirement/availability of a low-jitter clock.

An elegant way of reducing the effect of jitter on the amount of charge transferred is by using an FIR-DAC. The general structure of an FIR-DAC is shown in Fig.3.10. It is to be realized that the major contribution to increase in inband noise floor due

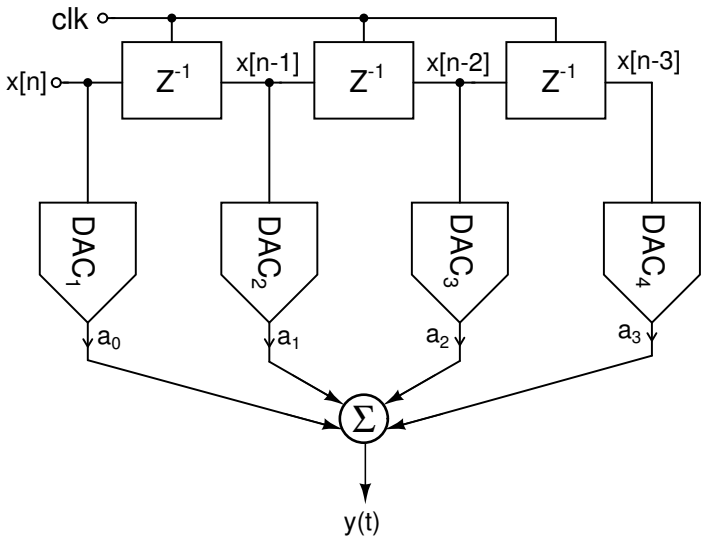

Figure 3.10: Architecture of a 4-tap FIR-DAC.

to data-jitter modulation is from the folding back of high frequency components of the data. Hence by filtering out the high frequency data, the amount of fold-back

can be reduced. This is exactly what an FIR-FILTER-DAC does. Therefore, the basic idea is to filter out the high frequency components around $\frac{f_s}{2}$.

The mechanism by which this architecture reduces jitter can be understood with the help of Fig.3.11.

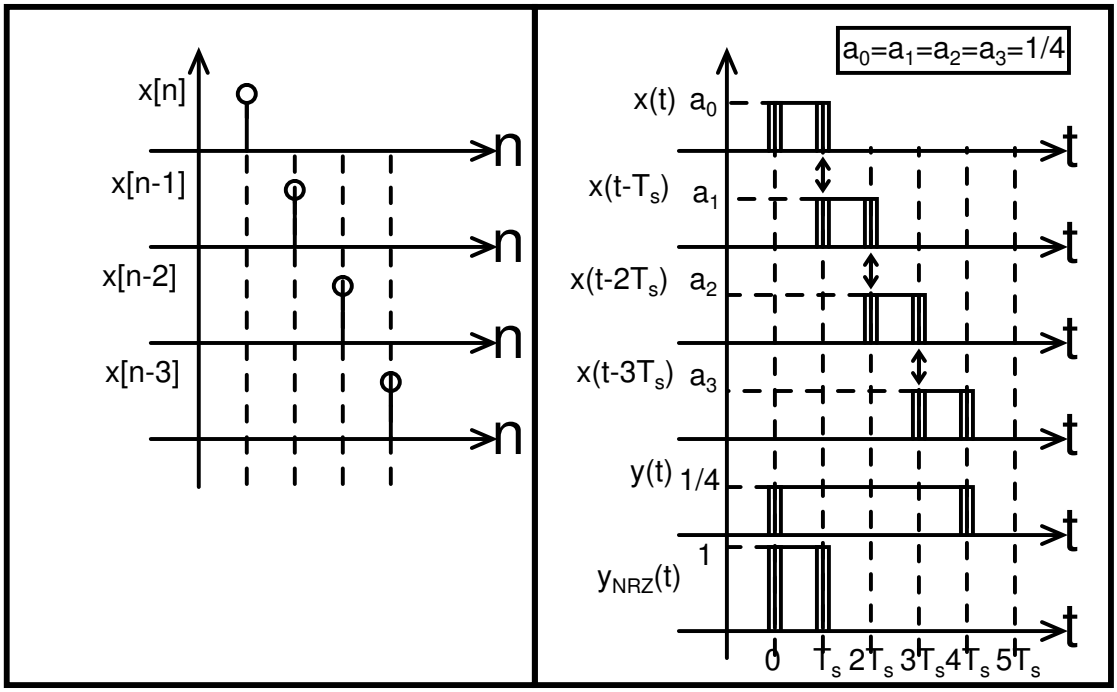

Figure 3.11: Jitter cancelling mechanism in FIR-DAC.

All the DAC elements are of the Non-Return-to-Zero(NRZ) type. Assume for simplicity that all the coefficients has the same value. The co-efficients are scaled to make the DC gain unity. Consider the input x[n] to be a digital impulse. The corresponding signal at each node of Fig.3.10 is shown in Fig.3.11. The jittery edges during data transitions is due to the fact that the instant at which the clock changes its state itself is jittery and quite random. Therefore the area of the shaded portion represents the error in the amount of charge that has been transferred to the analog system due to the clock edges being jittered. From the illustration, the main point to note is that any error in the charge transferred in the current cycle is compensated by the error in the charge transferred in the next cycle. This is because, if the clock period of the current cycle increases (relative to the ideal reference period) then, the clock period of the next cycle

automatically reduces(assuming the other edge is jitter-free). This cancellation property is true for all the intermediate cycles except for the first and the last cycle. Therefore, only the jitter in the first and the last cycle matters. The error in charge that gets compensated is indicated by double-arrows in Fig.3.11. The above cancellation does not occur if say a Return-to-Zero DAC(RZ-DAC) is used for the DAC elements but however, it gives lower jitter sensitivity than a simple RZ DAC because of the filtering of high frequency components.

Another way to think of this is that now the input data is low pass filtered in the digital domain. Therefore, the total power that gets modulated with jitter is reduced. This implies that performing a better low-pass filtering action by increasing the number of taps will furthur reduce the jitter sensitivity. However in reality, it will be limited by the jitter caused due to the delay elements itself. Therefore, if the frequency profile of the data is known, the FIR filter can be cleverly designed to reduce the jitter sensitivity. Say if it is known that there is a large spur at $\frac{f_s}{6}$, an FIR filter with a notch at $\frac{f_s}{6}$ can be designed.

It is worthy to compare the jitter sensitivity of an N-tap FIR with a multibit-bit quantizer. For the same inband performance, the NTF of a single-bit quantizer must have a higher out of band gain(OBG) than that of a multi-bit modulator. This is because the quantization noise is higher in single bit modulators and thus the inband of the NTF has to have more attenuation. Therefore in the case of multi-bit modulators, the high frequency components in the modulator output is reduced greatly and thus the fold back due to jitter is also reduced greatly. The same reduction in high frequency components can also be got by designing an FIR filter with similar high frequency characteristics. Thus, an FIR-DAC has the capability of having the same jitter sensitivity as that of a multi-bit quantizer.

The jitter sensitivity of the FIR-DAC can be calculated as follows; if the z-transform of data is denoted as D(z), the jitter spectrum as J(z), the error spectrum

as $J_e(z)$ and the FIR-filter transfer function as F(z) then,

$$J_e(z) = [D(z)F(z)(1 - z^{-1}) \circledast J(z)] \tag{3.12}$$

Assume for simplicity, $F(z) = 1 + z^{-1} + z^{-2} + ... + z^{-L}$ Then,

$$J_e(z) = D(z)(1 - z^{-(L+1)}) \circledast J(z) \tag{3.13}$$

$$|J_e(z)| = J(z) \circledast \left[D(z) \cdot 2sin \left[\omega \left(\frac{L+1}{2} \right) \right] \right] \tag{3.14}$$

In the case of an NRZ DAC it is;

$$= J(z) \circledast \left[D(z) \cdot 2sin \left[\frac{\omega}{2} \right] \right] \tag{3.15}$$

From Eq.3.14 and Eq.3.15 it is clear that the sensitivity to jitter is much lesser in the case of an FIR-DAC. The sensitivity to jitter for these two DACs is shown in Fig.3.12. It is clear form the frequency response that the FIR-DAC has lower sensitivity to jitter at higher frequencies than an NRZ DAC. Eventhough FIR has a higher sensitivity at lower frequencies, it does not affect much because the data will not have much power at those frequencies. It should be noted that Eq.3.14 can also be intuitively derived with the aid of Fig.3.11. In this work, a ten tap differential

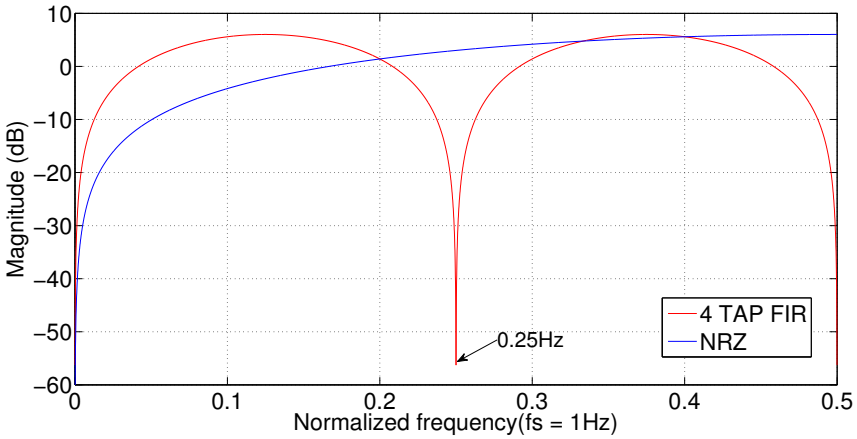

Figure 3.12: Jitter sensitivity comparison.

FIR-DAC is used. The structure of the ten tap FIR filter along with the DACs are shown in Fig.3.13. The DACs are implemented using just resistors. Therefore, this type of FIR-DAC can be called as resistive FIR-DAC due to its resistive output impedance. Another way to implement the DAC is through current-source

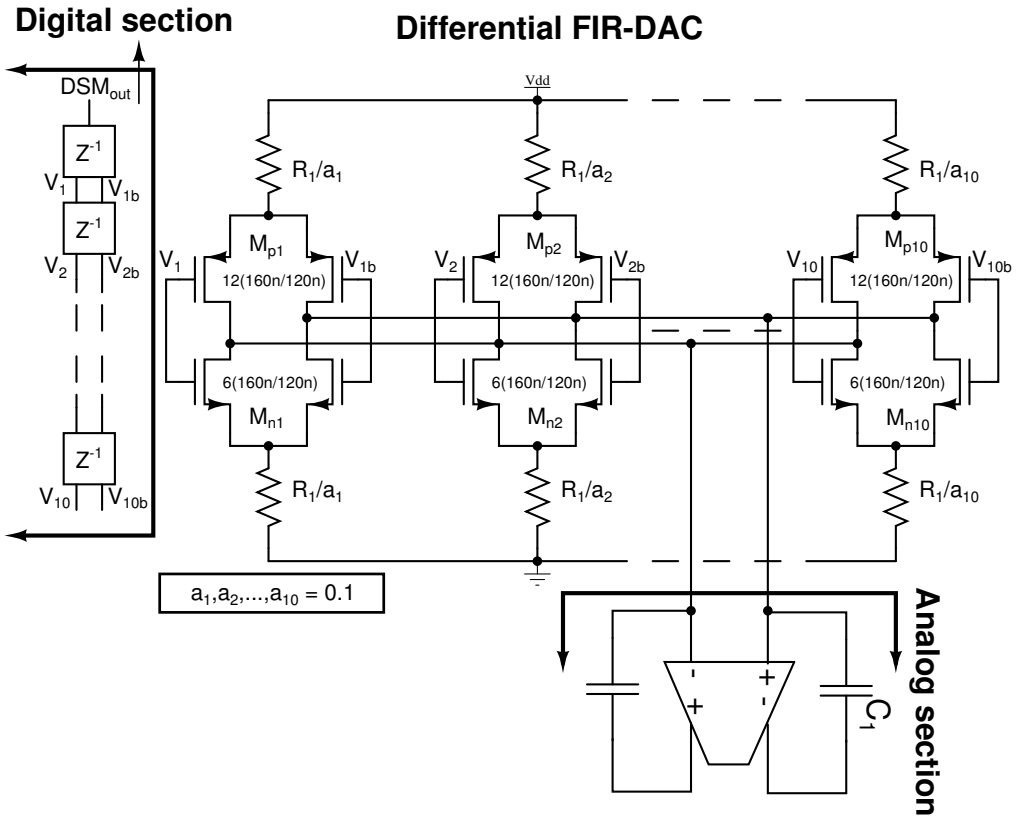

Figure 3.13: Schematic of a 10-tap differential FIR-DAC.

elements. These will be current-source FIR-DACs and will have ideally infinite output impedance. The advantage of input DACs being current-source type is that the input-referred noise power of the amplifier in the first integrator will only directly add at the output of the analog class-D system, instead of getting multiplied by the square of the inverse of the feedback factor of the closed loop system. Another advantage of current source DACs is its speed. However, the current-source DACs generate much higher noise when compared to an equivalent resistor. Since speed is not a constraint but noise is, a resistor FIR-DAC was chosen. R_{in} has been chosen to be 100 kΩ. Therefore, to design for a closed loop DC gain of unity, the parallel combination of all the ten individual resistors must also be 100 kΩ. Therefore, the individual resistances must be 1 MΩ each. Choosing higher number of taps will result in smaller coefficients and hence higher value of resistors. Large resistors have large amounts of distributed parasitics and large area and hence should be avoided.

The switches $M_{p1,...,10}$ and $M_{n1,...,10}$ connect the virtual grounds of the first integrator to either of the two resistors depending upon the data. This causes current(of value $\frac{V_{dd}}{2R_0}$) to be either sourced or sinked from or to the first integrator respectively. Since the FIR-DAC is outside the loop, its noise power adds directly at the output of the class-D amplifier. The main element that contributes to the noise is the resistor. Though the transistors $M_{p1,...,10}$ and $M_{n1,...,10}$ are resistively degenerated they can still contribute to flicker and thermal noise. Therefore, they were appropriately sized to ensure that the noise constraints are met and the only noise contributors are the resistors. Therefore, effectively, the noise power that the FIR-DAC adds at the output of the analog class-D amplifier will be equal to that contributed by the feedback resistors.

The schematic of the delay block is shown in Fig.3.14 A master slave approach

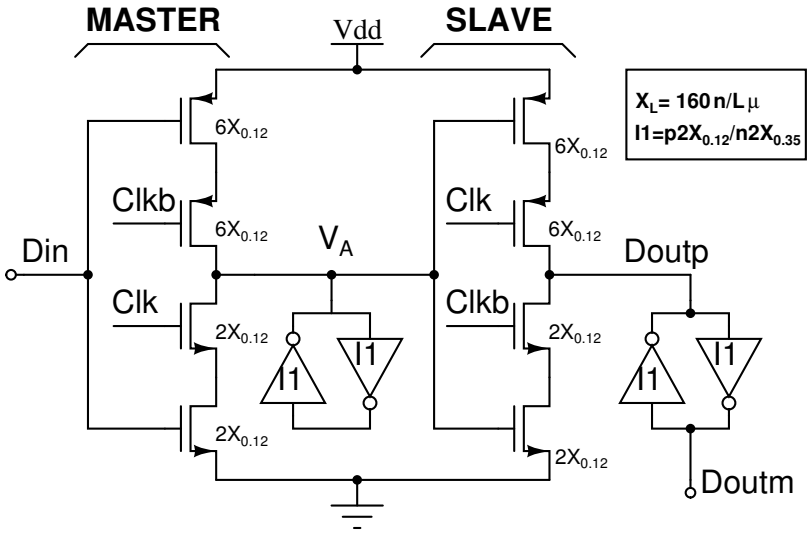

Figure 3.14: Schematic of unit delay block- D flip-flop.

has been employed. When clk is high Din is sampled on V_A. The cyclic back to back inverters acts as a latch and holds the value until the master forces its inputs. When clk becomes low, The slave outputs the sampled value on to another set of latches which holds it until the next slave cycle. Therefore, this operation gives a unit delay. The latches have to be sized such that they are weaker than the master and the slave.

3.3.2 Improving linearity of first integrator- the assisted opamp technique

By forming a closed-loop around the class-D power stage, the linearity requirements are now shifted to the loop-filter and specifically the first integrator. The integrator consist of a nonlinear transconductor-amplifier(TA). The output current of the transconductor, i_{out} is a nonlinear version of the input voltage $v_{g,diff}$. Therefore, when the TA supplies the input current and the feedback current, a nonlinear version of this output signal current gets developed as a voltage across the input terminals of the TA. This distorted voltage cause the input current also to be a distorted version of the input voltage. Within the signal bandwidth, most of this distorted current flows through the feedback resistor thereby causing the output voltage also to be a distorted version of the input voltage. The non-linearity of the first integrator affects the linearity of the overall system directly. Therefore efforts must be taken to make it as linear as possible. However, the nonlinearity of the second integrator is not that much of a problem within the signal band because it gets divided by the low frequency gain of the first integrator. Therefore, the blocks that contribute the most to signal distortion are, the amplifier of the first integrator, the feedback resistor and the input FIR-DAC. Nothing much could be done about the last two because they are dependant on the properties of the material used for the fabrication of the resistors. An elegant method to solve the linearity problem of integrators has been proposed in [11]. The idea is illustrated in Fig.3.15.

For simplicity, a single-ended version of the amplifier is used for explaining the idea. Assume that a DC negative feedback is established through a global feedback loop that is not shown. The feedback loop forces the negative input terminal of the transconductor to be virtual ground. Therefore, in the absence of assistant circuitry, a signal current of value $\frac{V_{in}}{R_{in}}$ flows through the integrating capacitor and hence into the transconductor. Now since the transconductor is nonlinear($f(v_d) =$

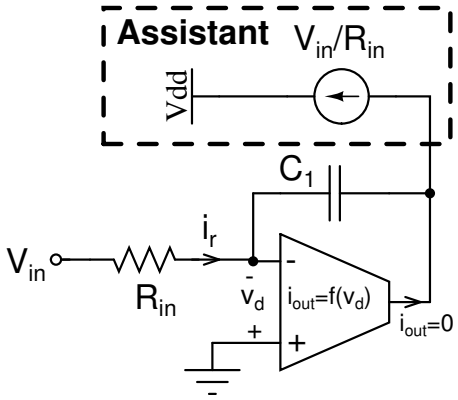

Figure 3.15: The assisted opamp technique.

i_{out}, where f is the nonlinear function), the input voltage will be $f^{-1}(i_{out})$. This implies that the input current is not just $\frac{V_{in}}{R_{in}}$ but $\frac{V_{in} - V_{dist}}{R_{in}}$ and hence is distorted. It should be realized that if we somehow force the signal current sourced/sinked by the TA to be zero, the voltage across the input terminals of the TA will also be zero. Therefore, the source of distortion-TA has been quietened and the signal at the output of the class-D amplifier will not be distorted. However, the above can be achieved only if we are able to force the output signal current of the TA to be exactly zero.

As shown in Fig.3.15, a current source circuit can be used to generate $\frac{V_{in}}{R_{in}}$ with the polarity shown there. Ideally, the signal current required by the TA now becomes zero and hence the virtual ground voltage will also be zero causing no signal distortion. However, in reality, these current source generating circuitry themselves will be non-linear and noisy and hence will not be able to generate the exact required current to make the output current of the TA zero. Anyway, this is not much of a problem because, any deviation of the current generated by the assistant from the required value, will be sourced/sinked by the TA. Therefore, if the mismatch between the current required by the TA and that generated by the assistant circuitry is minimized by proper design, the TA would need to source/sink only a very small amount of current that is proportional to the degree of mismatch.

Another way of thinking about this technique is that only the un-distorted compo-

nents of the current generated by the assistant circuitry flows into the integrating capacitor, whereas, all the distorted components is absorbed by the TA itself. By virtue of the high low-frequency transconductance of the TA, this non-linear component will have only a negligible contribution at the output of the class-D loop. The same arguments also hold for the noise generated by the assistant circuitry. Therefore, the design of assistant circuitry is not that critical.

Another advantage of using the assistance technique is that for the signal path, ideally, the poles of the main TA does not come into picture. This is because of the fact that now the signal current is supplied by the assistant circuitry and not by the main TA and thus the speed of the response depends on the speed of the assistant circuitry which can be designed to have a good bandwidth. Another benefit is that the non-zero low frequency integrator pole is shifted to DC. On the whole, the assistant technique helps the practical integrator approach an ideal one. It should be noted that since this is a cancellation-based technique, the accuracy will be limited by systematic and random errors. Another point to note is that this technique is based on the principle of feedforwarding and hence will not cause stability issues. This technique was adopted in this work as shown in Fig.3.16

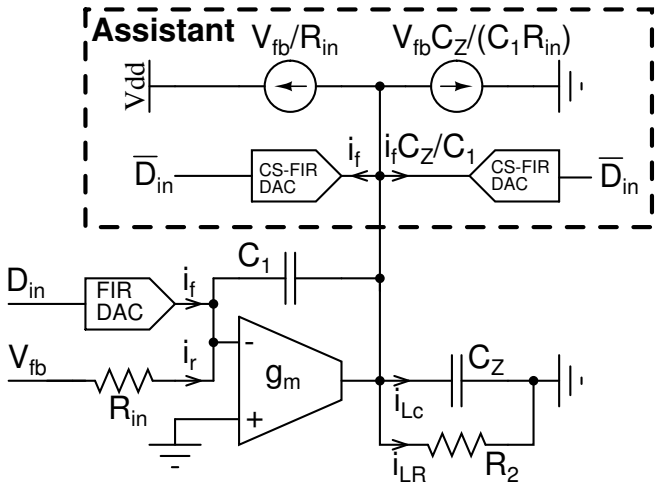

Figure 3.16: Implementation of the assisted opamp technique.

With reference to Fig.3.3, the current that the transconductor-amplifier(TA) needs to source/sink is $i_f + \frac{V_{fb}}{R_{in}} + i_f\frac{C_Z}{C_1} + \frac{V_{fb}}{R_{in}}\frac{C_Z}{C_1}$. Here, V_{fb} is the output of the class-D

amplifier. As shown in Fig.3.16, one current source circuit can be used to generate $i_f\left[1+\frac{C_Z}{C_1}\right]$ and another to generate $\frac{V_{fb}}{R_{in}}\left[1+\frac{C_Z}{C_1}\right]$. A point to note here is that even the load currents are being made to be supplied by the assistant circuitry, thereby making the amplifier to source/sink virtually zero signal current. The signal current component i_{LR} has not been assisted for, as the assistant circuitry required would itself be complicated. However, since i_{LR} itself is very less, it can be supplied by the TA without affecting the linearity of the system.

Fig.3.17 shows the assistant circuit employed for generating $\frac{V_{fb}}{R_{in}}\left[1+\frac{C_Z}{C_1}\right]$. Since the fedback signal V_{fb} is either ground or supply, the current waveform through R_{in} switches between $-\frac{V_{dd}}{2R_{in}}$ and $\frac{V_{dd}}{2R_{in}}$ depending on the data. Therefore, a differential circuit with two current sources which is switched depending upon V_{fb} is adopted as shown in Fig.3.17. i_{outp} and i_{outm} flow differentially into the output terminals of the first integrator.

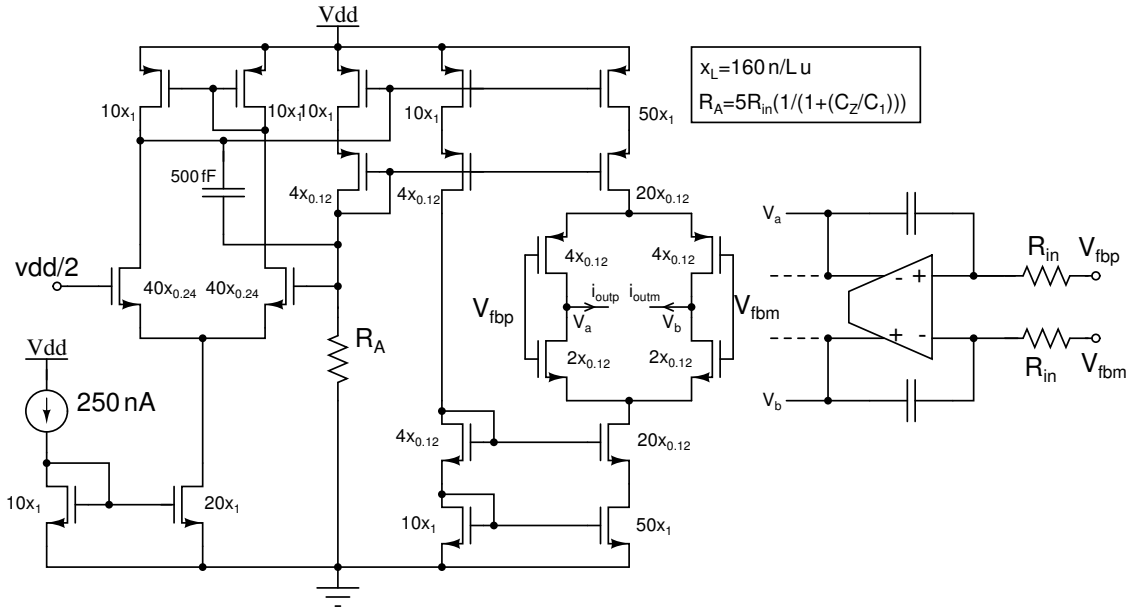

Figure 3.17: Assistant for the feedback current.

The schematic of the assistant that is used to generate $i_f\left[1+\frac{C_Z}{C_1}\right]$ is shown in Fig.3.18. A structure similar to the input resistive FIR-DAC cannot be used as an assistant because of its low output impedance. However, the same architecture should be used except that now the resistors need to be replaced by current sources.

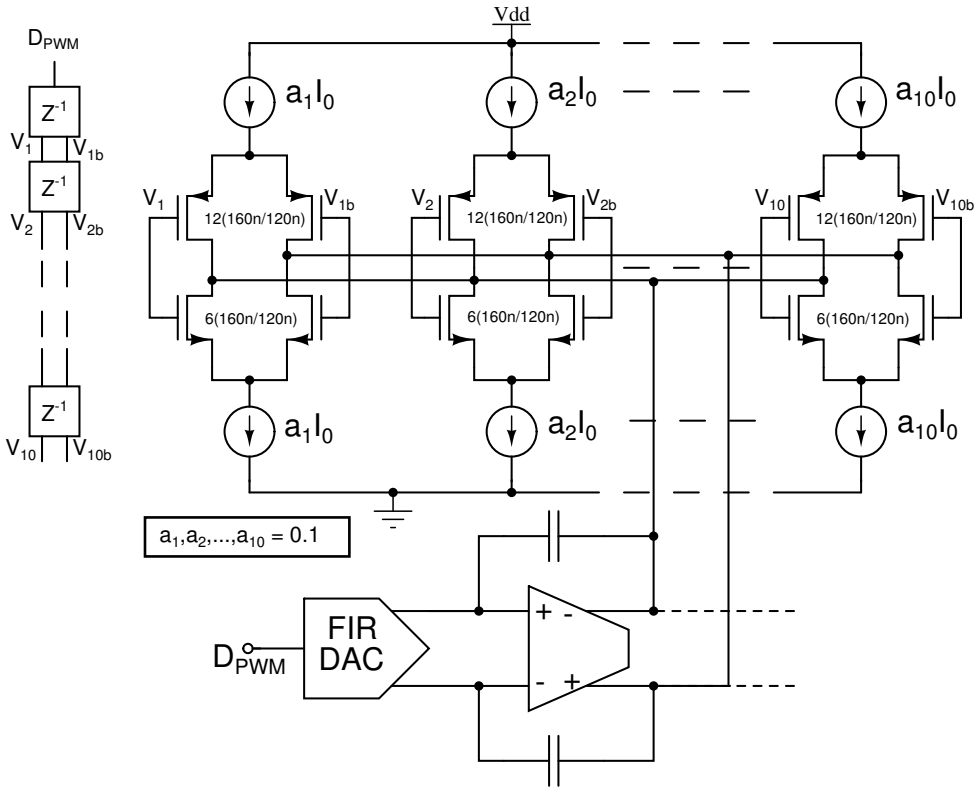

Figure 3.18: Assistant for the input FIR-DAC current.

These current sources have a similar cascode structure as shown in Fig.3.17 and the currents are generated by using an amplifier structure that is similar to the one shown in Fig.3.17.

3.3.3 Transconductor-Amplifier(TA) design

The schematic employed for the amplifier of the first integrator is shown in Fig.3.19. Since this TA has an assistant to provide the current required by the inputs, the driving stage need not be biased for full signal-current swing. However, this does not mean that the output stage of the TA can have zero current because, the noise current and distortion components generated by the assistant circuitry and the error current due to mismatches between assistant and main TA have to be suppressed by the effective transconductance of this TA. Therefore in practice, a finite amount of bias current is allotted in the output stage. This is a two stage amplifier with feedforward compensation. The output of the amplifier is the sum

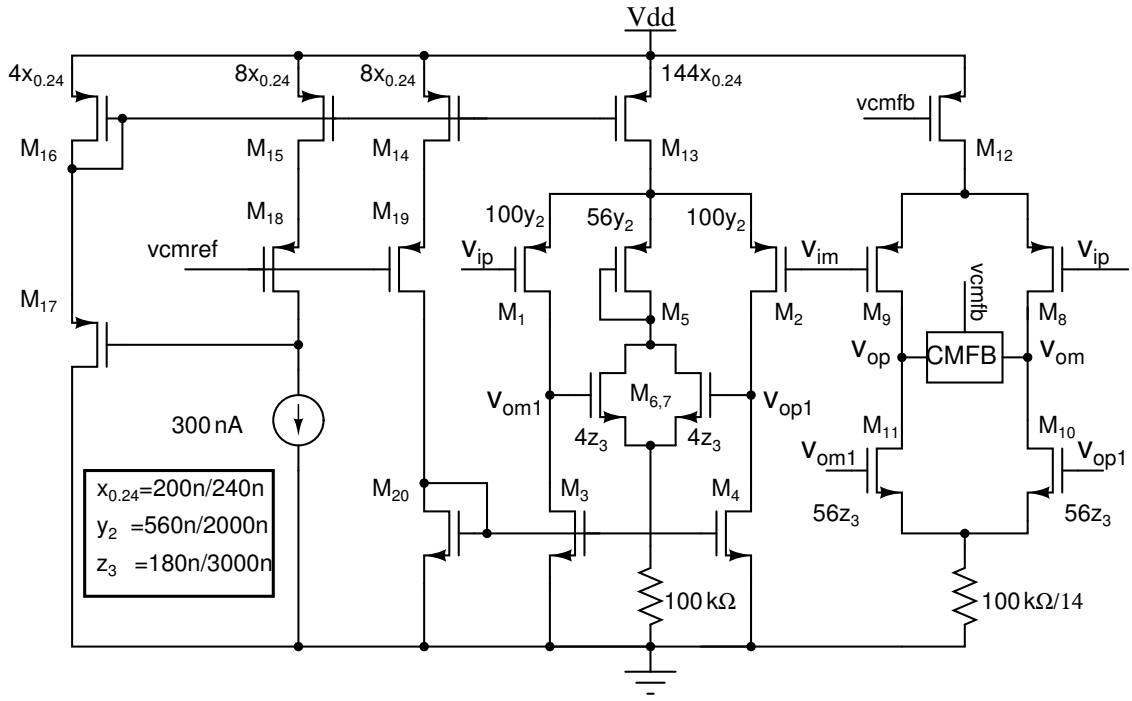

Figure 3.19: Schematic of TA of first integrator.

of a second order path($M_{1,2} - M_{3,4} - M_{10,11}$) and a first order fast path($M_{8,9}$). The amplifier is designed such that the fast path starts dominating the second order path at a frequency well before the UGB of the second order path as shown in Fig.3.20. In other words this is like adding a zero to the loop and counteracting the effect of a pole. Therefore, the second order path can have a high low frequency gain while the first order path has a high bandwidth. Fig.3.20 also shows the expected frequency response of a feedforward amplifier.

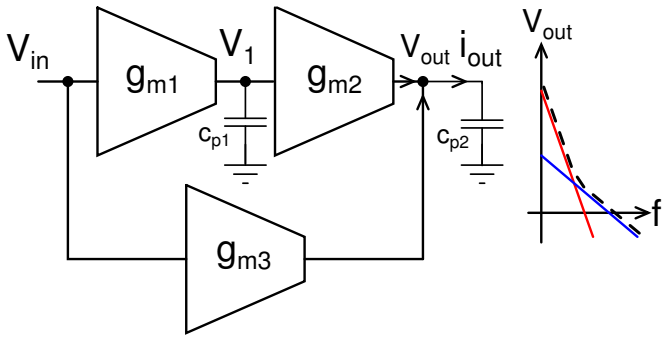

Figure 3.20: Principle of feedforward compensation.

The input-referred noise power of $M_{1,2}$ is multiplied four times when referred at the output of the class-D amplifier. Therefore, PMOS input pair is chosen to reduce

the flicker noise contribution. $M_{6,7}$ forms the averaging part of the first stage CMFB loop. The 100 kΩ resistor is for level shifting so that $M_{3,4}$ does not enter triode across PVT. M_5 is used to establish a perfect(upto second order) current mirroring between the first stage CMFB and the second stage of the amplifier. $M_{8,9}$ forms the fast path or the first order path. Their transconductance determines the UGB of the amplifier and hence is chosen to be relatively higher than that of other transistors.

The CMFB loop of the second stage of the amplifier is a conventional differential input and single-ended output, Miller-compensated amplifier. This has a similar structure as that of the first stage of the amplifier used in Fig.3.17. The sizes of the CMFB amplifier are chosen such that there is no systematic error in current mirroring to the second stage of the differential pair, which is also the second stage of the CMFB loop. The amplifier in the CMFB loop is shown in Fig.3.21

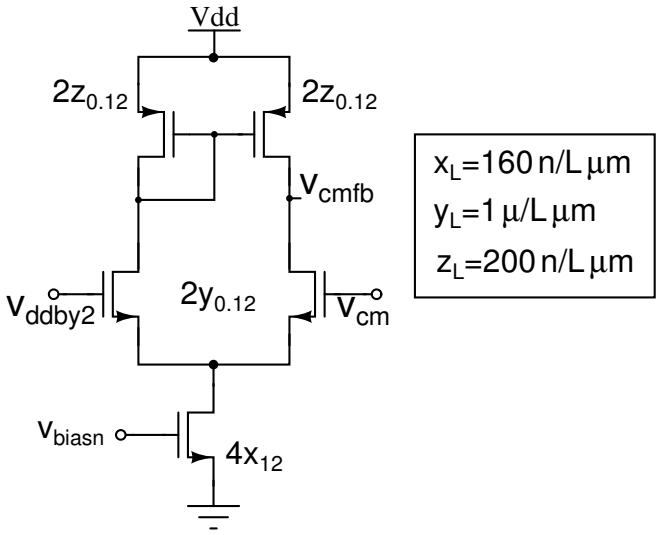

Figure 3.21: Schematic of the CMFB amplifier.

The frequency response of the designed amplifier with a 1 pF load capacitance is shown in Fig.3.22.

The TA used in the second integrator has an NMOS input pair. This is also feed-forward compensated and has similar first stage and second stage CMFB circuits. It's schematic is shown in Fig.3.23. The biasing and the CMFB are similar to

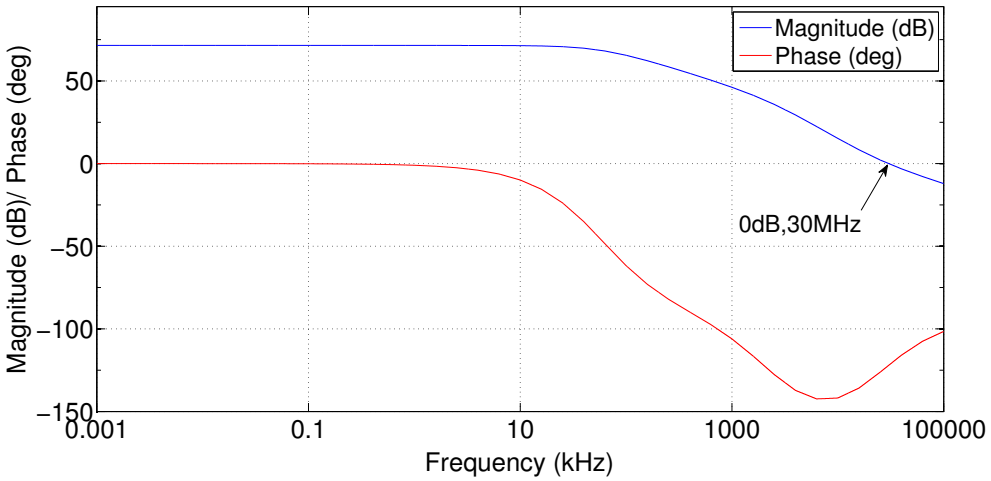

Figure 3.22: Magnitude and phase response of the transconductor-amplifier.

that of the first TA. An assistant was used for providing the square-pulse current which is used for triangle wave generation.

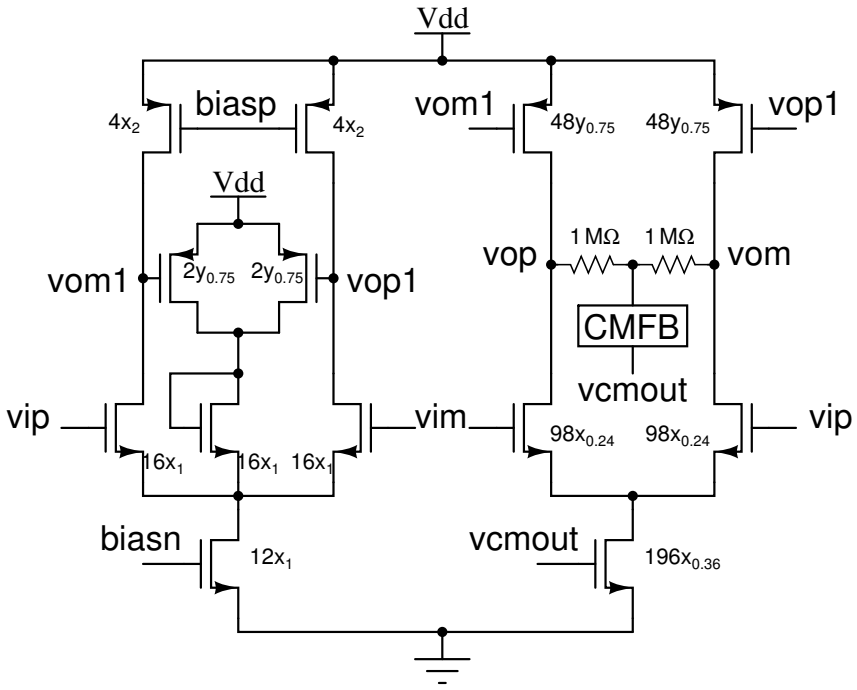

Figure 3.23: Schematic of TA of second integrator.

3.4 Comparator

This is a design which incorporates dead-time generation circuitry within the comparator itself. A comparator compares the voltages across its input terminals and drives its outputs to either supply or ground depending upon which of the two inputs are higher. Another way of thinking at it is that, it compares the differential signal to a virtual ground and takes a decision depending on the polarity. The comparison process has to be performed all the time continuously and hence a continuous-time architecture has to be adopted. A comparator that is to be employed for a class-D amplifier, must have fast rise and fall times, because finite rise and fall times causes the PWM to become non-linear. However, in the case of closed loop class-D systems such as the one employed in this work, the non-linearity is suppressed by the loop by appropriately adjusting the pulse widths. Another point is that finite rise and fall times limit the maximum/minimum duty cycles and hence the maximum output power deliverable. Therefore it is always better to keep rise and fall times much lower than the switching period.

An amplifier can by itself act as a comparator if it is operated in open loop. For the comparator to resolve even small differences between its input terminals, it has to have a very high gain. The minimum input difference required by a comparator employing an amplifier of gain A is $\frac{V_{out}}{A}$, where V_{out} is usually V_{dd}. Therefore, a second order amplifier without compensation was adopted in this work to achieve high gain. It is to be noted that cascading gain stages will have a relatively faster rise and fall times than cascoding. This is because cascoding will push the -3 dB pole to lower frequencies by a factor of the cascode gain, whereas, cascading will reduce the effective pole frequency only by a relatively smaller amount. However, it has to be ensured that the additional poles added by cascading does not cause stability problems for the class-D loop. The architecture adopted for the comparator is shown in Fig.3.24.

In addition to the gain stage, the comparator has a high-swing output stage. The

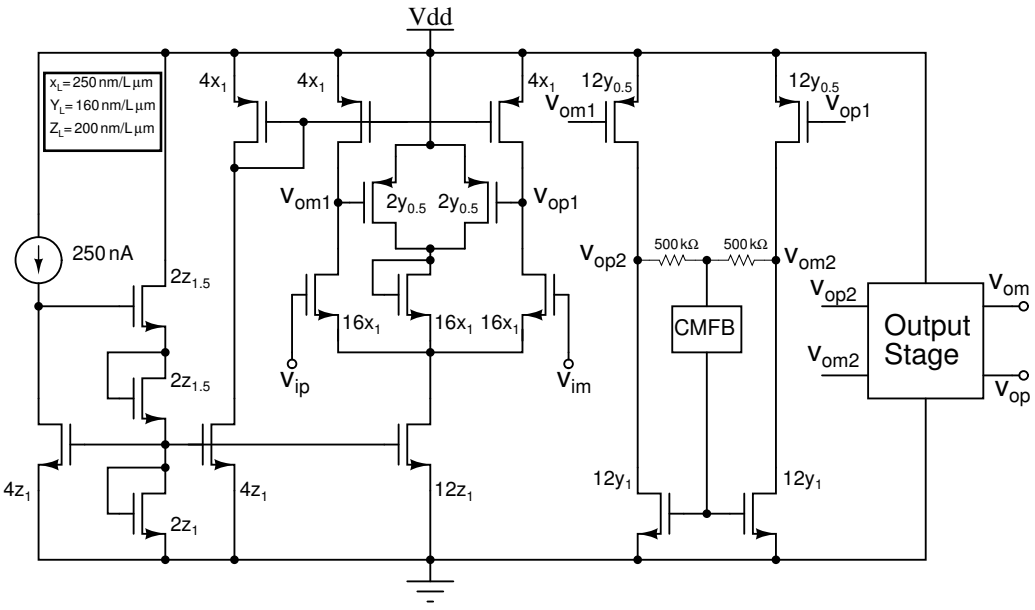

Figure 3.24: Schematic of comparator.

output stage of the comparator is designed to allow rail to rail output swings. This structure is nothing but an inverter as shown in Fig.3.25. The details of dt_1 and dt_2 are discussed in the next subsection.

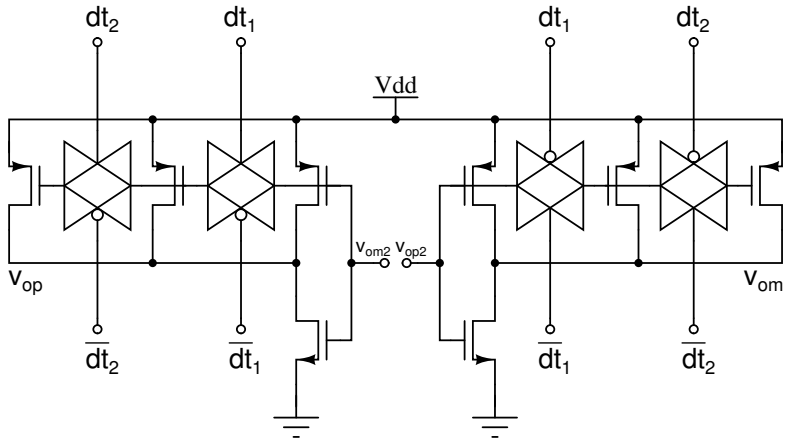

Figure 3.25: Schematic of output stage.

3.4.1 Comparator as a dead-time generator

Non-overlapping pulses are required to drive the H-Bridge in order to avoid shorting the supply to ground through a low impedance path. The typical waveforms needed to drive a H-Bridge driver is shown in Fig.3.26.

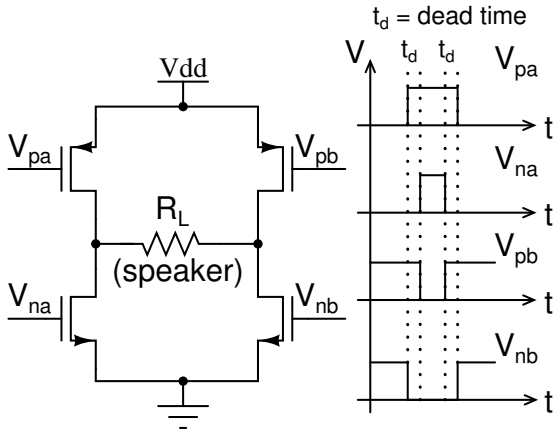

Figure 3.26: H-Bridge with non-overlapping data inputs.

To understand how the comparator circuitry generates the dead time t_d, consider Fig.3.27. For simplicity, assume the input signal to the class-D loop is a DC of value $\frac{V_{dd}}{2}$. Then, the waveform at the output of the second integrator will have only the triangular carrier waveform as shown in Fig.3.27. When V_{im} is greater

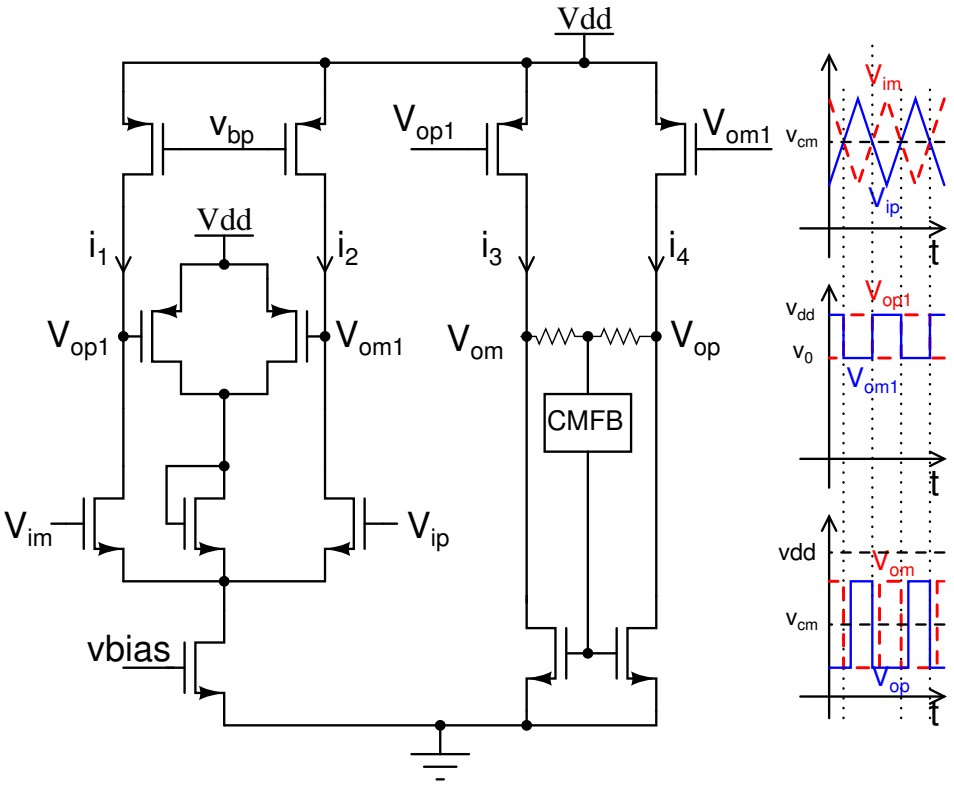

Figure 3.27: Mechanism of dead-time generation.

than V_{ip}, the current i_2 almost reduces to zero. This would tend to force V_{om1} to V_{dd}. Now because of the first stage CMFB transistor, V_{op1} does not go down

all the way to zero but settles to a value V_0 which will be somewhere between V_{dd} and $\frac{V_{dd}}{2}$. Let us assume the transition time from V_0 to V_{dd} is equal to that from V_{dd} to V_0 (however in reality, transistors take longer time to switch off due to their on-resistance increasing with decrease in current). This signal is applied to the second stage input pair. Here, V_{om} drops from a higher voltage to a lower voltage much more quickly than V_{op} rises from a lower voltage to a higher voltage. This is because V_{op1} has an initial voltage of V_0 where the transistor is completely switched on and has a good initial drive. However for V_{om1}, the initial voltage is V_{dd} and hence has a zero initial drive. This causes a slower transition. During the opposite transitions, the situation is reversed. V_{op} falls from a higher voltage to a lower voltage faster than V_{om} rises from a lower voltage to a higher voltage. This phenomenon results in a dead-time being developed as illustrated in Fig.3.27.

Since the swings at the output of the second stage does not go all the way from V_{dd} to ground or vice-versa, a high gain output stage is used as shown in Fig.3.25. Since the dead time generated due to the above phenomenon will vary with process, it was tuned out using the control bits dt_1 and dt_2. The idea is to change the drive strength of the inverters so that the rise time can be increased or decreased depending on the corner the chip gets fabricated. A separate tuning was not provided for the NMOS as it was verified from simulations that it was not required. The change in dead-time for two extreme control bits is shown in Fig.3.28. From Fig.3.28 it is clear that when the control bits [dt1 dt2] are changed from 00 to 11, the dead time collapses. Therefore, if the chip comes in a corner where the dead time is too high, [dt1 dt2] can be set to 11. If its too low, they can be set to 00 and for intermediate values, 01 and 10 setting can be used. From the same figure, the rise time/fall time is noted to be about 20 nSec. This is sufficient as it is just about one percent of the switching period of 1.5625 μSec.

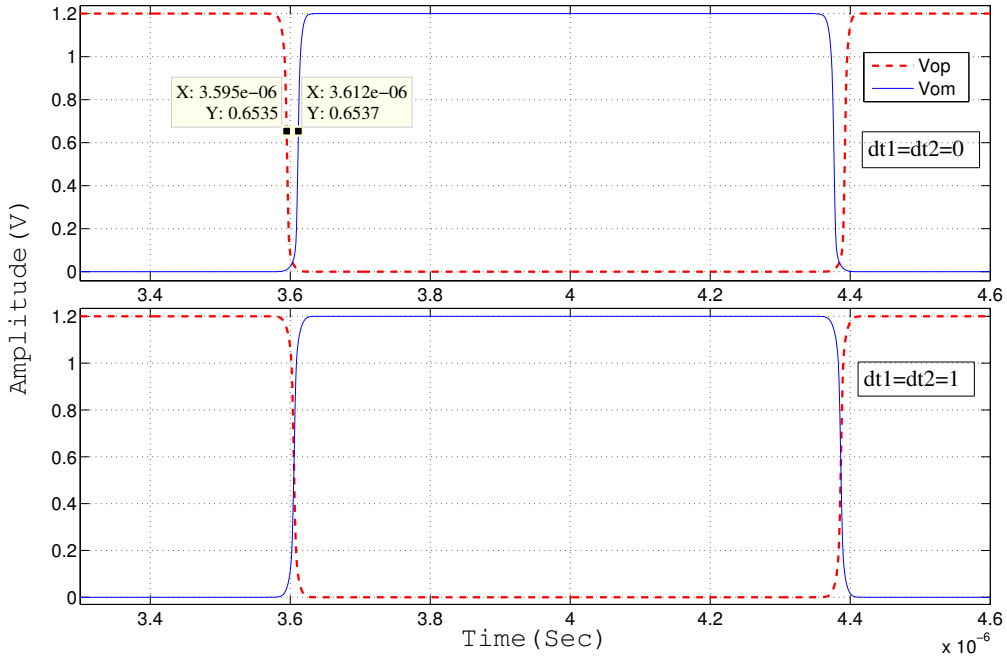

Figure 3.28: Tuning the dead-time.

3.5 Buffer and H-Bridge driver

This is the actual driver stage. The switches has to have a sufficiently low impedance in order to achieve a high efficiency. According to the required specifications, the differential output impedance of the switches were chosen to be 20 Ω. Eventhough this is a relatively high value of switch resistance, it is acceptable as generally hearing aid speakers will have a high output impedance in the order of 200-300 Ω. Since the differential on-resistance of the bridge is 20 Ω, each switch should have an on-resistance of 10 Ω. This would imply that large transistors have to be used. The H-Bridge along with the switch sizes are shown in Fig.3.29. Due to the large sizes of the switches in the H-Bridge, the output stage of the comparator will not be able to drive the H-Bridge. Therefore, a buffer circuitry is required. This is shown in Fig.3.30 The plots of waveforms are shown in Fig.3.31.

A control bit named mode is used in the H-Bridge stage. When mode is 1, the differential output impedance will be set to 20 Ω and when 0, will be set to 40 Ω. This arrangement of the buffers gives tight matching about both vertical and

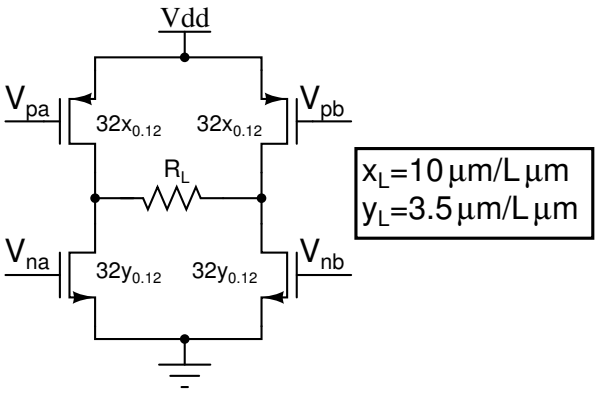

Figure 3.29: H-Bridge driver.

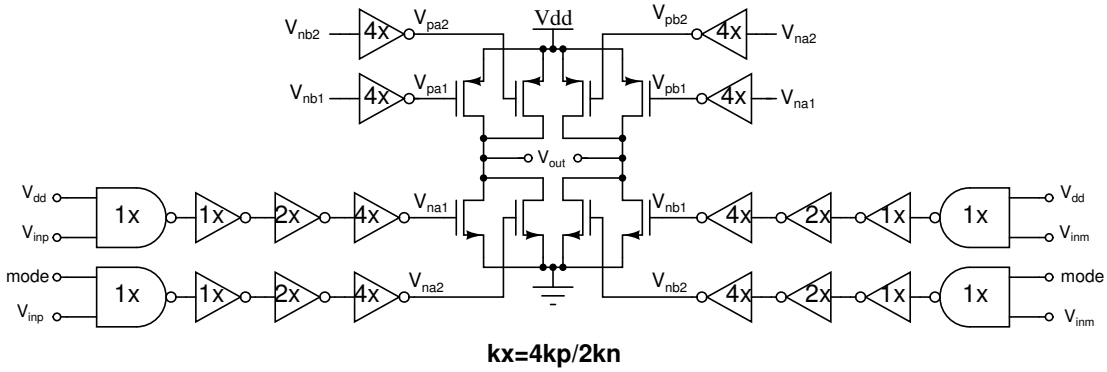

Figure 3.30: Driving the H-Bridge.

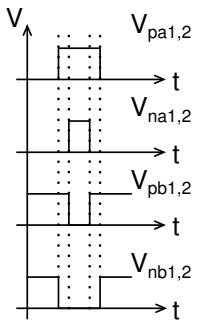

Figure 3.31: The timings for meeting non-overlap requirements.

horizontal cross-sections.

3.6 Performance summary

The PWM output of the H-Bridge will have very high frequency components(theoretically infinite). Therefore, the output should be filtered first. A second order Butterworth low pass filter has been used as the LPF. The frequency response of the filter is shown in Fig.3.32. Fig.3.33 shows the combined performance of the analog

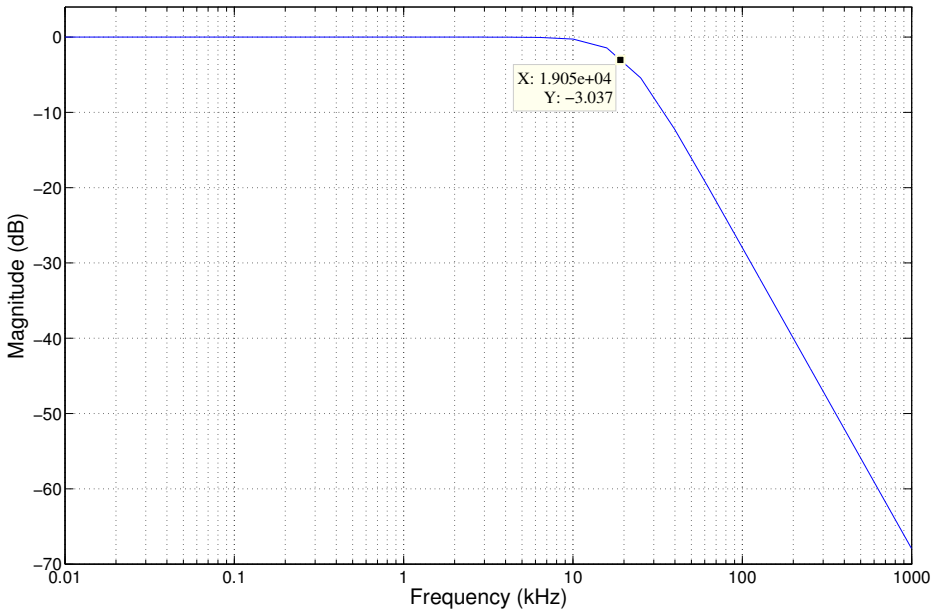

Figure 3.32: Frequency response of second order LC low pass filter.

and digital section of the class-D amplifier across various corners. The input is a single tone sine wave at 625 Hz and has an amplitude 0.95 times the Maximum Stable Amplitude(MSA).

The performance achieved by this design has been compared with those achieved by other reported designs and is tabulated in Table 3.2. The comparison is done based on the Figure Of Merit(FOM) of the designs. FOM=$DR + 10log\left(\frac{BW}{\left(\frac{P}{V_{dd}^2}\right)}\right)$.

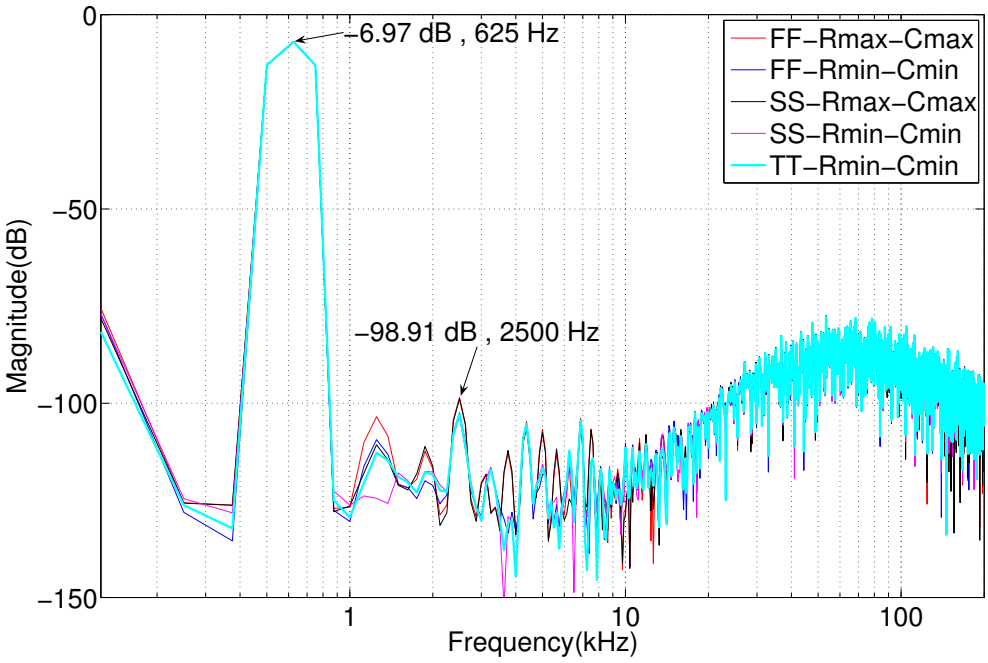

Figure 3.33: PSD at the output of Class-D loop.

Table 3.2: Performance comparison with reported designs

Design	Bandwidth	THD+N(dB)	Process(μm)/Supply	Power	FOM
[12]	4 kHz	-66	0.35/1.1 V	60 μW	145
[13]	22 kHz	-96	0.35/5.0 V	150 mW	162
[14]	8 kHz	-74	0.35/1.1 V	31 μW	159
[15]	20 kHz	-65	0.18/1.0 V	35 μW	152
[16]	20 kHz	-74	0.18/3.0 V	7.7 mW	147
This work	10 kHz	-89	0.13/1.2 V	117 μW	170

CHAPTER 4

Miscellaneous Blocks and Layout

This chapter deals with the blocks that are associated with the design of class-D amplifier but are not fundamental to their design.

4.1 Serial Peripheral Interface- SPI

The input to the class-D system is a 16-bit digital signal. If we were to bring the input parallely into the chip, it would require 16 pins. This means lot of area and moreover, these pins can be allotted for other inputs/outputs for probing. Therefore, instead of sending in the 16-bit digital word parallely it is sent into the chip serially. Therefore now one pin is enough to send the data into the chip. However, the start and the end of the word must be known to the receiver. This is accomplished by the SPI protocol as shown in Fig.4.1. According to this

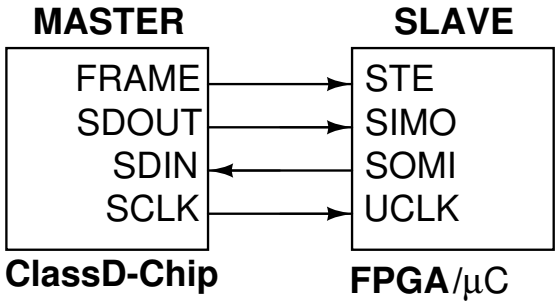

Figure 4.1: SPI protocol- Master Slave communication.

protocol, a master device and a slave device has to be assigned. The master device is the one which sends out the serial data and the synchronization signals. Therefore, the class-D amplifier chip is the master. The slave is the receiver which receives the data and the synchronization signals and decodes the message. The FPGA board is the slave. For synchronization purposes, the master sends out two

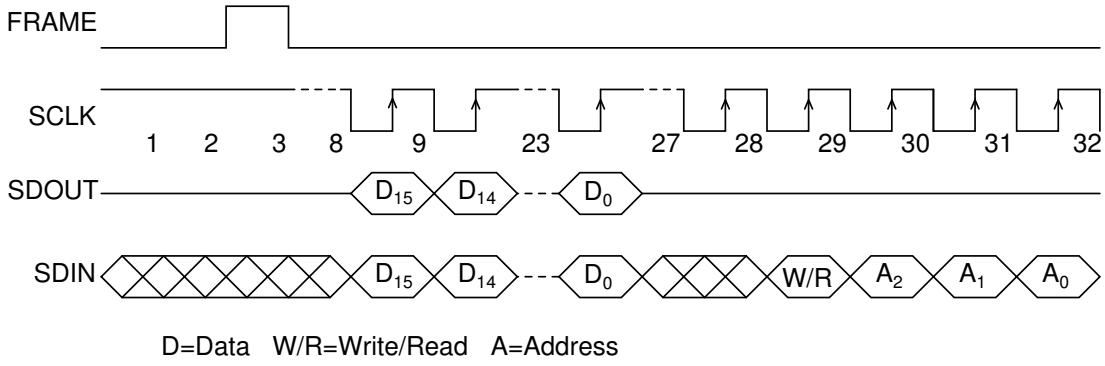

Figure 4.2: Address frame.

signals- FRAME and SCLK as shown in Fig.4.2. The FRAME signal indicates the beginning of a new frame or a new word. The SCLK deals with proper transmission and reception of data. At every rising edge of SCLK, the data sent by the master is read(SDOUT) by the slave and at every falling edge of SCLK, any data to be sent to the master is sent(SDIN) by the slave.

More complex masters will have many registers that needs to be programmed. This programming of registers is done through SDIN/SOMI. In order to program a register, first the address of the register has to be entered and then the control word has to be programed. This can be done over two frame cycles. In the first frame cycle, the timing diagram looks as in Fig.4.2. The three LSBs corresponds to the address of the register. The fourth bit is the write/read bit. If a control word has to be programmed, this bit is set to one. If this bit is set to one, then in the next frame cycle, the eight LSBs of SDIN would correspond to the control word to be programmed as shown in Fig.4.3. Therefore the programming of one control

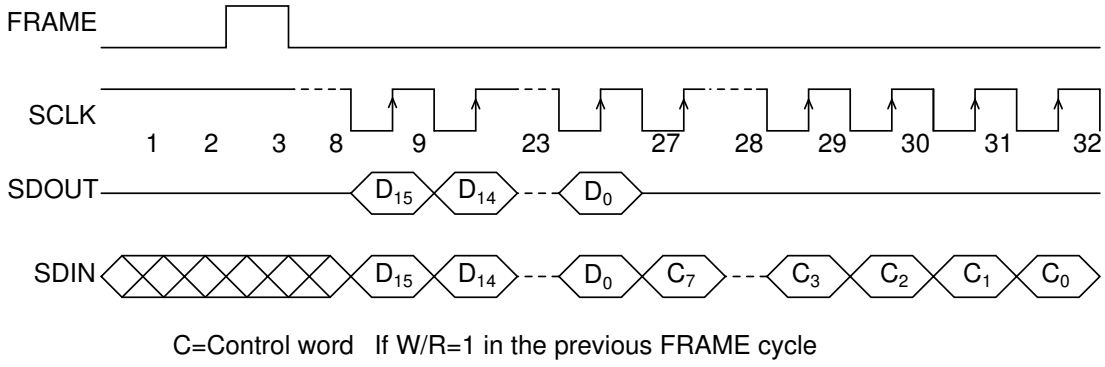

Figure 4.3: Control word frame.

word can be accomplished in two FRAME cycles. If in the current FRAME cycle the W/R bit is set to zero, then in the next FRAME cycle, the last 8 bits of the SDIN are don't cares and the last 8 bits of SDOUT can have some information from the master, say, the temperature of the chip or the gain setting of any internal amplifier. This is shown in Fig.4.4.

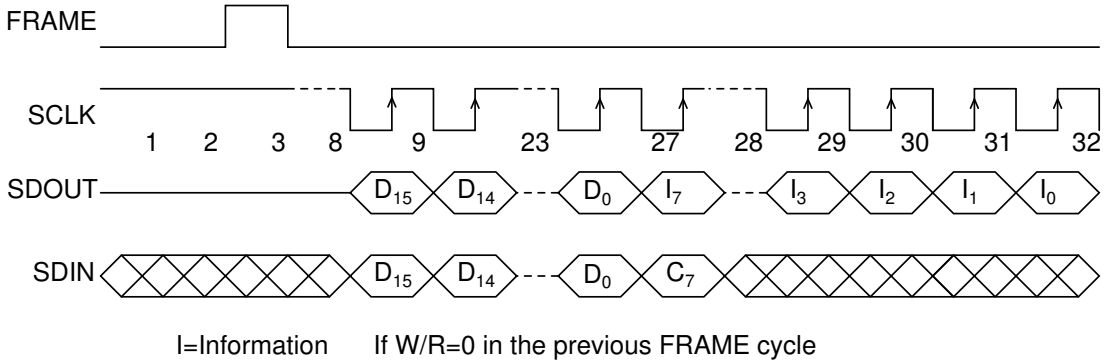

Figure 4.4: Read frame.

By setting all the address bits to zero denotes that no control action needs to be taken in the next cycle. Therefore, once the programming is done, the address bits are always kept zero.

4.2 Low Battery Monitor (LBM)

This block has been designed to indicate when the supply voltage decreases below a particular voltage. This chip is designed to be operated from a battery supply and we can expect the battery voltage to drop with time. Since operating the system at low supply voltages will cause the system to malfunction and may produce erroneous sounds. This will cause discomfort to the user. Therefore, the function of LBM is to indicate low battery.

Since the hearing aid contains digital circuits and DSP, there would be spiky currents of large magnitude drawn from the supply. The series inductance of the supply will cause the supply within the chip to spike down and can cause the LBM to give wrong indications during the spikes. Therefore its design should

take into account the above factors. Taking reference from a TI's IC bearing the model number AIC111, only if the internal supply voltage is below 1.05 V(The chip operates at 1.2 V) for more than 44 μSec, the LBM should indicate that the battery is low. The design of the LBM is shown in Fig.4.5. The PMOS divider is

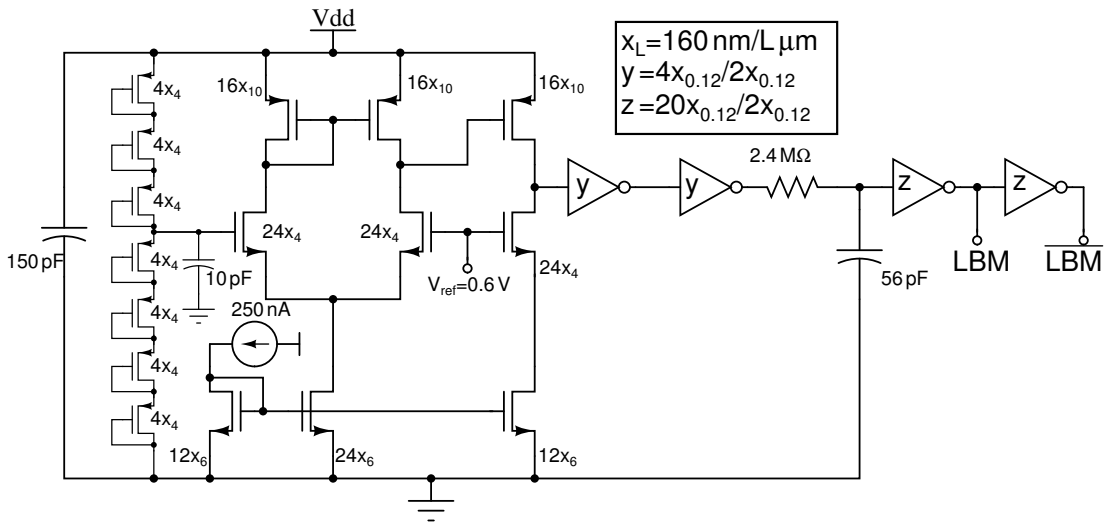

Figure 4.5: Low battery monitor.

used to scale down the supply voltage. This scaled down voltage can be compared with a reference voltage that is independent of supply. This reference voltage is derived from a Bandgap circuit. The 10 pF capacitor along with the potential divider forms a filter to reject the high frequency spikes from the supply. The cut-off of this filter is about 3 kHz. This filtered waveform is compared with 0.6 V and drives the output stage(output of y-sized inverters) of the comparator to either supply or ground. This is subjected to another stage of filtering whose cut-off is at 1.2 kHz. These cut-off frequencies were chosen from simulations and was found to meet the requirements across corners and temperature. A typical low battery scenario and the response of the LBM circuit is shown in Fig.4.6 and Fig.4.7.

From Fig.4.6 it is clear that if the supply droops below 1.05 V and stays there for a long time, the output of the LBM goes low indicating low battery. Fig.4.7 shows that if the supply droops below 1.05 V only for a small duration, the output of the LBM does not drop to zero. This is the required functionality that the LBM was designed for.

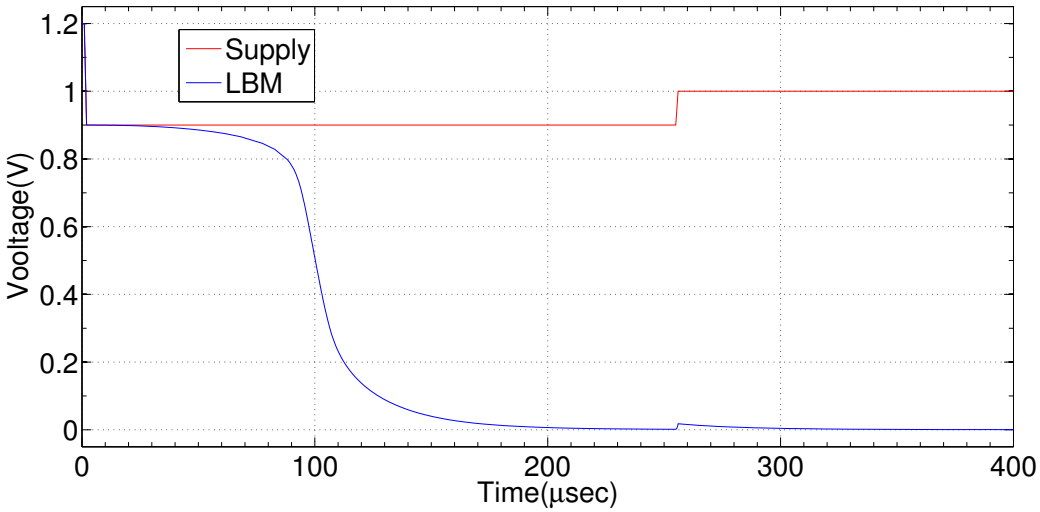

Figure 4.6: Low-battery indication.

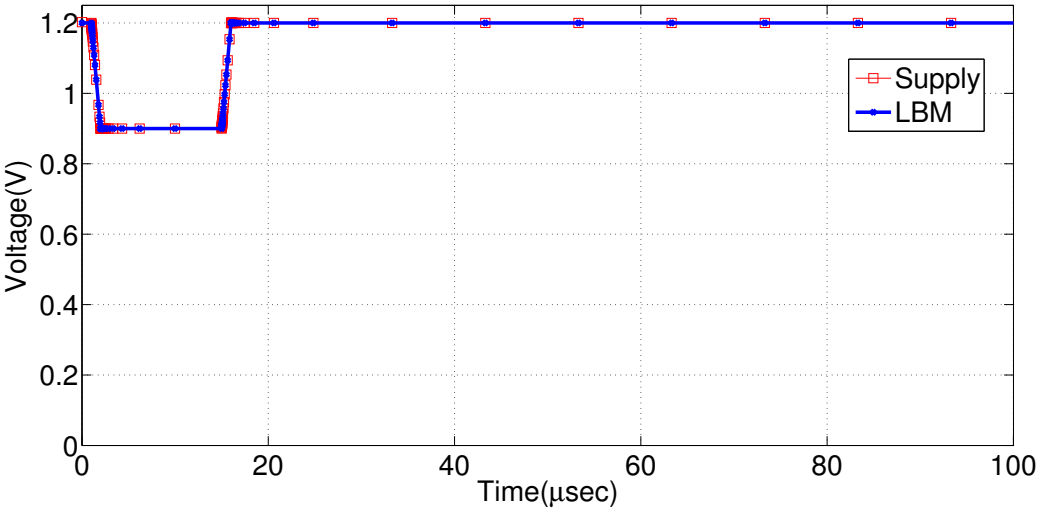

Figure 4.7: Normal operation.

4.3 Bandgap Voltage Reference

The bandgap voltage reference circuit was designed to generate a V_{ref} of 0.6 V which is required by the LBM. Since the output voltage of the bandgap is less than the conventional 1.2 V, a low-voltage architecture has to be adopted[17]. The schematic is shown in Fig.4.8. The basic idea is to create a current that is propor-

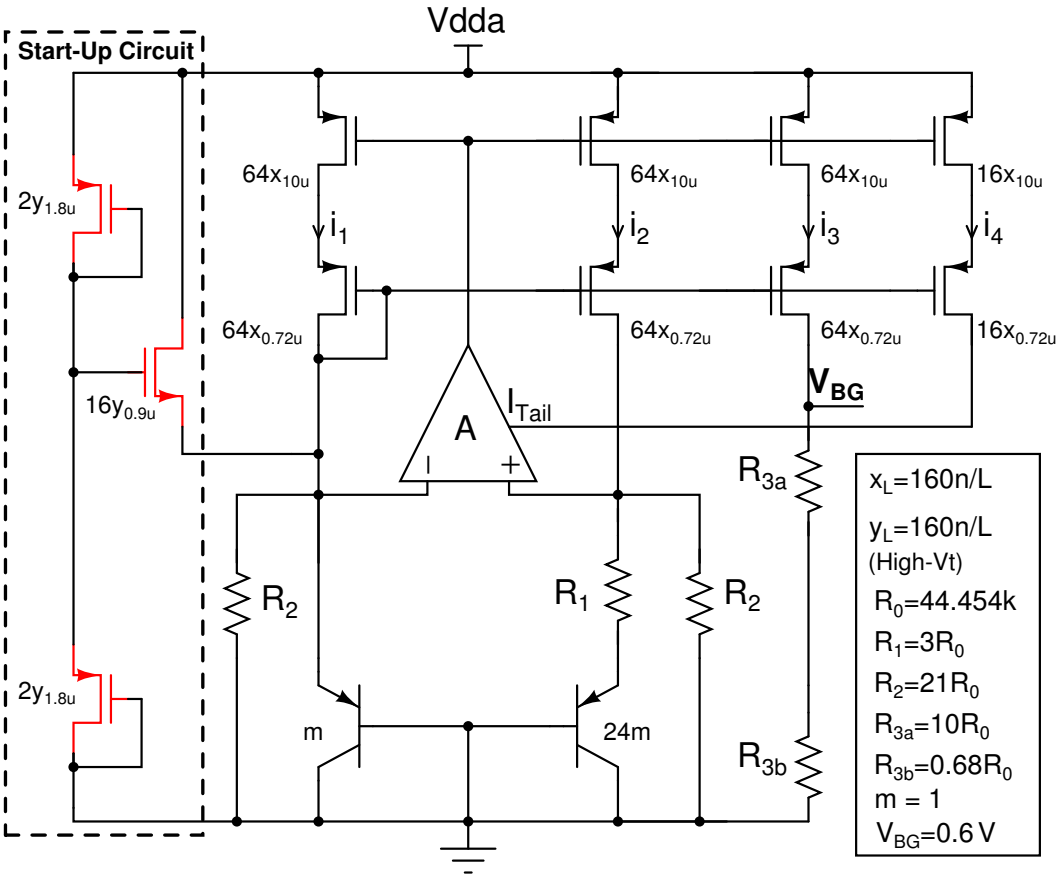

Figure 4.8: Fractional Bandgap voltage reference.

tional to temperature (PTAT) and another current that is inversely proportional to temperature (CTAT) and weight and add them such that the temperature dependence is nullified in the resultant current. PTAT current can be generated by the loop formed by the two BJTs, the amplifier and resistor R_1, as shown in Fig.4.8. The amplifier forces the voltage across its inputs to be zero and the cascode mirroring causes i_1 to equal i_2. Therefore, the voltage across R_1 is $V_{BE1} - V_{BE2}$ which equals $V_T ln(N)$. In this case N(the ratio of emitter areas of the two BJTs) was chosen to be 24. Choosing N as 24 allows us to place 24 fingers of the bigger BJT

in a common centroid fashion around the single finger BJT. This ensures almost perfect area scaling. Now the current through R_1 is $\frac{V_T ln(24)}{R_1}$ which is PTAT. It is well known that upto a first order, the temperature dependence of the diode voltage is given as [17];

$$V_{BE}(T) = V_{BG} - (V_{BG} - V_{BE0})\frac{T}{T_0}. \tag{4.1}$$

where, V_{BG} is the silicon bandgap voltage extrapolated to 0^0 K ($\approx$1.206 V), T_0 is the reference temperature and V_{BE0} is the base-emitter voltage at T_0. The derivative of the above equation with respect to temperature(T) clearly shows that the diode voltage drop has a negative dependence on temperature. Practically, this is about -2 mV/^{0}C.

Therefore;

$$i_2 = \frac{V_T ln(24)}{R_1} + \frac{V_{BE1}}{R_2} \tag{4.2}$$

This is the sum of PTAT and CTAT currents. On differentiating the above equation with respect to temperature and equating to zero gives the required relation as;

$$\frac{R_2 ln(24)}{R_1} = 22 \tag{4.3}$$

On choosing $R_!$ and R_2 such that the above constraint is satisfied, a temperature independent current i_2 is got. This current is mirrored into another resistor R_3 in order to get the desired voltage. Therefore;

$$V_{ref} = \frac{R_3 V_T ln(24)}{R_1} + \frac{R_3 V_{BE1}}{R_2} \tag{4.4}$$

However, the assumption made in the above derivation is that there are no sys-

tematic or random offsets associated with the amplifier. This is not true. A Systematic offset is created in the amplifier if its output stage current density is not equal to the current density of the PMOS transistors it biases and if the amplifier has a finite gain(which is always the case). This offset can vary with process and temperature. Therefore, a method has been proposed as shown in Fig.4.8 and Fig.4.9.

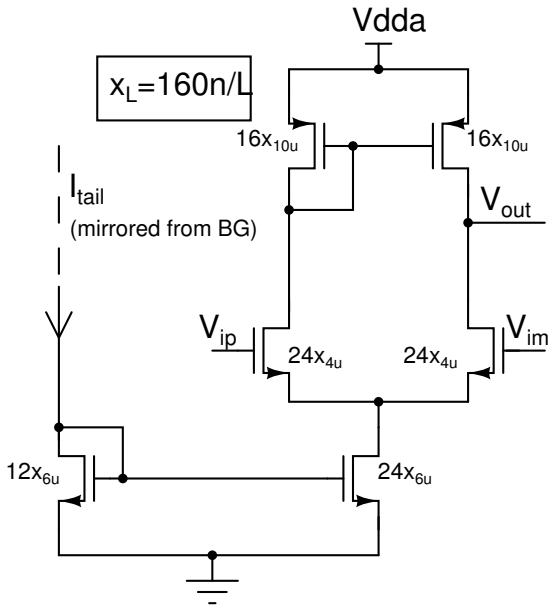

Figure 4.9: Amplifier used in bandgap.

In this method, the master current of the amplifier is derived from the output current of the bandgap circuit itself. This forms a cyclic requirement. That is, only if the amplifier works the bandgap will generate the required current and only if the bandgap generates the required current, the amplifier will work as required. It was ascertained through simulations that this feedback loop always sets as required. This type of an arrangement makes the current density of the output stage of the amplifier and the PMOS current source to be equal and thereby avoids systematic offsets.

Another common problem with bandgap circuits is that it has two stable states- A zero diode drop state and the actual desired state. This problem can be traced out through simulations by ramping up the supply very slowly. There is a possibility

that both i_1 and i_2 remains zero (and hence i_3) as this is a perfectly valid state. The amplifier is also dead and hence is the loop. However, this is not what we desire and hence the circuit has to be pulled out of this state. This is done by the start-up circuit as shown in Fig.4.8. The two PMOS transistors in the startup circuitry forms a potential divider and biases the in-between node at approximately $\frac{V_{dd}}{2}$. If the diode is stuck at 0 V, the NMOS transistor will have a large V_{GS} developed across it and therefore will pump current into the diode and the resistor R_2. This will cause the potential across the diode to increase which will in-turn resurrect the amplifier and hence the loop. Once the loop gains enough strength, it will make the circuit settle to the other desired operating point. Once the bandgap circuit has reached the desired operating points, the V_{GS} of the NMOS transistor in the start-up would have reduced to zero and thus the start-up circuit will not come into picture once the bandgap has started up High V-t transistors were used in the start-up circuitry to minimize the leakage currents.

The variation of bandgap output voltage with temperature is shown in Fig.4.10 From Fig.4.10, the variation of bandgap voltage is about 110 μV/^{0}C. The gain(from

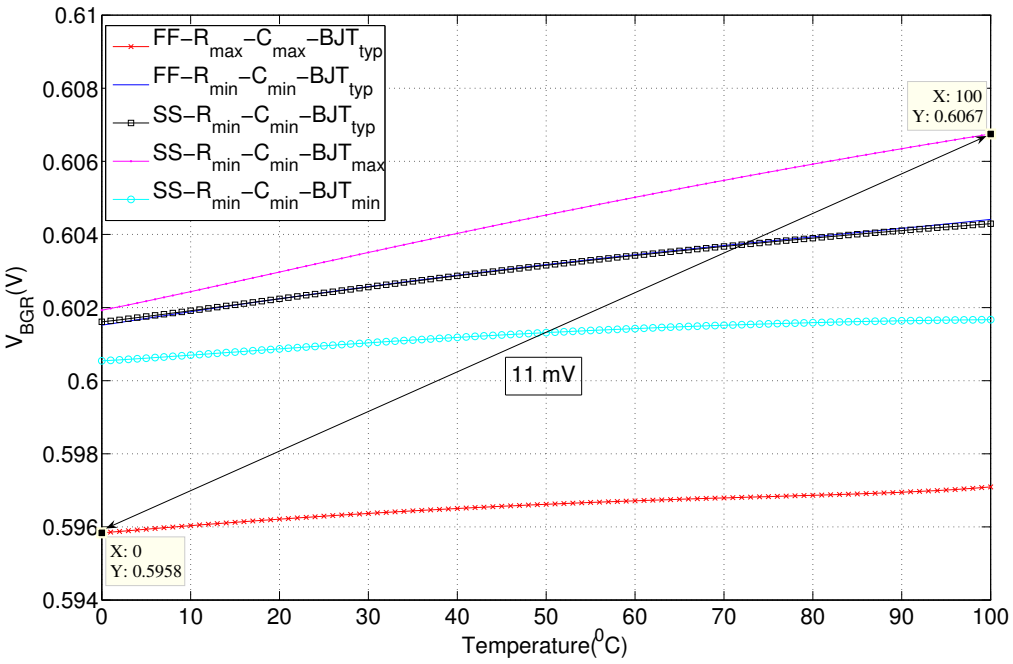

Figure 4.10: Temperature dependence of Bandgap output.

supply to bandgap output) vs temperature of the bandgap circuit for a 10 kHz tone on the supply is shown in Fig.4.11. The starting up of bandgap circuit was verified by slowly ramping up the supply as shown in Fig.4.12.

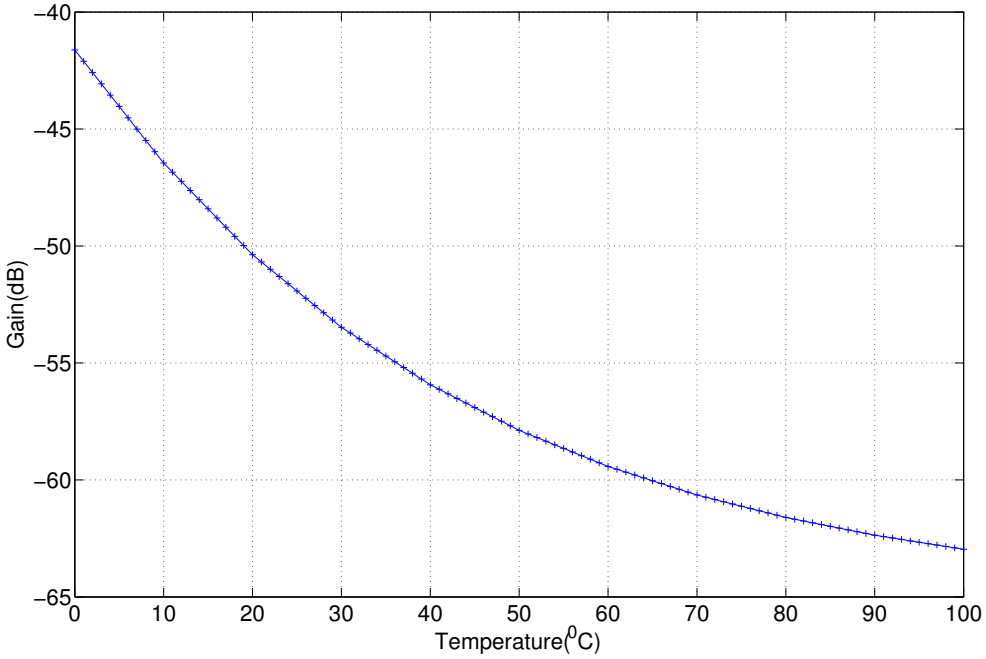

Figure 4.11: PSRR of Bandgap output.

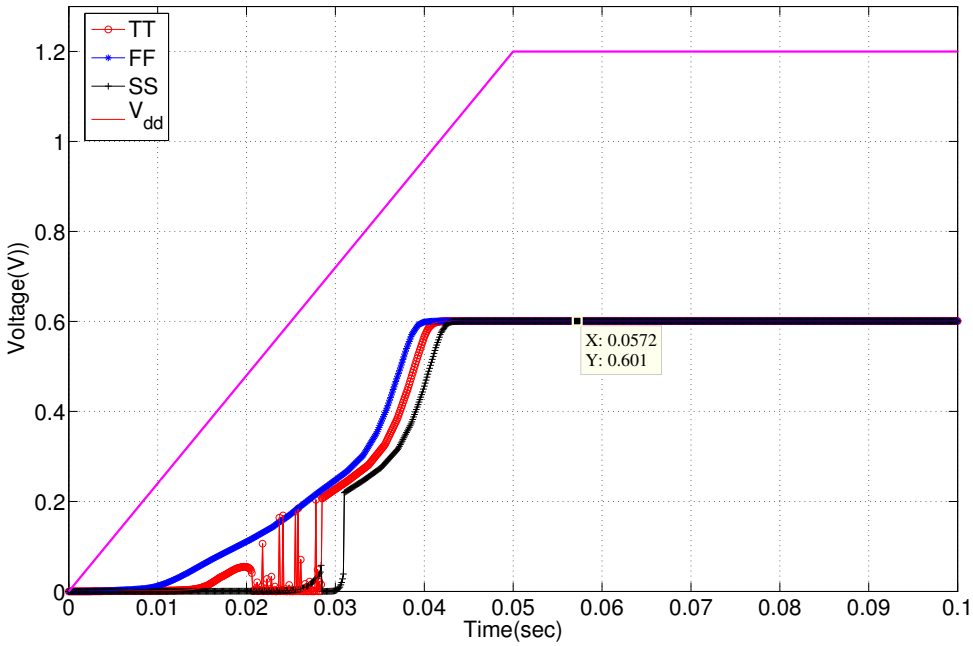

Figure 4.12: Starting up the bandgap.

4.4 On-chip Master current generator and distributor

Portable devices such as hearing aids should have all the circuitry in-built, including the reference current generation. The challenge in designing this block is that this block will be providing the bias current for itself to operate. This is because this is the master current source. The schematic of this block is shown in Fig.4.13. A negative feedback loop is formed by $M_{1,2}$, $M_{3,4}$, M_{10}, M_{11} and R_0. This causes

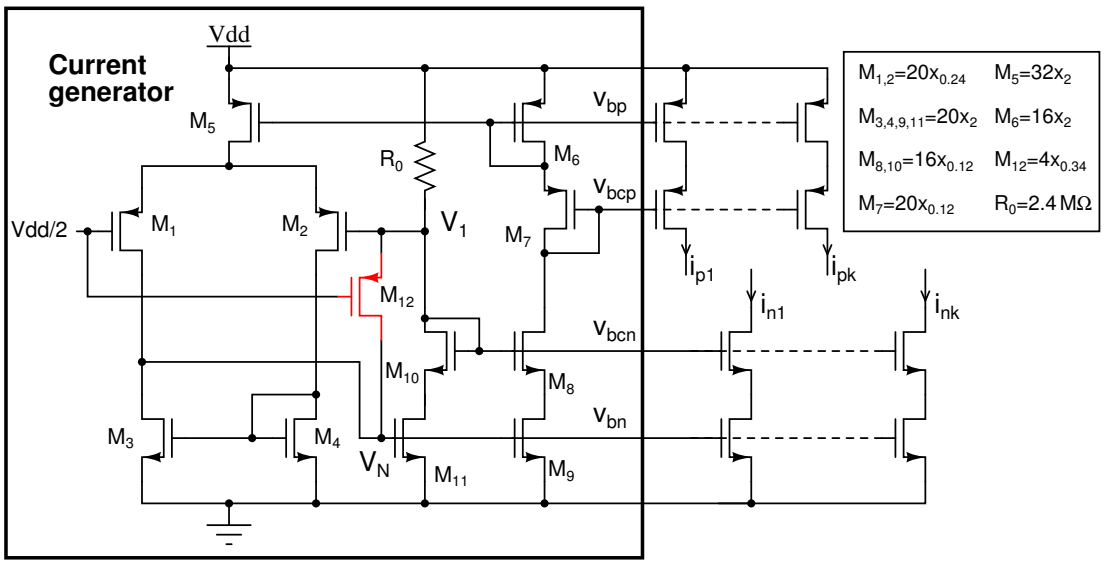

Figure 4.13: Master current source.

V_1 to be $\frac{V_{dd}}{2}$ and causes a current of $\frac{V_{dd}}{2R_0}$ to flow through R_0. This current is mirrored back to the amplifier and acts as the tail current for the amplifier itself. Now there is a circular dependency- only if the amplifier works, a current will be generated and only if a current is generated the amplifier will work. There are two states which satisfies the above condition. One is the desired state and the other is when V_1 is stuck at V_{dd}. When V_1 is stuck at V_{dd}, the current through the second stage of the amplifier is zero. This implies that the tail current is also zero and thus the amplifier is dead. A simple solution to this problem is utilizing a start-up circuit. Including M_{12}(high-V_t) as shown solves this deadlock problem. If V_1 is stuck at V_{dd}, a large V_{SG} is developed across M_{12}. This causes it to pull

out current from the node V_1. This causes V_1 to decrease. Moreover, this pulled down current is pushed into V_N, thereby increasing the node potential. Both the above mechanisms tend to increase the second stage current. The increase of V_N is the dominant mechanism by which the current increases. This increase in current causes an increase in the tail current and this resurrects the negative feedback loop and ultimately causes the circuit to settle to the expected operating points.

The current from M_8 and M_9 is mirrored to all the circuits that requires a current sink and that from M_6 and M_7 to all the circuits that require a current source.

4.5 Chip Floorplan and Layout

The routing of the H-Bridge outputs to the pads must be as short as possible. This minimizes the resistance in series with the bridge and thus avoids degradation of the system efficiency. Another advantage is that the capacitance to ground from the H-Bridge outputs is also reduced which helps avoid increase of switching losses. The FIR-DAC should be placed as close to the input as possible. In total, three different supplies are used. The supplies and grounds of H-Bridge are taken out separately. This helps to avoid spiky voltages from coupling into quieter analog supplies. The supply of the digital blocks are also taken out separately for the same reason. Finally, the supply of the quieter analog blocks are also taken out separately. Using different pads for each supply and connecting all of them externally gives good isolation between these supplies. All the digital inputs and outputs are buffered by means of simple inverter circuits. A provision has been kept to either give a serial input through SPI or as a 16-bit parallel input word. The layout is shown in Fig.4.14

The front-end of this hearing aid which was designed by others was also integrated into this chip. Therefore, this chip contains both the front-end and back-end. The complete floorplan of this chip is shown in Fig.4.15. The pinout details is shown

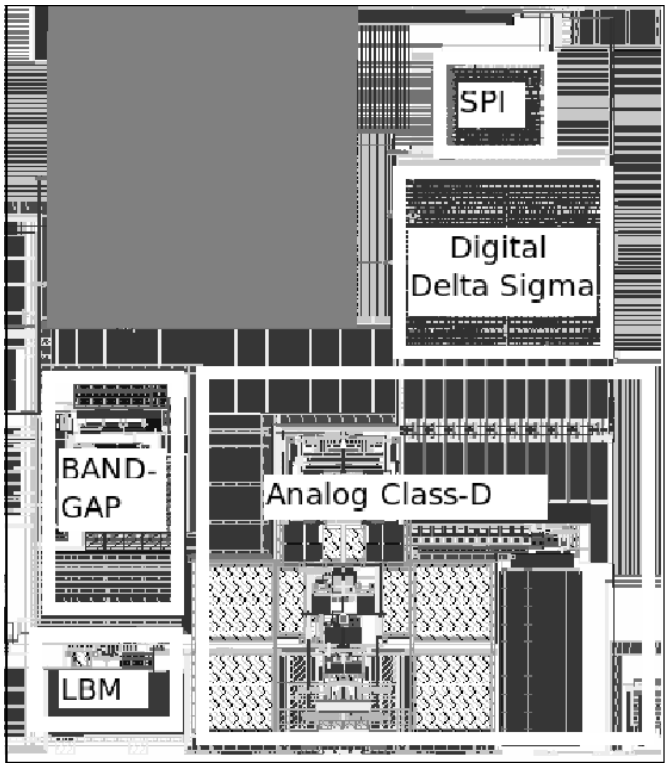

Figure 4.14: Layout of the entire backend.

in Fig.4.15. An 80-pin QFN package was chosen to package the chip.

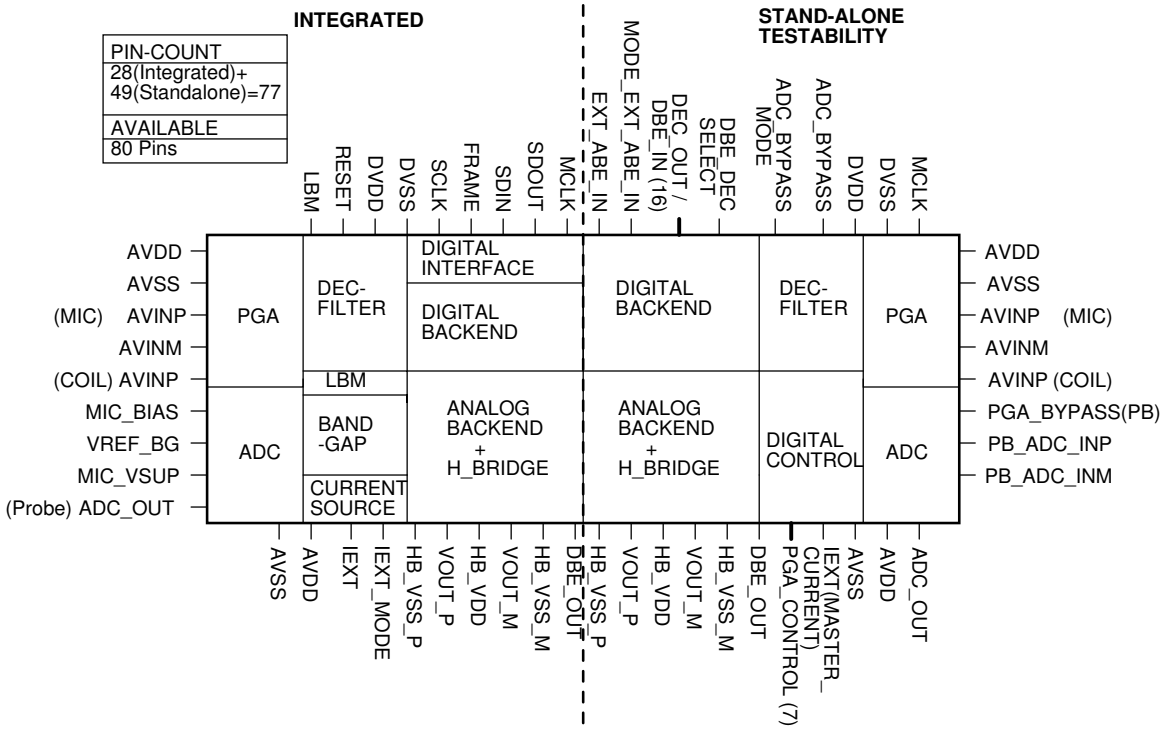

Figure 4.15: Floorplan of the entire chip with pin-out details.

The complete layout of this chip is shown in Fig.4.16

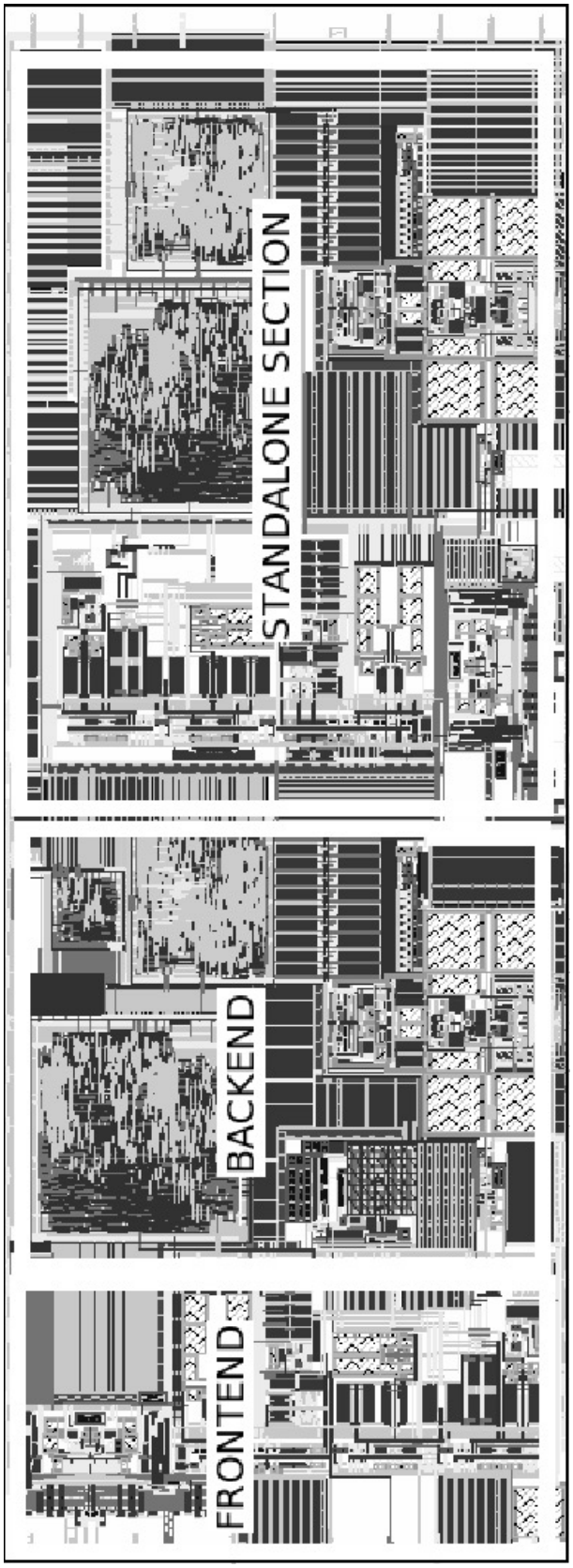

Figure 4.16: Complete chip layout.

CHAPTER 5

Testing and Measurement Results

5.1 Board Design

Since the class-D output has a large amount of high-frequency components, the radiation it emits will be considerable. In order to avoid this from coupling to the nearby blocks a four layer board was chosen. Since the chip had both the front-end and the back-end, provisions were kept in the board to test the performance of both the blocks. To describe the front-end briefly, it has a Programmable Gain Amplifier(PGA), an ADC and a Decimation filter. The input to this front-end is in analog domain and the output is in digital domain. The inputs are AC-coupled to the chip. A provision has also been made to supply the required input DC bias to the chip. On-board buffer ICs have been placed to take the digital outputs.

The inputs for the backend is generated using an FPGA. The synchronization signals like SCLK and FRAME that are generated from the chip have to be given to the FPGA. Since the chip's logic levels are 0 V and 1.2 V and the available FPGA's logic levels are 0 V and 2.5 V, the chip's output has to be up-converted. This is done with the help of up-converter ICs. RMC connectors are used to power up the board and buck sticks have been provided to apply input or probe outputs. Analog inputs are fed in and analog outputs are taken out of the board through BNC connectors. On-board LDO ICs were used to regulate the power supply. Two separate supplies, one for analog and one for digital is used. The schematic of the board is shown in Appendix.D.

A complete plane has been devoted for the board supply and another complete plane for the ground. This helps reduce the series resistance and inductance in the

supply and ground paths. It is advantageous to assign the first plane for signal routing, the next for ground, the next for power and the last again for signal routing. Since the ground plane is very near the signal plane, the area of ground loops are considerably reduced and the return currents need not travel a long way. The same argument holds for supply current paths too. Furthur, since the ground plane and supply planes are adjacent to each other, there will be a good amount bypass capacitance between the two. Power islands were created in the supply plane for the digital supply and the analog supply. These islands ensure shortest paths for currents being drawn from their respective supplies. The free space was filled with copper which can act as an effective termination for field lines.

The class-D outputs need to be filtered before giving into an audio analyzer. Therefore, a simple third order Low Pass Filter(LPF) as shown in Fig.D is used. It should be noted that the adopted LPF leads to huge efficiency degradations. However, it also leads to huge space saving as now inductors are not used. The cut-off of the LPF is chosen such that the out-of-band components of the shaped PWM output are filtered out sufficiently. The snapshot of the board is shown in Fig.5.1 and that of the measurement setup in Fig.5.2.

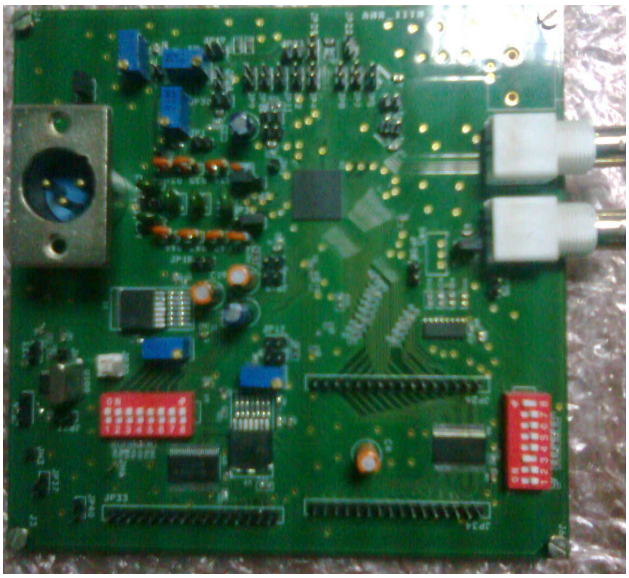

Figure 5.1: Snapshot of the board.

Figure 5.2: Snapshot of the Measurement setup.

5.2 Measurement results

5.2.1 16-bit digital to 1-bit digital converter

The measurement setup is shown in Fig.5.3. A 16 bit digital sine wave at a rate of 40 kHz is generated by the FPGA (A). It is provided as the input to the chip(DUT). The 1 bit digital PWM signal(B) is captured using a logic analyzer and then its PSD is taken. All the blocks operate synchronously from a master clock of 20.48 MHz.

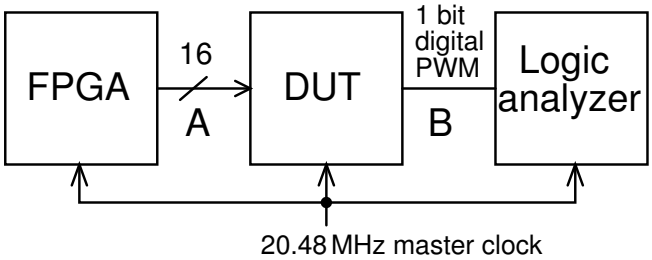

Figure 5.3: Measurement setup for measuring performance of digital class-D section

Fig.5.4 shows the PSD of the 1 bit digital signal for various input amplitudes.

From the PSD data in Fig.5.4, the SNDR, SNR and THD are calculated and is plotted for various input amplitudes. This graph is shown in Fig.5.5. All the harmonics of the fundamental upto 10 kHz were chosen for THD calculation. This

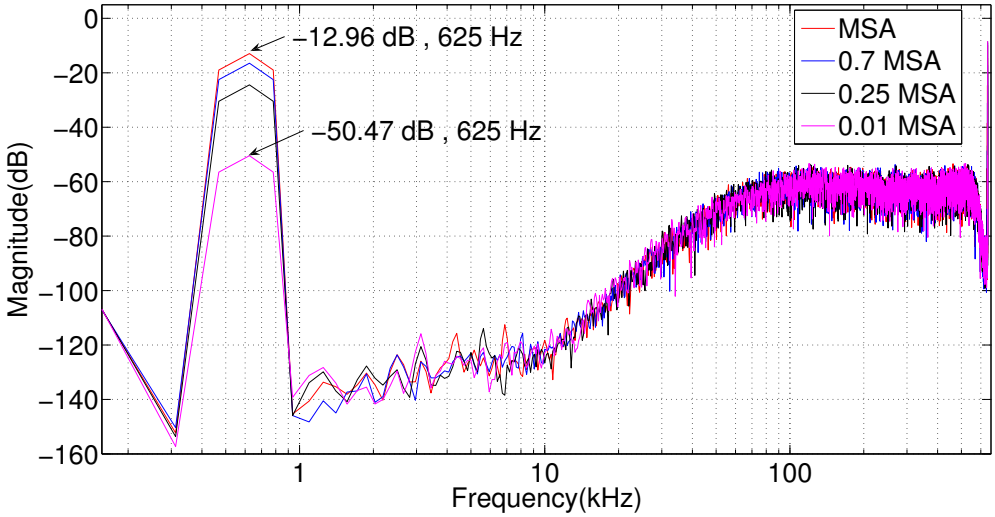

Figure 5.4: Measured PSD of the digital output.

digital system achieves a peak THD of about -99.5 dB and a peak SNR of 102.5 dB.

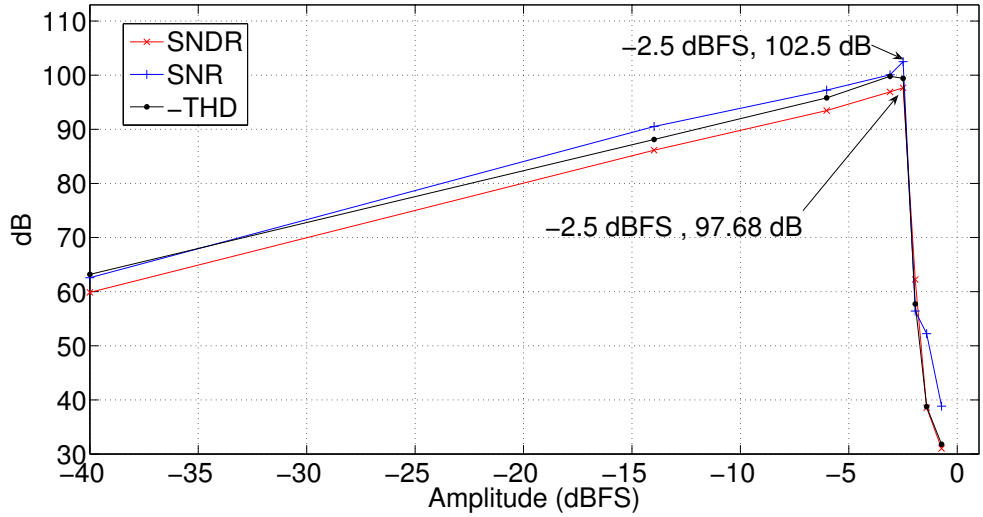

Figure 5.5: Amplitude sweep measurements.

5.2.2 Analog class-D amplifier

The measurement setup is shown in Fig.5.6. The FPGA generates the 1 bit PWM signal(at A). This 1 bit PWM signal is applied as input to the analog section(closed loop class-D amplifier) of the chip(DUT). The differential analog PWM output

signal is low pass filtered using Audio Precision's AUX0025 low pass filter. A load R_L has been connected across the H-Bridge to facilitate measurements with load. This low pass filtered signal is given to an AP-SYS-2722 audio analyzer which measures the PSD of the analog PWM signal.

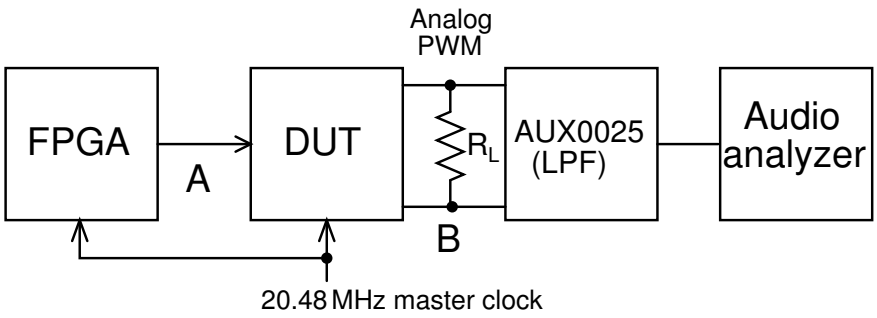

Figure 5.6: Measurement setup for measuring performance of analog class-D section

The filtered output is given through XLR connectors to the audio analyzer. The analog section of the class-D amplifier was tested stand-alone. The inband idle channel noise was calculated to be 13.6 μV_{rms}. The PSD of the analog PWM signal for the idle channel case and for single tone input at -2 dB MSA(0.75 times full scale) is shown in Fig.5.7.

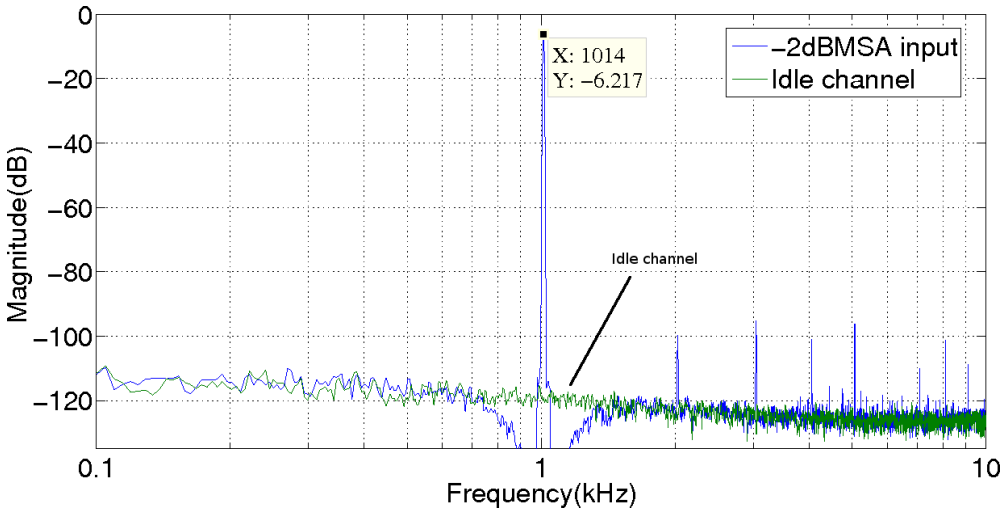

Figure 5.7: PSD of the filtered analog PWM signal.

The input amplitude was gradually increased from zero till the MSA and the THD+N(%) $\left(\text{THD+N}(\%) = \sqrt{\frac{\text{Harmonic power+Noise power}}{\text{Signal power}}} \cdot 100\right)$ for each input amplitude is plotted. The same experiment was repeated for a load resistances

of 100 Ω. The resulting graph is shown in Fig.5.8. A peak THD+N(%) of 0.006 is

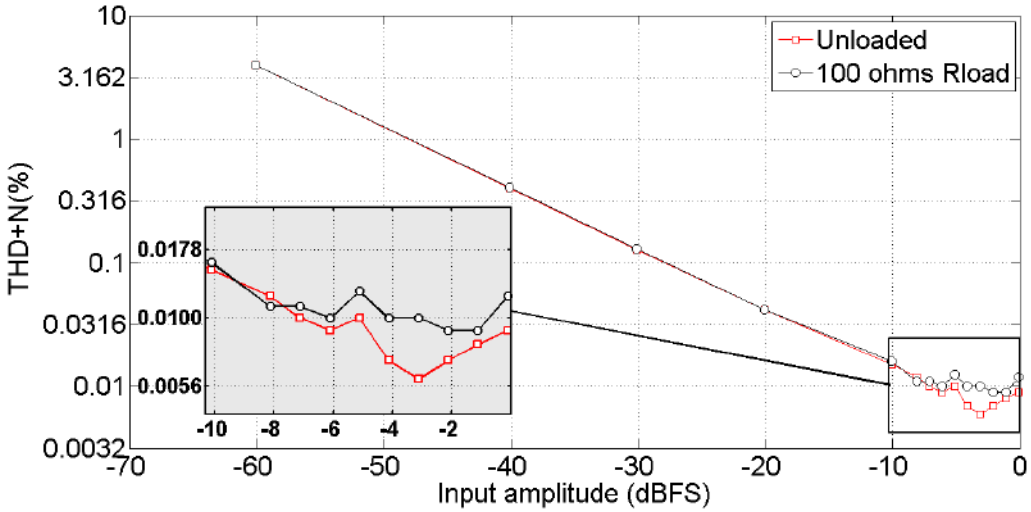

Figure 5.8: THD+N(%) for various input amplitudes.

achieved from silicon results. The graph of THD+N(%) vs output power is shown in Fig.5.9. The load is a single resistor of value 100 Ω connected directly across the H-Bridge.

Figure 5.9: THD+N(%) for various output powers.

Since this design(backend class-D driver section of the hearing aid) was integrated with the front-end section of the hearing aid and fabricated, it was not possible to measure the power consumed by the class-D amplifier section alone.

CHAPTER 6

Conclusion

This thesis dealt with techniques for the design, implementation and testing of class-D amplifiers for hearing aid applications. The primary difficulty in converting high resolution(sixteen bits and greater) digital signals into analog were discussed in this thesis. The design and implementation of digital input class-D amplifiers was discussed in detail. The advantages and disadvantages of various digital input class-D topologies were also described in detail. It was seen that direct conversion of high resolution digital to analog is wasteful of power and degrades signal quality and hence a two step approach was adopted. The various problems associated with using the digital output to directly drive the speaker were discussed. It was seen that adopting a negative feedback loop around the class-D driver stage mitigates all the above mentioned problems to a great extent. The problem of clock jitter at the digital to analog interface was addressed by adopting a Finite Impulse Response DAC(FIR-DAC). The design and implementation of the FIR-DAC was described in detail in this thesis. The dominant source of nonlinearity in closed loop class-D driver stages and ways of improving the linearity using the assisted opamp technique was also discussed. The design of comparator with inbuilt non overlap generator was proposed. The layout of the taped out chip was shown.

Design of miscellaneous blocks such as Serial Peripheral Interface(SPI), Bandgap Voltage reference and Low Battery Monitor(LBM) was discussed in this thesis. The design of test board to aid the testing of the chip was explained. The issues that are to be considered while designing a test board for this sort of an application were also discussed briefly. From the measurement results, it was seen that the digital 16 bit to 1 bit converter works exactly as designed for and the measured results matches closely with simulations. This digital system achieves a peak THD

of about -99.5 dB and a peak SNR of 102.5 dB. The analog closed loop section also works fine. The peak THD+N(%) achieved was around 0.006 (4 dB lesser than simulations) which adheres to the requirement of hifi audio drivers.

In essence, the driver stage of a hearing aid was designed and implemented successfully. It was made highly efficient by using class-D driver stage. The linearity of the system was improved by using techniques such as pseudo NPWM and assisted opamp technique and the jitter performance was improved by using an FIR-DAC.

APPENDIX A

Efficiency degradation in practical class-D amplifiers

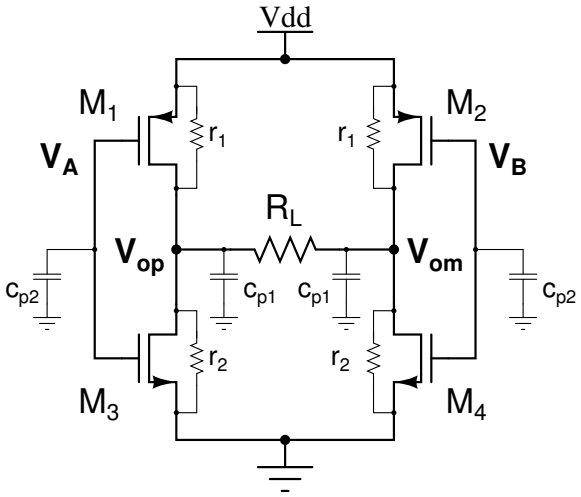

Figure A.1: Parasitics in class-D driver stage.

Efficiency of practical class-D amplifiers are less than 100%. One of the main factors is the finite on-resistance of the switches in the driver stage. If the on-resistances are represented by r_1 and r_2 as shown in Fig.A.1 and the load current is denoted as $i_L(t)$, then the amount of power wasted as heat in the switches is $i^2_{Lrms}(r_1+r_2)$. This type of loss is termed as conduction loss. Therefore minimizing the on-resistance of the switches will decrease the amount of power lost as heat. Another mechanism that causes power loss is the charging and discharging of parasitic capacitors c_{p1} and c_{p2} and is termed as switching loss. If both the input and the output of the bridge can swing between V_{dd} and ground, the power lost due to switching is $2(c_{p1} + c_{p2})V^2_{dd}f_{avg}$. This type of loss dominates at very low input amplitudes. Here, f_{avg} denotes the average switching frequency. Another mechanism of power loss is during dead time. When the PWM signal transits from one state to another, there can arise a situation when both the switches on the

same side are simultaneously on for a short duration. During this duration, there will be a very low impedance path from V_{dd} to ground through the on-resistance of the switches which can potentially damage the switches. Therefore, the PWM signal is given through a dead-time generator block before driving the H-Bridge. This block generates non-overlapping signals for the same-side switches. During the dead-time, the load current flows through the body diodes of the transistors. This leads to a relatively huge potential drop across the switches with the full load current flowing through them. This causes considerable power loss(in inductive loads) and is termed as dead-time loss. This loss can be reduced by reducing the dead time but the risk of supply shorting with ground increases. Apart from the above losses, there is another loss mechanism where during transitions the current through the switch has risen to $i_L(t)$ but the voltage across it still remains about V_{dd}. Therefore for a small fraction of the switching period there will be a large instantaneous power drawn from the supply. These losses can be reduced with the help of snubber circuitry. Finally, the losses associated with the control system also reduces the overall efficiency of the class-D amplifier. If conduction loss is denoted as $P_{c,loss}$, switching loss as $P_{sw,loss}$, dead-time loss as $P_{dt,loss}$, transition loss as $P_{vi,loss}$, control system loss as $P_{ctrl,loss}$ and the power delivered to the load as P_L, then,

$$\text{Efficiency}(\eta) = \frac{P_L}{P_L + P_{c,loss} + P_{sw,loss} + P_{dt,loss} + P_{vi,loss} + P_{ctrl,loss}} \tag{A.1}$$

Practically, conduction loss is dominant for very high output loads and switching loss during idle states and for light loads. Conduction losses can be reduced by increasing switch sizes to reduce their on-resistance. However, this increases the parasitics at every node of the switch, thereby increasing switching loss. Therefore an optimum switch size must be chosen from actual simulations that would keep the sum of conduction loss and switching losses to a minimum.

APPENDIX B

Nonlinearity in UPWM

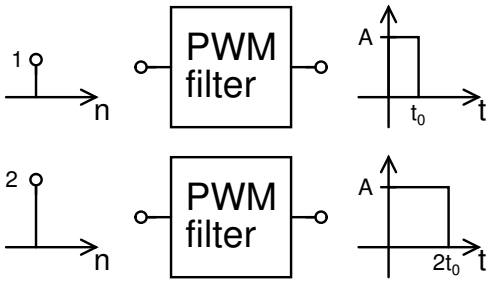

Figure B.1: Impulse response of of a PWM filter.

The process of mapping amplitudes of a uniformly-sampled waveform into pulse widths is a non-linear operation. The source of non-linearity can be explained with the aid of Fig.B.1. The PWM filter takes an amplitude as input and generates a proportional pulse-width as output. If the input is a sample with unit amplitude, the output of the PWM filter is a pulse with width t_0. This can be thought of the impulse response of the filter. Now if the input amplitude is doubled, the pulse width also doubles. Therefore, the PWM filter has an input signal dependent impulse response. If the filter was linear, the output amplitude should have doubled with the pulse width remaining the same. Therefore, one can conclude that UPWM conversion is non-linear.

APPENDIX C

Linearized, Low-frequency model of PWM block

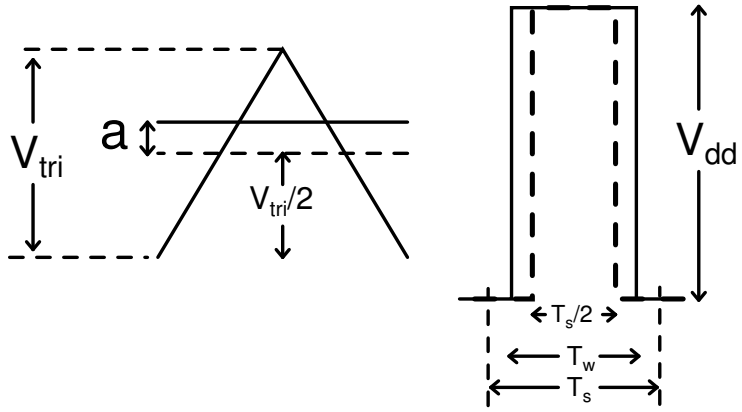

Figure C.1: Linearizing the PWM block.

Let the carrier be a triangular waveform with an amplitude V_{tri} as shown in Fig.C.1. To linearize this block, consider an operating point, say, $\frac{V_{tri}}{2}$. Let the corresponding pulse-width for this operating point be $\frac{T_s}{2}$, as shown in Fig.C.1. The area under the PWM signal is $\frac{V_{dd}T_s}{2}$. Now assume a small perturbation to the operating point by an amplitude 'a'. Now the corresponding pulse width would be T_w. Geometrically,

$$T_w = \frac{\left(\frac{V_{tri}}{2} + a\right)}{V_{tri}} T_s \tag{C.1}$$

Therefore, the average value of the PWM waveform is,

$$V_{\text{out,avg}} = V_{dd} \frac{\left(\frac{V_{tri}}{2} + a\right)}{V_{tri}} \tag{C.2}$$

If we make an assumption that the perturbation (message signal) occurs at a much lower frequency than the triangular carrier, then the instantaneous value

of the input message can be represented by the local average of the pulse width modulated waveform. This implies that this model is accurate only for messages whose frequency is much lesser than that of the triangular carrier and hence is a low frequency model.

Differentiating Eq.C.2 with respect to the message 'a' gives

$$\frac{\mathrm{d}V_{\mathrm{out,avg}}}{\mathrm{d}a} = \frac{V_{dd}}{V_{tri}} \tag{C.3}$$

Therefore, Eq.C.3 represents the low frequency small signal gain of the PWM block.

APPENDIX D

Printed Circuit Board(PCB) schematic

The pin connections of the taped out chip is shown in Fig.D.1.

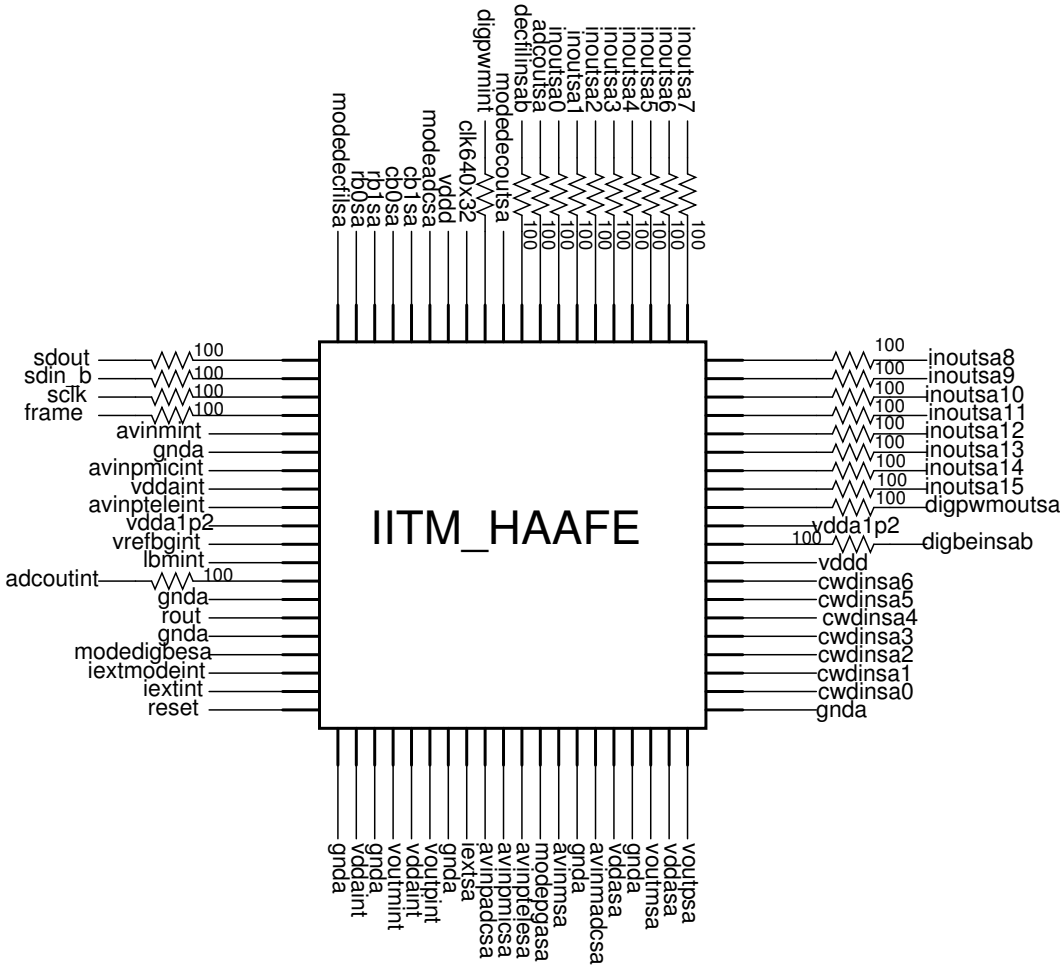

Figure D.1: Schematic- Page1.

The connectors for providing analog inputs, the TI LDOs for supplying the power to the chip and the master current source is shown in Fig.D.2.

The custom low pass filter used for filtering out the high frequency components of the analog PWM output is shown in Fig.D.3. The buffer IC used for accepting digital inputs/outputs from/to FPGA are also shown in Fig.D.3.

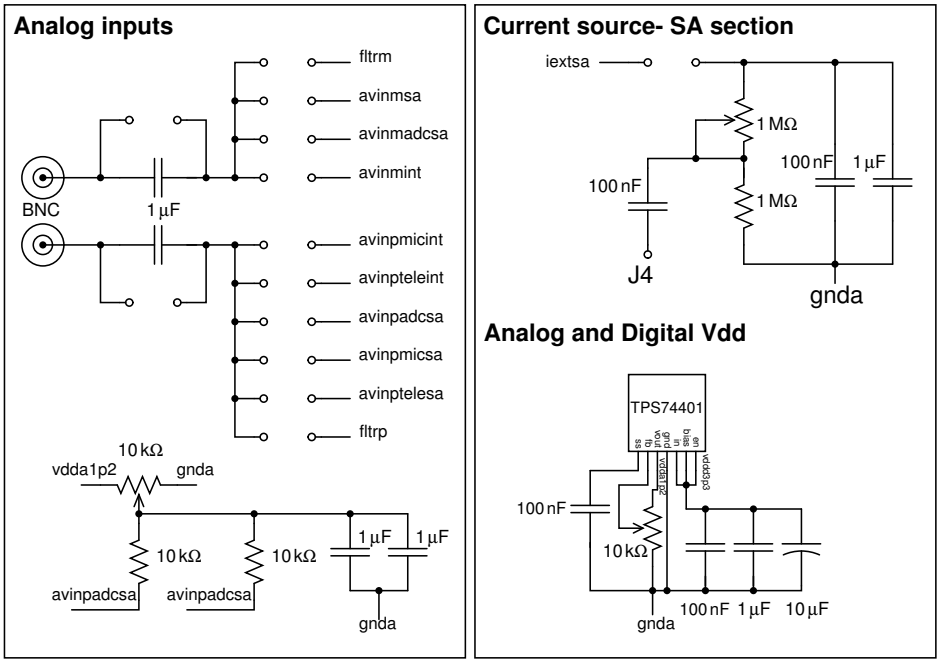

Figure D.2: Schematic- Page2

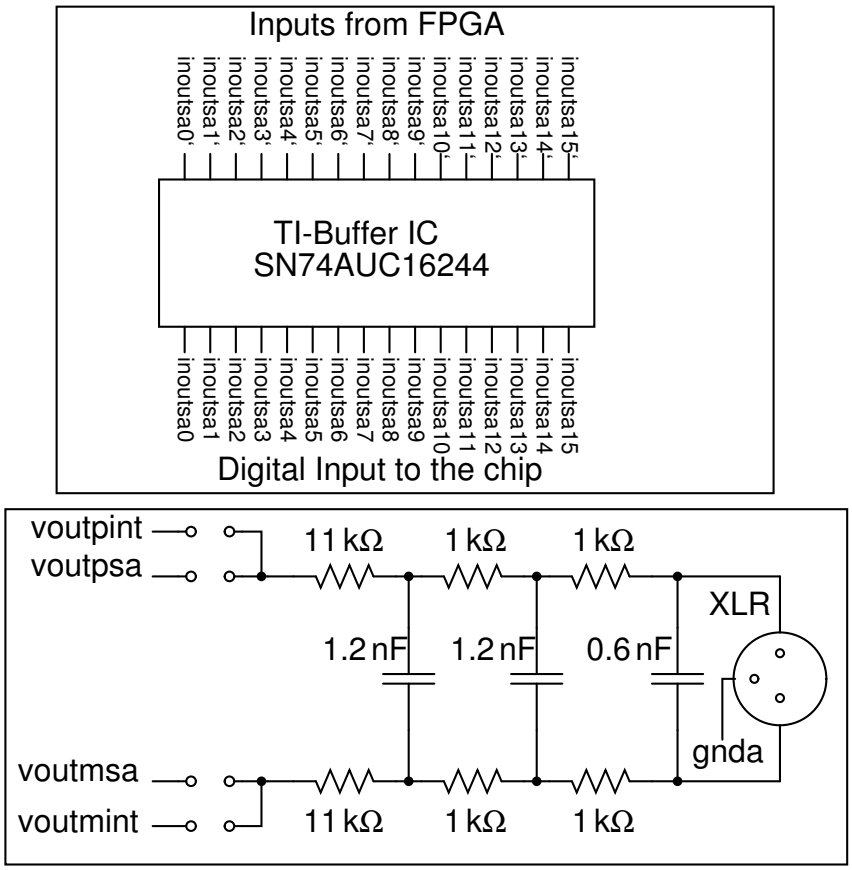

Figure D.3: Schematic- Page3.

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