VLSI DATA CONVERSION CIRCUITS : PROBLEM SET 7

This problem set will cover the design of a continuous-time $\Delta\Sigma$ ADC designed as a part of an FM receiver. The signal bandwidth is 200 kHz, and an inband peak SNR of 90 dB is desired. For some design margin, the in-band SQNR should be atleast 12 dB better than the desired SNR. For reasons beyond your control, the OSR has been chosen to be 64. For implementation reasons, a quantizer resolution greater than 4 bits is not feasible. Your manager is also uncomfortable with large OBG - so let us limit the maximum OBG to 3. Since the supply voltage is 1.8 V, the quantizer range is 3 V (peak-to-peak differential). For reduced jitter sensitivity, assume an NRZ feedback DAC.

1. Determine the order and number of bits you will want to use in the quantizer.
2. Determine the coefficients of the NTF, and plot the NTF magnitude response in a dB scale. What is the MSA ?
3. What is the maximum RMS clock jitter you can tolerate, so that the SNR degradation due to clock jitter is less than 1 dB ?
4. Assume that the Flash/DEM/DAC path has a delay of 1 ns. Determine the transfer function of the continuous-time loop filter required to achieve the desired NTF.
5. Assuming a CIFF loop filter, scale the integrator outputs so that they never go beyond 1.5 V (peak-to-peak differential).
6. Implement the loop filter using fully differential active-RC integrators. Use ideal opamps. The second and third integrators should use integrating resistors of 50 K each. The feedback resistor of the summing opamp should be 50 K. The inband thermal noise added by the input resistors of the first integrator should limit the inband SNR of the ADC to 94 dB. Limit the opamp outputs to the supply voltage - otherwise your modulators will oscillate. You can use a verilog-A ADC/DAC.
7. Run time domain simulations with a 40 kHz input tone with an amplitude of 0.9 MSA. Plot the PSD of the ADC output, where the PSD is computed with a 1024 point Hann window. Determine the in-band SQNR and compare with your calculations.
8. Plot the waveforms at the outputs of each integrator to ensure that they do not go over 1.5 V pp,diff.