## 23.3 Analog Processing Circuits for a 1.1V 270μA Mixed-Signal Hearing Aid Chip

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This single-chip mixed-signal hearing aid system exhibits audio performance superior to that of published chips consuming over 1mA of battery current [1]. Circuit and architectural design techniques reduce system power to the level where 40 days of average lifetime is achieved for a small zinc-air battery.

Figure 23.3.1 is a block diagram of the hearing aid chip. Microphone signals are buffered by an external JFET source follower and applied to an input compressor and limiter (ICL) amplifier. After a passive anti-alias filter, the audio signal is digitized by the third-order ΣΔ ADC and fed through a programmable prescription digital filter. A digital three-level ΣΔ DAC modulator follows, and its 2b output stream operates a push-pull H-bridge receiver (earphone) driver. The shaped DAC quantization noise is filtered by the receiver electrical and mechanical response. The microphone power and circuit bias block is based on a sub-bandgap reference. Those blocks outlined with solid lines will be detailed here.

The chip operates with a single cell voltage supply, as low as 1.1V. The 0.6μm, 3.3V CMOS IC process used includes a deep n-well layer essential for junction isolation of digital and analog sections. This layer also affords a vertical npn bipolar device in the input stage opamp to reduce $1/f$ noise, as well as in the bandgap reference. Also available are a low threshold voltage option for the MOS devices and EEPROM cells for prescription selection and analog trim functions. Both the ICL and the ADC use a locally-boosted supply voltage to drive the nMOS analog switch gates.

A diagram of the ICL is shown in Figure 23.3.2. After conversion from the single-ended microphone input by this stage, fully-differential circuitry is employed throughout the analog blocks. A closed-loop architecture satisfies 0.03% input-stage harmonic distortion requirement, and keeps static power consumption constant over all gain settings. Resistor taps and nMOS switches are provided for 83 gain steps of 0.5dB, from –1dB to 40dB. Input signals experience gain compression and release governed by four time constants. Relatively fast gain reduction and recovery occurs for brief and exceptionally high sound levels, whereas compression and release from sustained sound levels occurs at significantly slower rates.

The bidirectional shift registers in Figure 23.3.2 drive the resistor array switches without intervening decoder. These registers may change the state of only one switch per clock cycle, giving glitch-free gain steps. Compare and maximize are computed with a chain of simple bitwise gates. Closed-loop gain is reduced as 'one' bits are shifted to the right in response to sound levels greater than full scale, and is increased as 'zero' bits are shifted to the left during release. The first 57 steps of gain reduction are realized by taps on the feedback resistance, and the final 26 steps, for very high sound levels, adjust the input resistance. This arrangement saves considerable bias current in the opamp output stage, since minimum load resistance is kept high, but still gives minimum noise with lower input resistances at high gain settings. A 3dB hysteresis window inhibits changes in the gain setting for steady state sound levels, preserving linearity. Even though the incremental resistance for each 0.5dB gain step is nonuniform, almost all of the resistance required for each tap is realized with a varying number of unit resistors from an array of matched cells. Small stub resistors outside the array are then used on each tap to make up the difference between the nearest integer number of unit resistors and the nonuniform resistance required. This layout, achieves accurate logarithmic gain steps and accurate total gain.

The input sampling network for the third-order ΣΔ ADC is shown in Figure 23.3.3. The use of a single pair of differential sampling capacitors, $C_S$, reduces the total input capacitance for a given $kT/C$ noise budget, and allows reduction of opamp power. An additional short clock phase, $\phi_3$, discharges these capacitors before each sample and erases the charge condition from the previous full-scale reference sample. This reduces the dynamic signal input charge required, eliminating an active buffer in preference to a simple passive RC antialias filter as shown. Furthermore, the switches that sample the reference voltage with a polarity that conveys the feedback digital bit, D, are arranged to hold both parasitic capacitances $C_P$ discharged to ground except around time interval $\phi_2$. This suppresses a mechanism for data-dependent charge drain from the reference voltage, and eliminates an active buffer for the reference. A simple RC filter from the battery supply, as shown, performs well as a reference supply in this system.

A three-level DAC minimizes power consumed in the output H-bridge driver, since most samples will be zero for the typical audio levels well below full scale. Return-to-zero (RTZ) coding is used to preserve linearity, and the RTZ pulse edges are resynchronized to the lowest jitter clock in the system just before feeding the output buffers. This reduces sensitivity to jitter in the DAC circuitry, and saves system power by requiring supply current be spent only to suppress jitter in the clock oscillator core.

A low-jitter clock is provided by the three-stage ring oscillator in Figure 23.3.4. The bias current for all stages is trimmed at test to set the clock frequency to 2.56MHz. The delay in each stage is implemented by symmetrical p and n transconductances and load resistances driving the gate capacitance of the next stage. Symmetry is essential to match clock waveform rise and fall times, and reduce up-conversion of $1/f$ noise [2]. In addition, extra capacitance added at the tail nodes, $C_T$, significantly reduces jitter from kickback and from current source noise.

System power is minimized by careful planning of digital clock rates, from the ADC decimation through the digital filtering and DAC modulator. Power required by digital filtering is minimized with a specialized processor design, rather than a general instructional processor.

A measured output voltage spectrum is plotted in Figure 23.3.5. The input is a 1kHz sinusoid at 4mV peak amplitude. This level corresponds to routine conversational speech at about 79dB SPL, and is 6dB below the level where gain compression is initiated by the input stage. The output is loaded with a test circuit equivalent to a receiver. Harmonic distortion is well below the 0.1% specification for low-level inputs. Figure 23.3.6 summarizes the chip performance, and Figure 23.3.7 is a die micrograph.

*References:*

[1] H. Neuteboom et al., "A DSP-Based Hearing Instrument IC," *IEEE JSSC*, vol. 32, no. 11, Nov. 1997.
[2] A. Hajimiri et al., "Jitter and Phase Noise in Ring Oscillators," *IEEE JSSC*, col. 34, no. 6, June 1999.

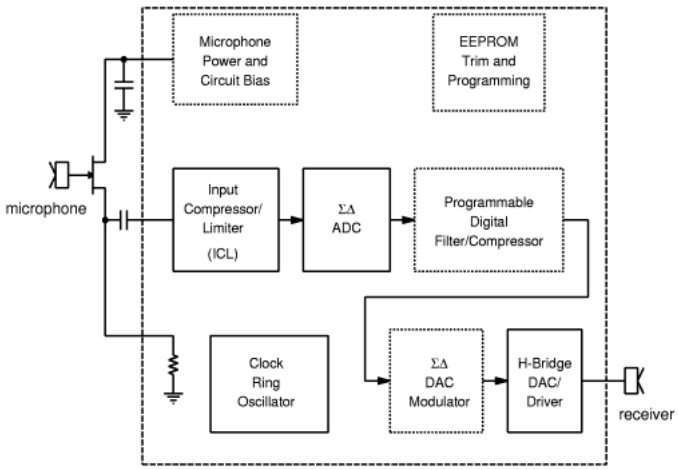



Figure 23.3.1: Hearing aid chip block diagram.

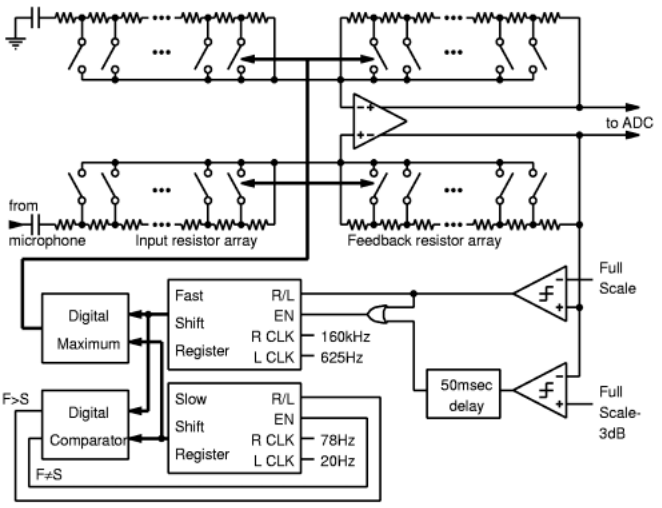



Figure 23.3.2: Input compressor-limiter (ICL) schematic.

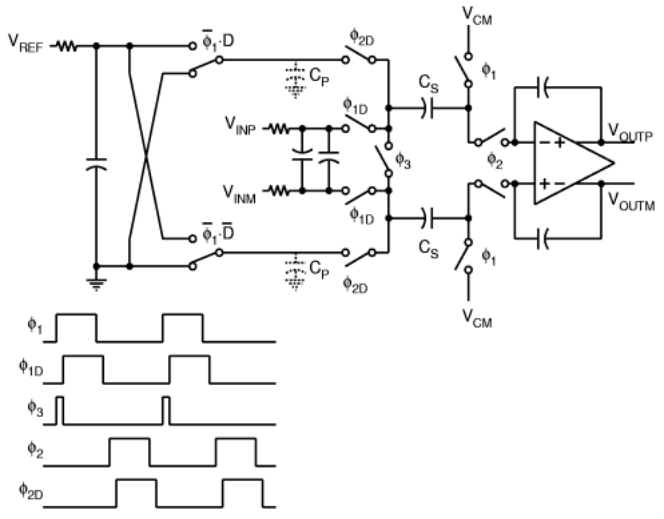



Figure 23.3.3: First ΣΔ ADC integrator.

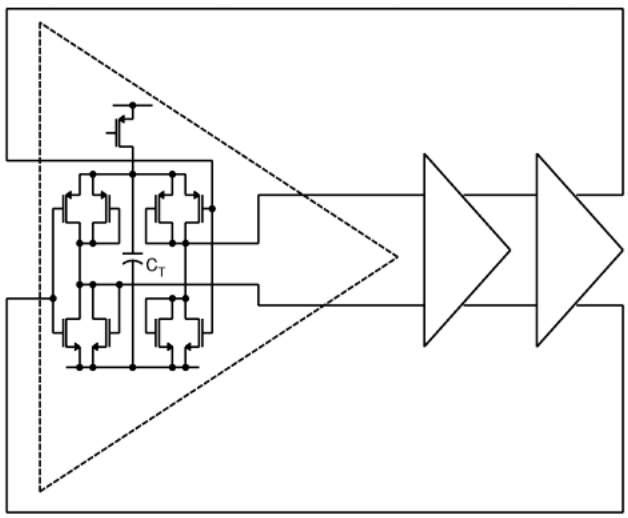



Figure 23.3.4: Three-stage ring oscillator schematic.

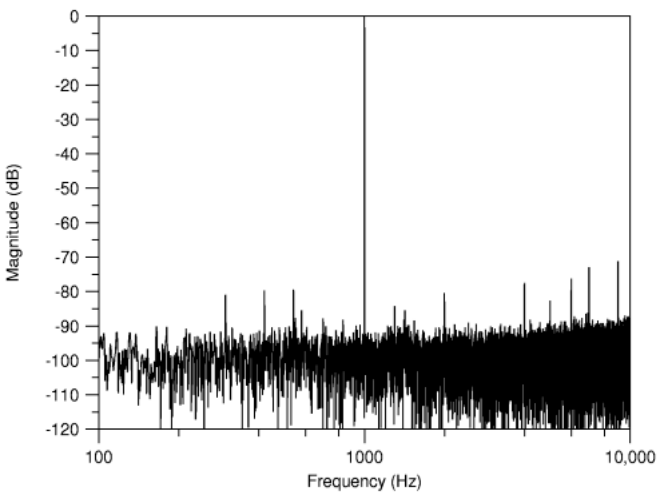



Figure 23.3.5: Spectrum of measured output with 4mV, 1kHz input sinusoid.

| | | |
|---|---|---|
| Battery voltage range | | 1.1-1.5V |
| Battery current consumption (no signal) | | |
| 1.1V supply | | |
| Analog | 173μA | |
| Digital | 48μA | |
| H-Bridge | 15μA | |
| Ring oscillator | 34μA | |
| Total | | 270μA |
| 1.3V supply | | 299μA |
| 1.5V supply | | 323μA |
| -3dB Bandwidth | | 100Hz-10kHz |
| Input referred noise (100Hz-10kHz) | | 2.8μVRMS |
| Total harmonic distortion | | |
| $v_{IN}$=7mVpk | | 0.02% |
| $v_{IN}$=80mVpk | | 0.5% |
| Input compressor maximum gain step error | | 0.09dB |
| Maximum input signal | | 450mV peak |
| Clock jitter | | 147ps RMS |
| Sub-bandgap reference stability | | 1% |
| Temperature range | | 20-40°C |
| Die size | | 12mm² |

Figure 23.3.6: Measured performance summary.

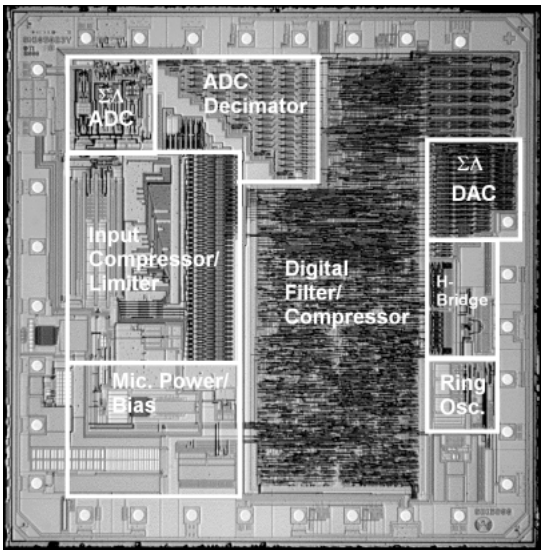
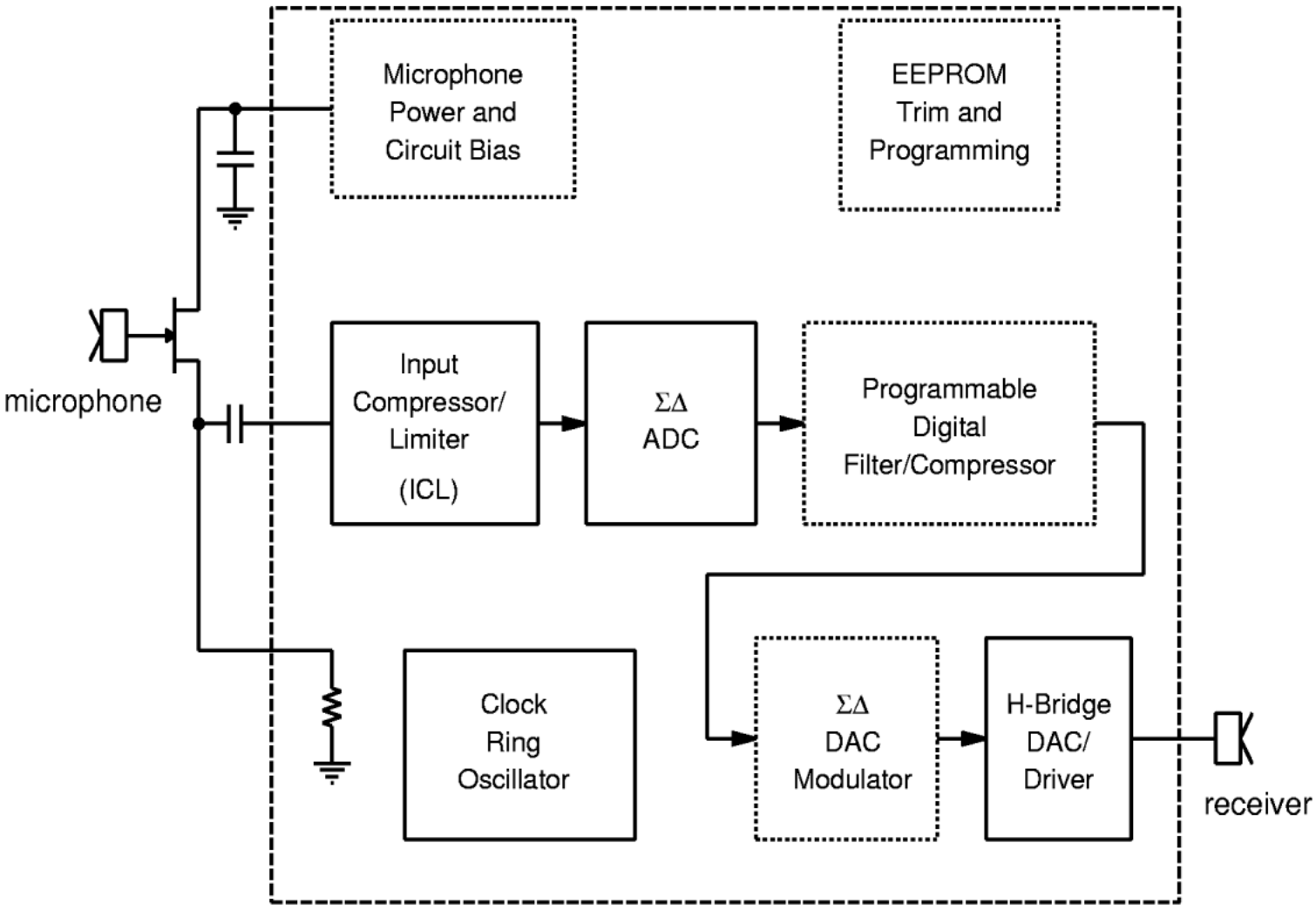



**Figure 23.3.7: Die micrograph.**

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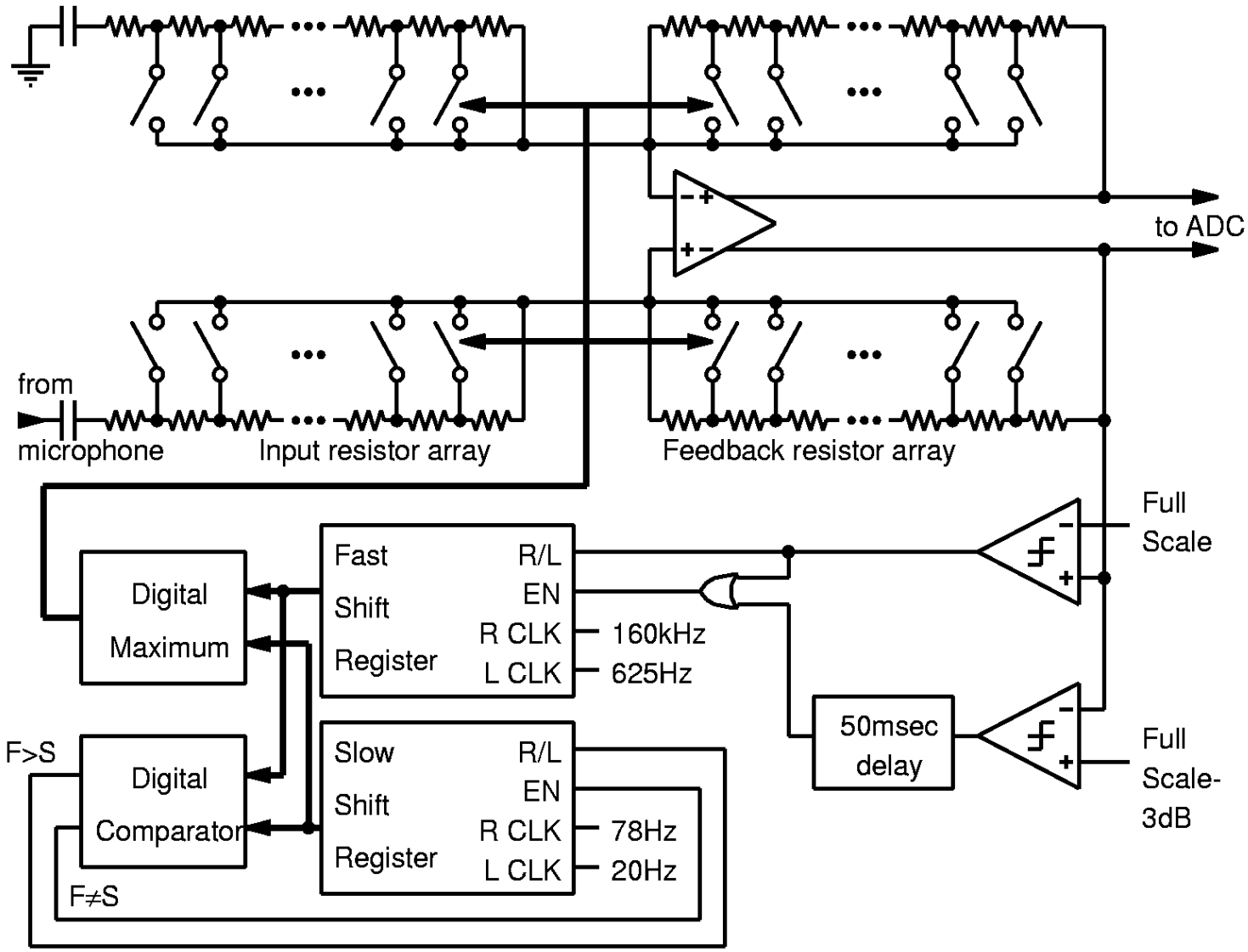


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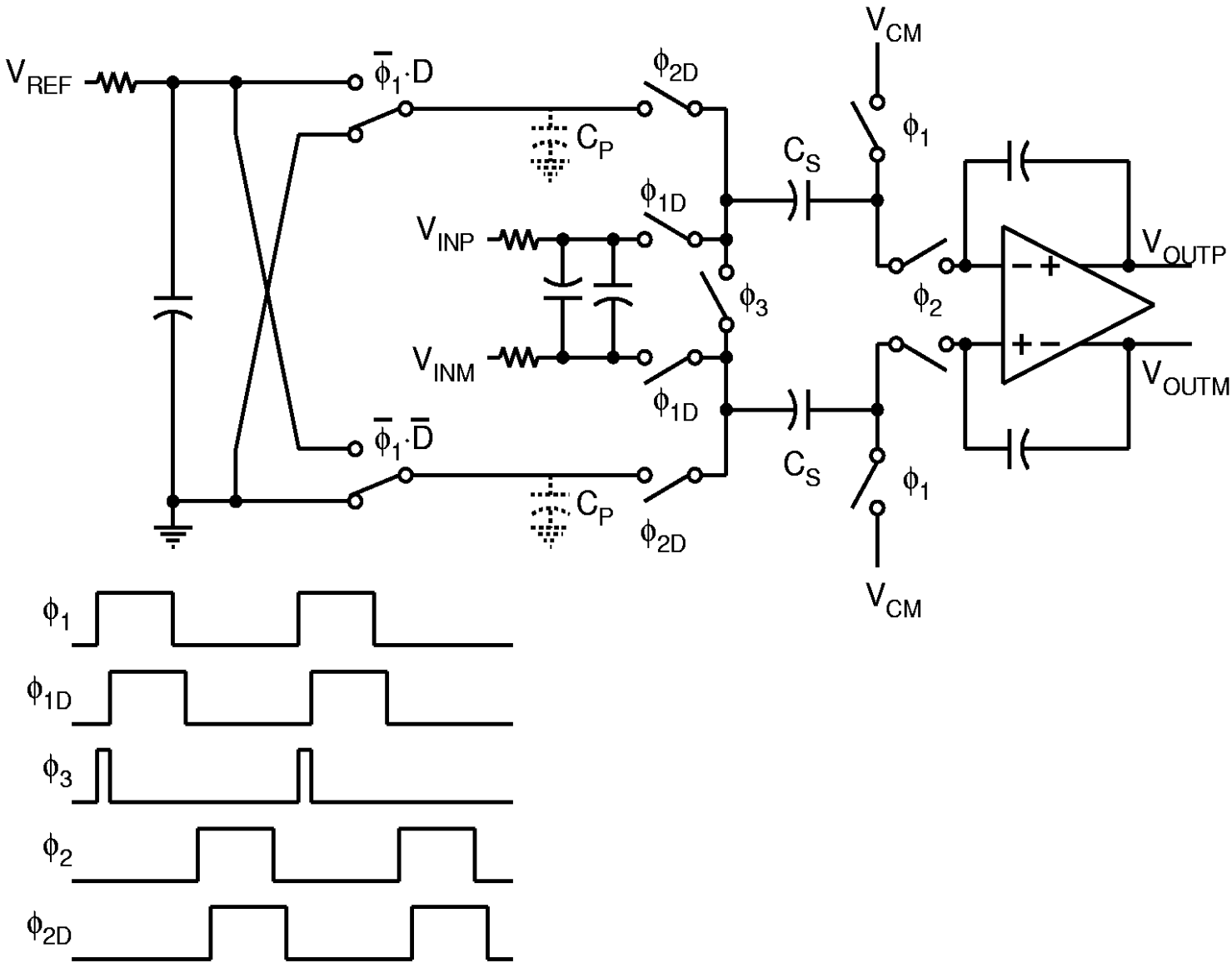


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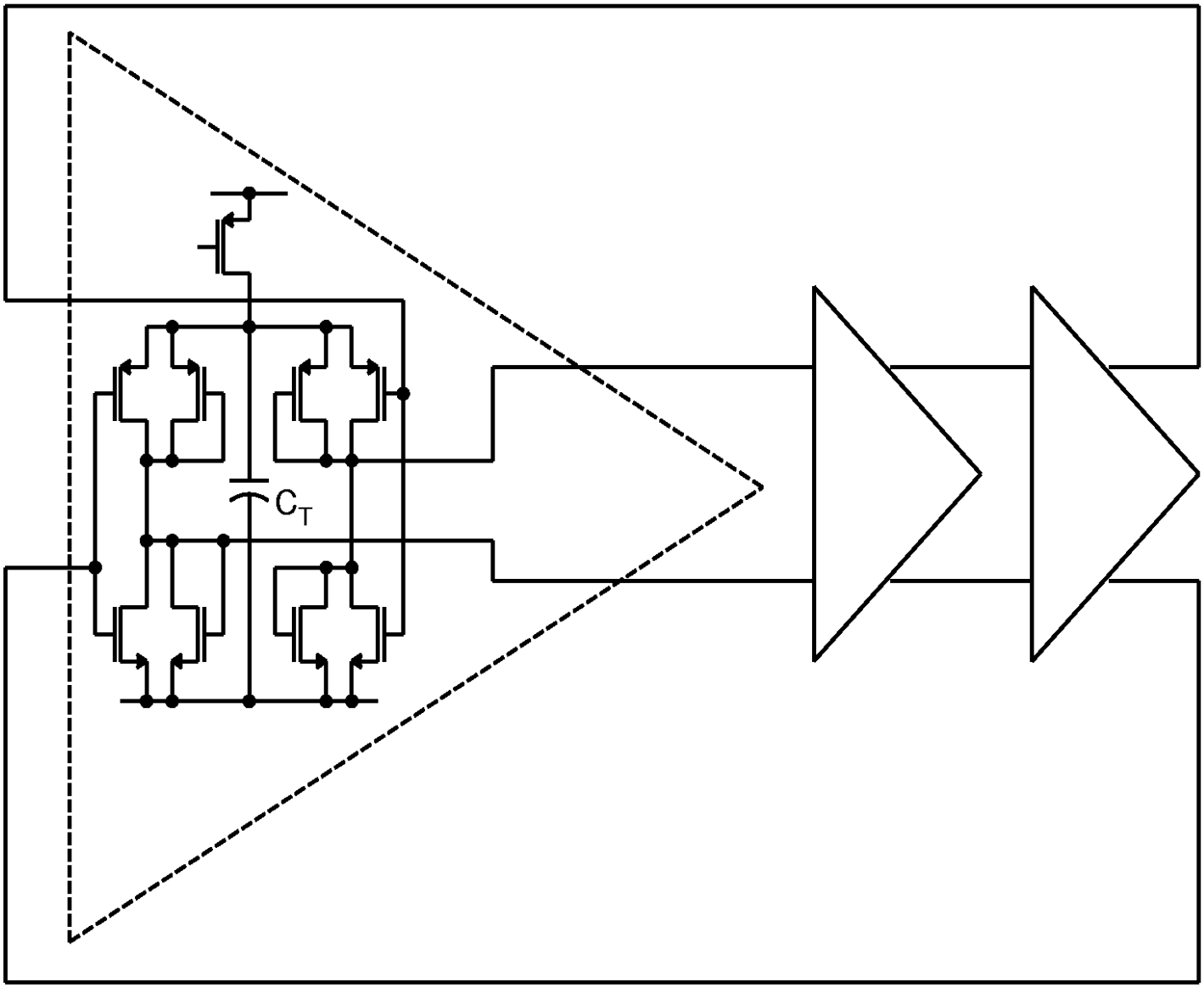


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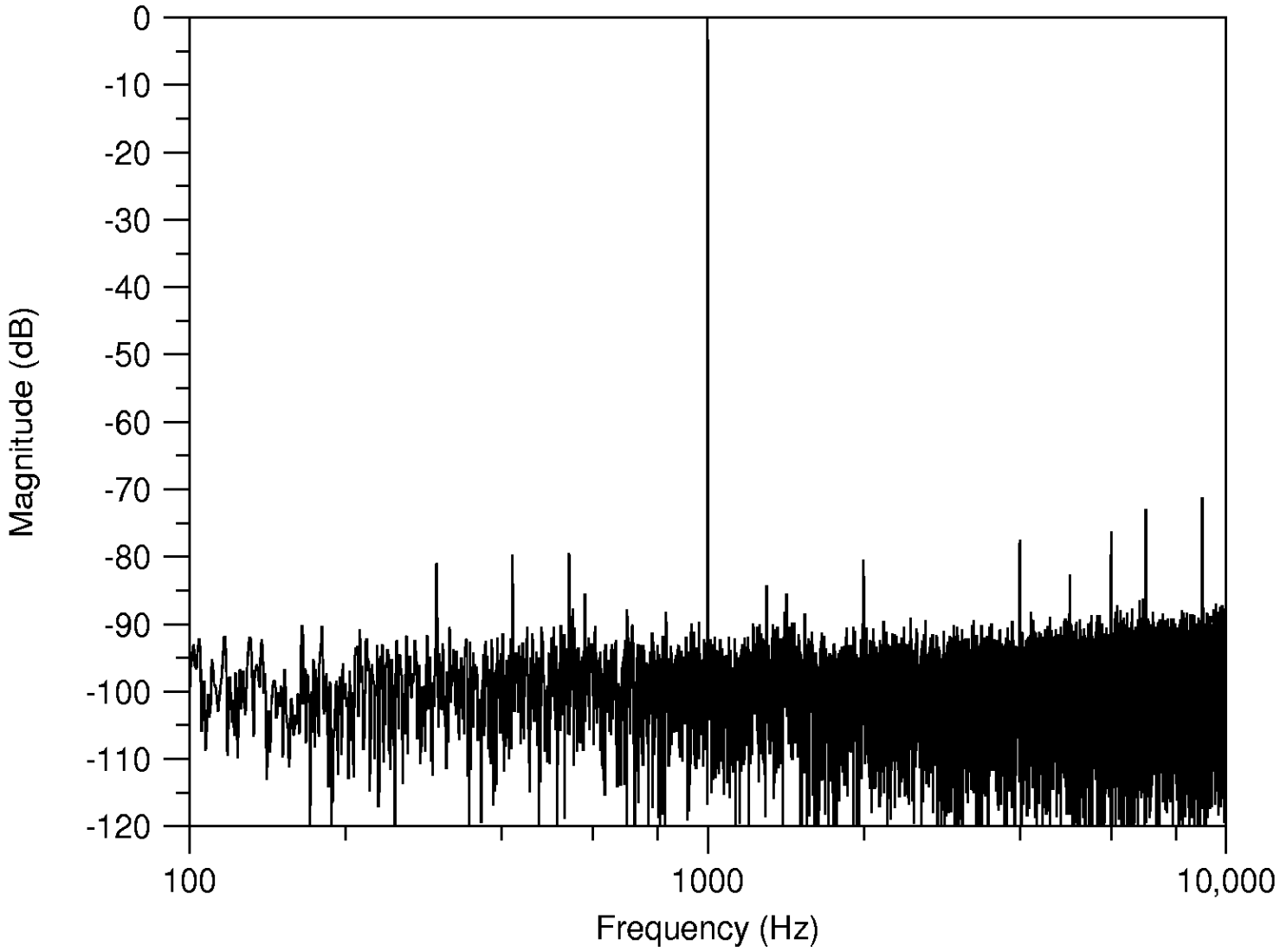


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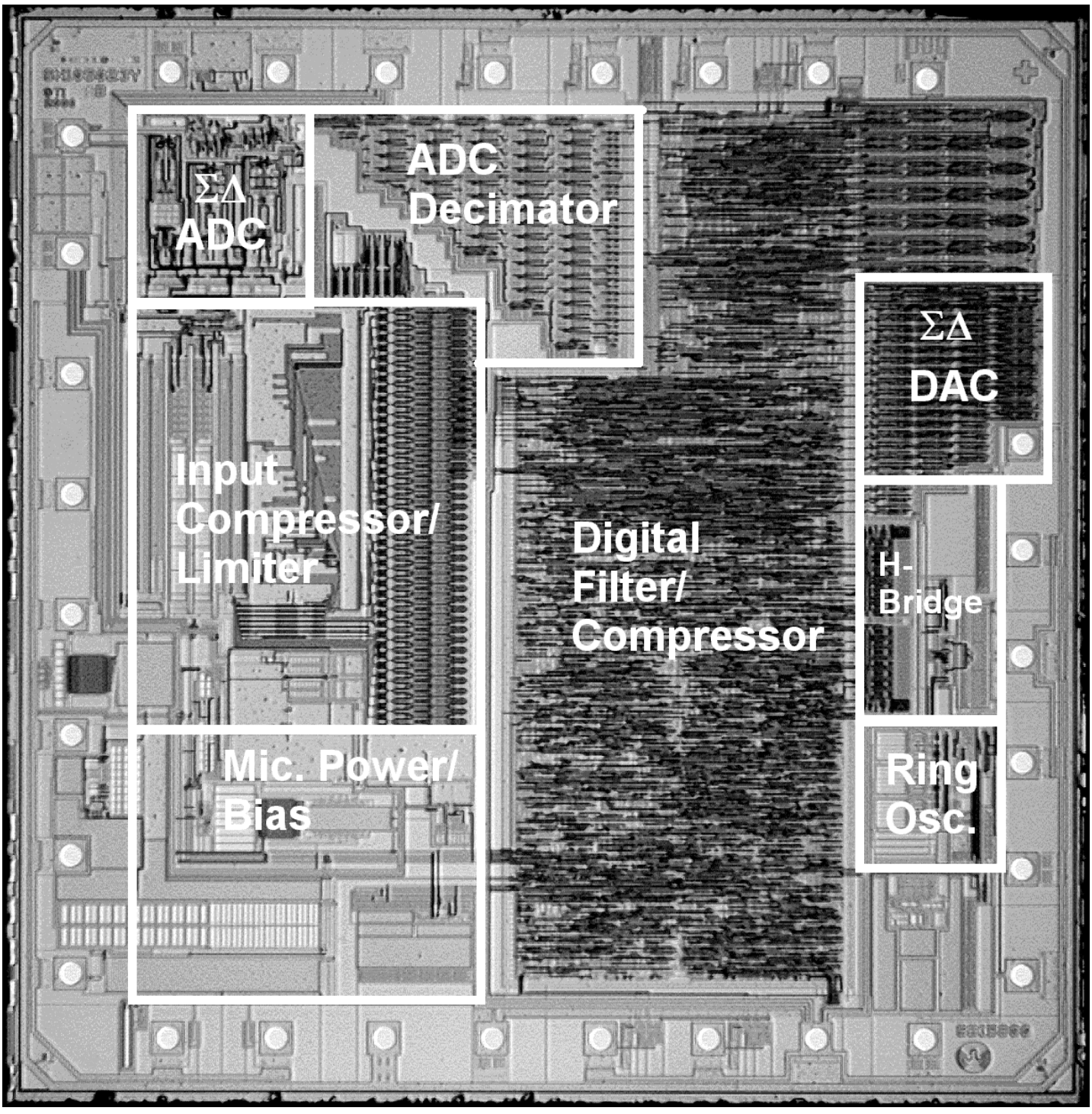


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