Design of Driver for a Digital Hearing Aid

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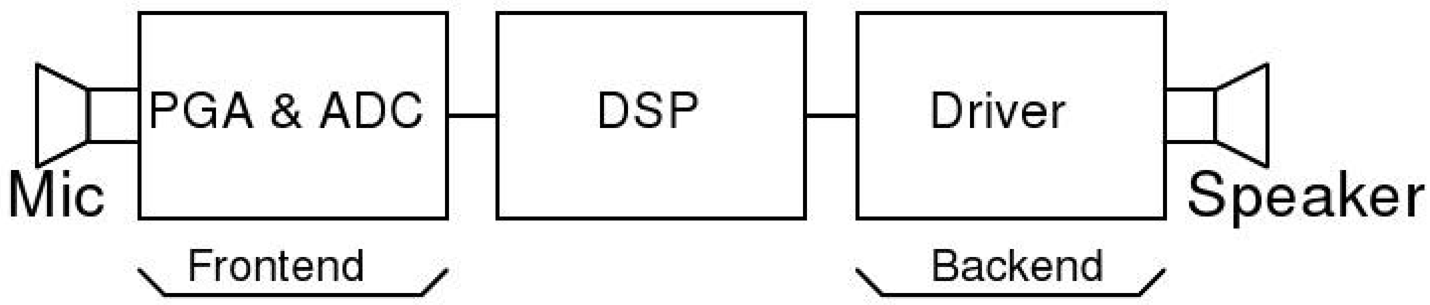
Outline

- Introduction to digital hearing aids
- Digital portion
- Analog portion
- Performance summary

Digital hearing aid

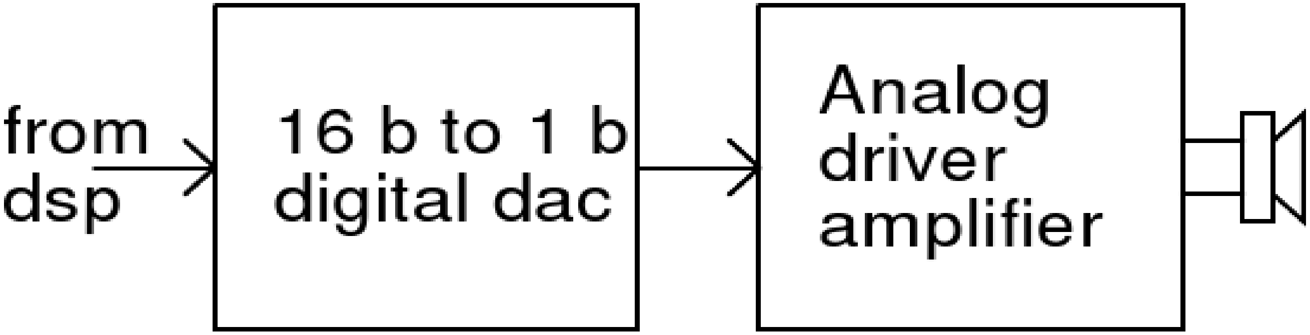


- Frontend converts analog input to digital for further processing
- DSP processes the digital signal
- Backend drives the speaker using DSP's output

Target Specifications

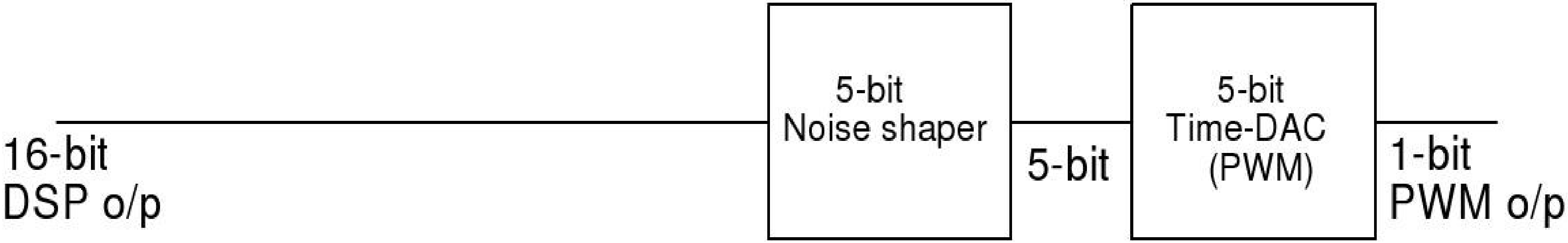
- SNR > 95 dB
- THD > -70 dB
- O/p Thermal noise < 12 micro V rms
- Minimal power consumption

Backend driver



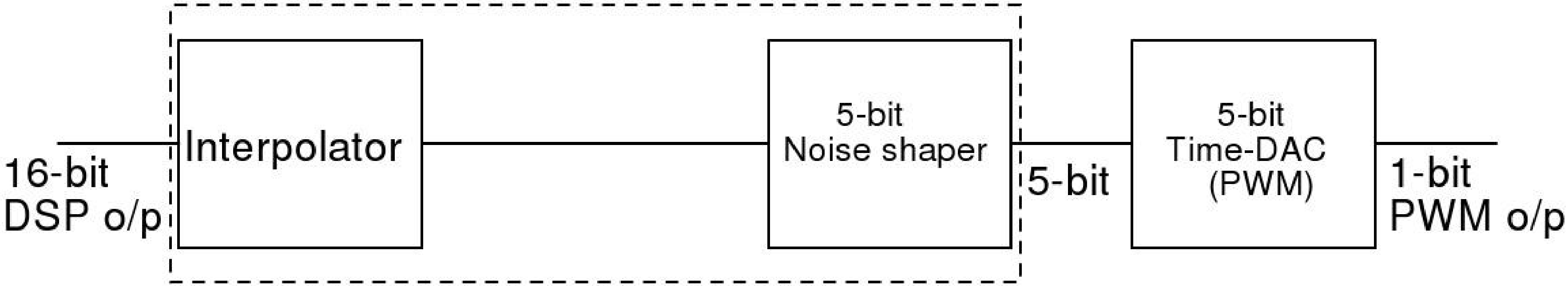
- DSP outputs a 16-bit signal
- Speaker requires analog signal as input

Digital DAC



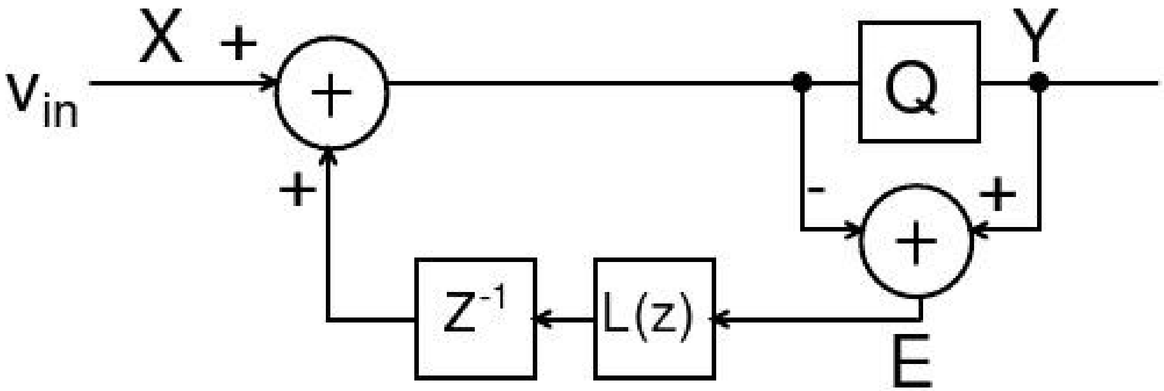
- 16-bit to 1-bit conversion in 2 steps
- Digital Delta Sigma(DDS) used for noise shaper
- 5-bit DDS o/p mapped into pulse widths

Digital Noise Shaper (DDS)



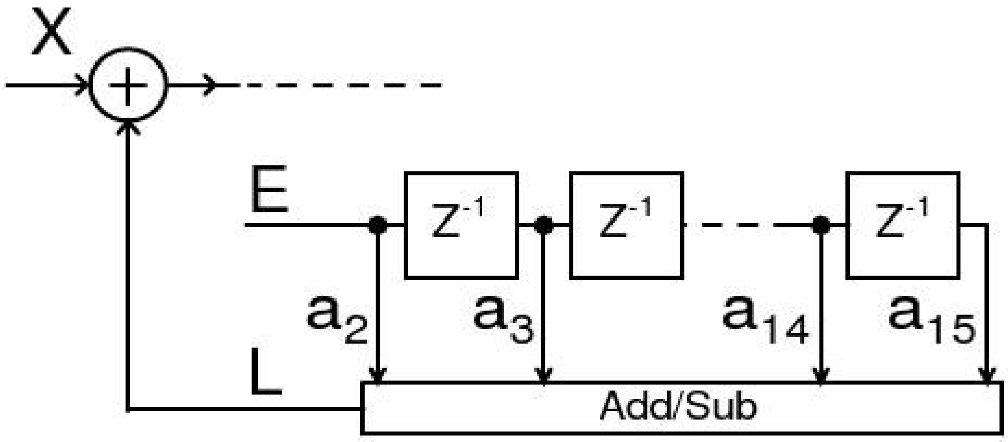
- From MATLAB simulations, an OSR of 32 and a 5-bit internal quantizer was chosen
- DSP o/p is a 40 kHz PCM signal
- Hence a 16x interpolator is used

DDS-Architecture



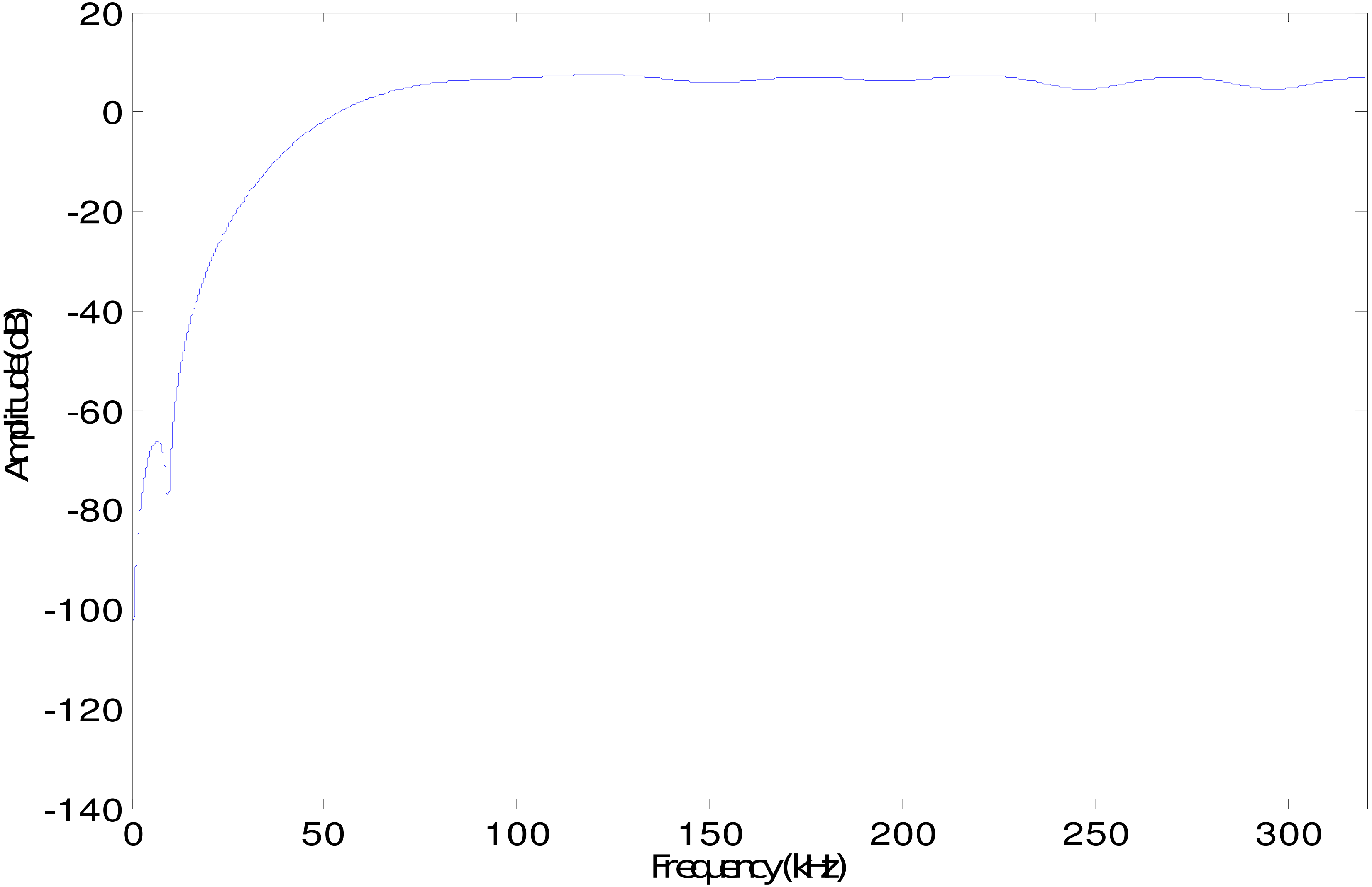
- An error feedback architecture is adopted
- $Y(z) = X(z) + [1+(z^{-1})L(z)]E(z)$
- The coefficient of E(z) is NTF(z)
- L(z) = z[NTF(z)-1]. If NTF is FIR, so is L.

DDS-Loop filter

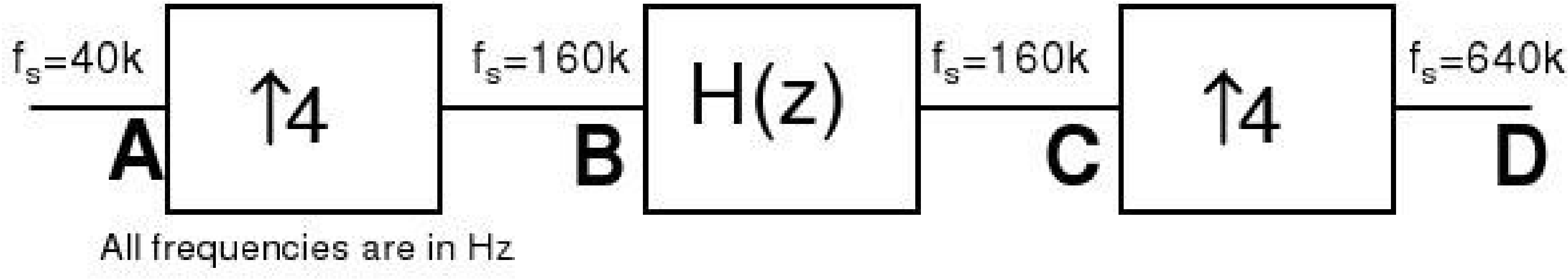


- A 15th order FIR-NTF is used
- Hence a 14-tap loop filter

DDS-NTF Frequency response

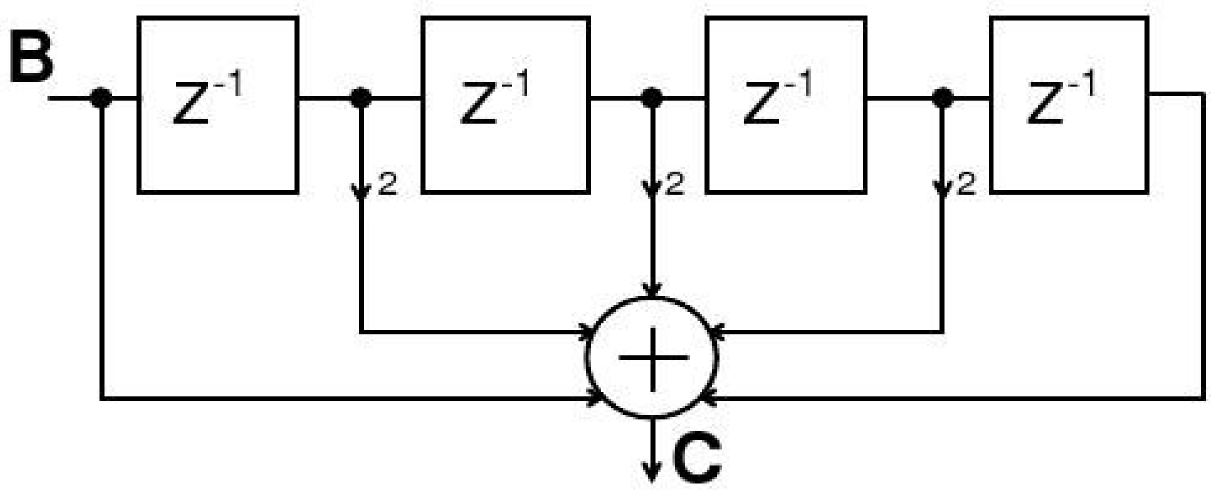


Interpolator



- Repeating the same value 4 times is cosine filtering
- In addition to above inherent filtering an explicit filter H is used

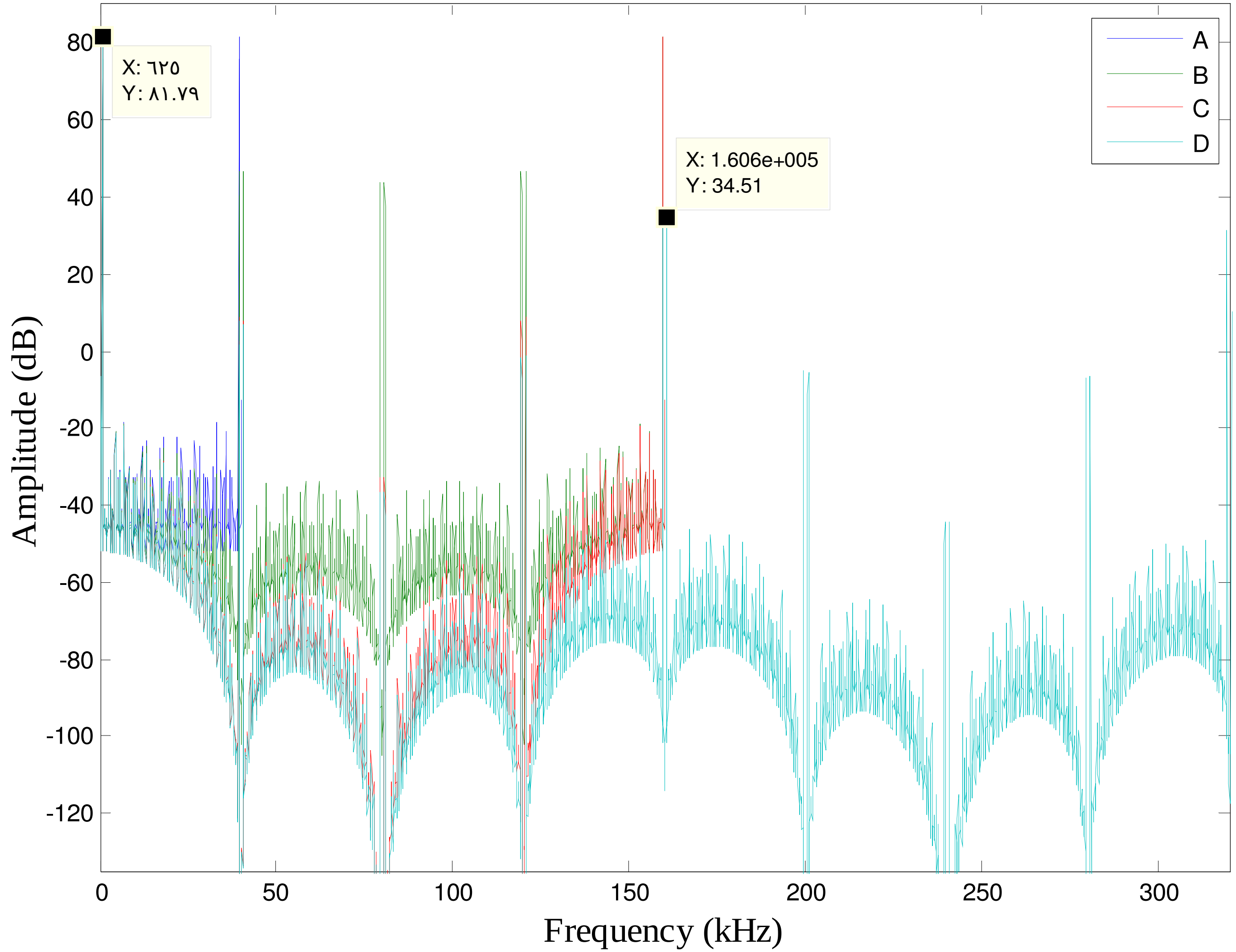
Interpolator – Filter (H)



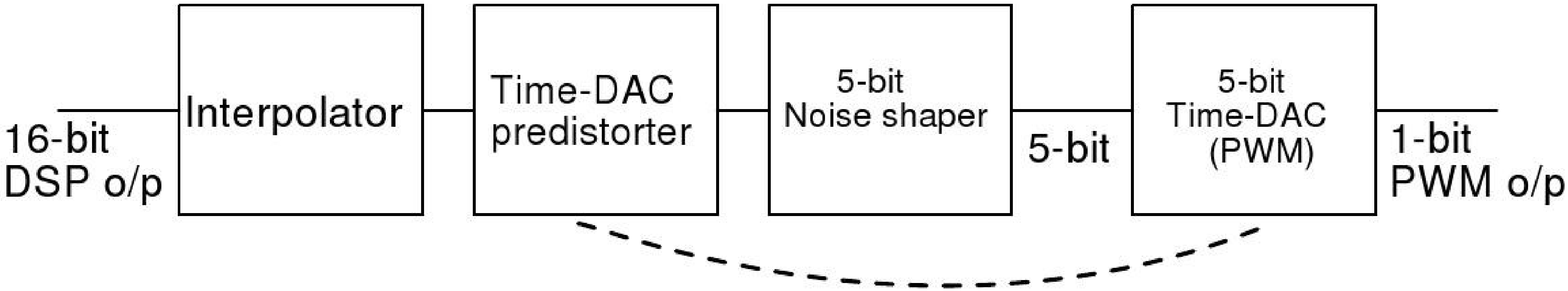
$$H_1(z) = 1 + 2Z^{-1} + 2Z^{-2} + 2Z^{-3} + Z^{-4}$$

- A simple low-pass FIR filter is used
- Has notch at 0.5fs(80 kHz) and 0.25fs(40 kHz)

Interpolator-Spectrum

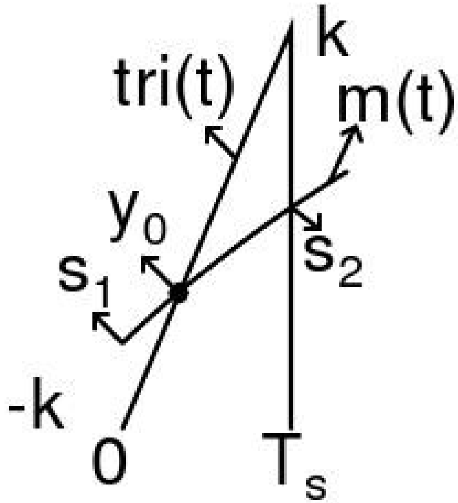


Predistortion – Time DAC



- To accurately represent a sine wave(or any signal) in PWM format, there are only 2 ways; comparing it with a triangle or a sawtooth
- Blind mapping of amplitude to time leads to signal distortion
- A predistorter emulates the comparison process

Predistorter- Algorithm



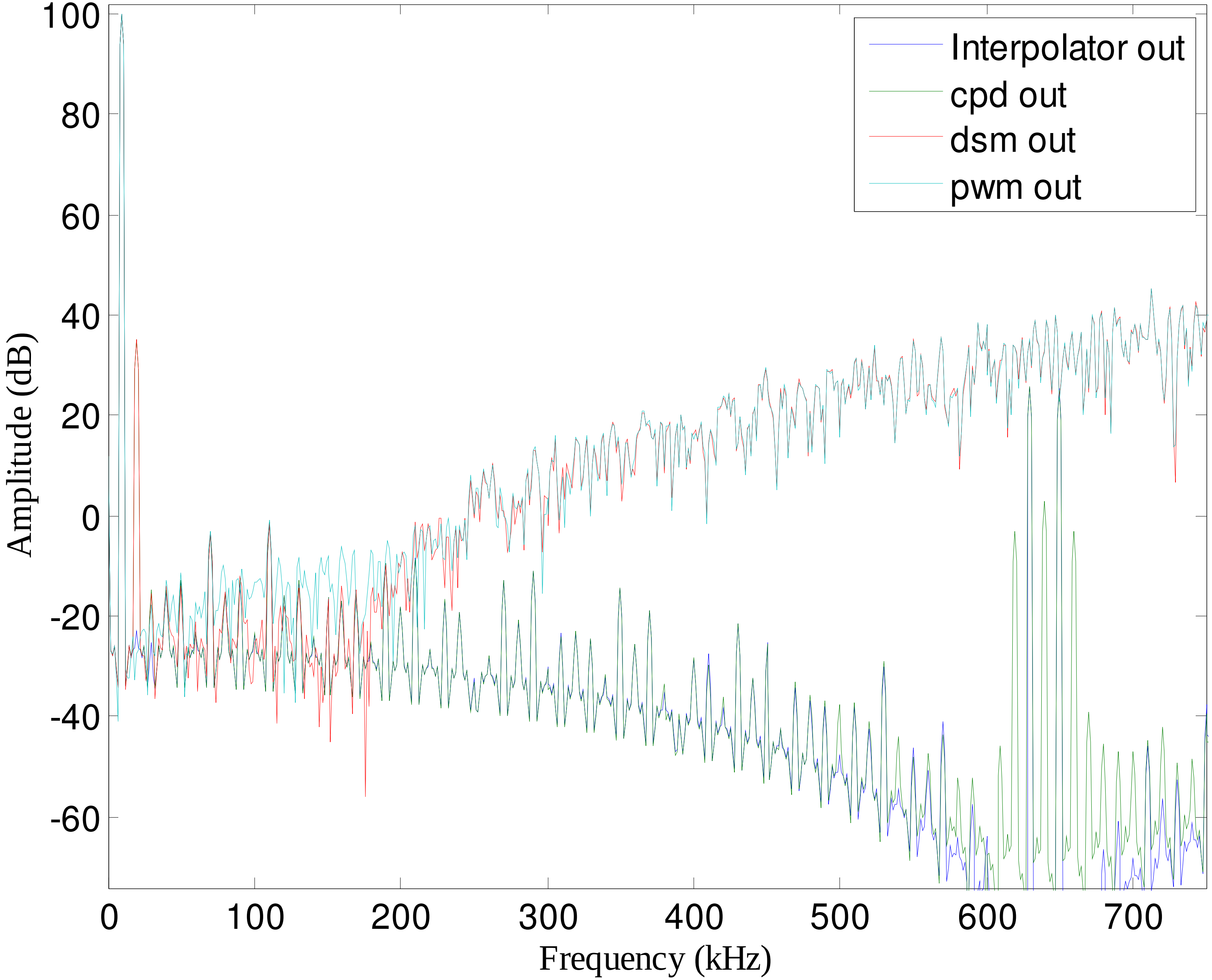
$$y_0 = \frac{k(s_1+s_2)}{2k+s_1-s_2}$$

$$\approx \frac{1}{4k}(s_1+s_2)(2k-s_1+s_2)$$

s_1, s_2 are sampled message amplitudes

- All the calculations gets implemented digitally
- Sawtooth carrier is used for both simplicity and to prevent foldback

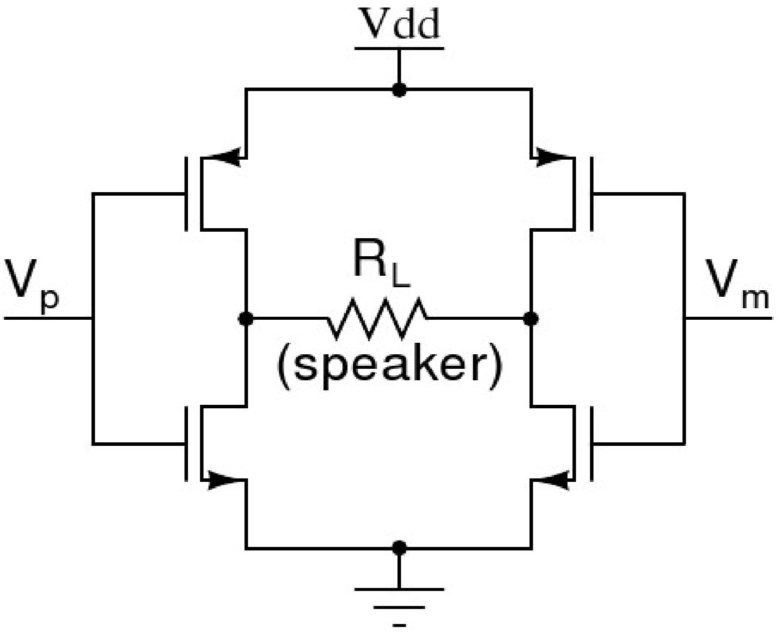
Digital DAC – output spectrum



Digital DAC – Performance summary

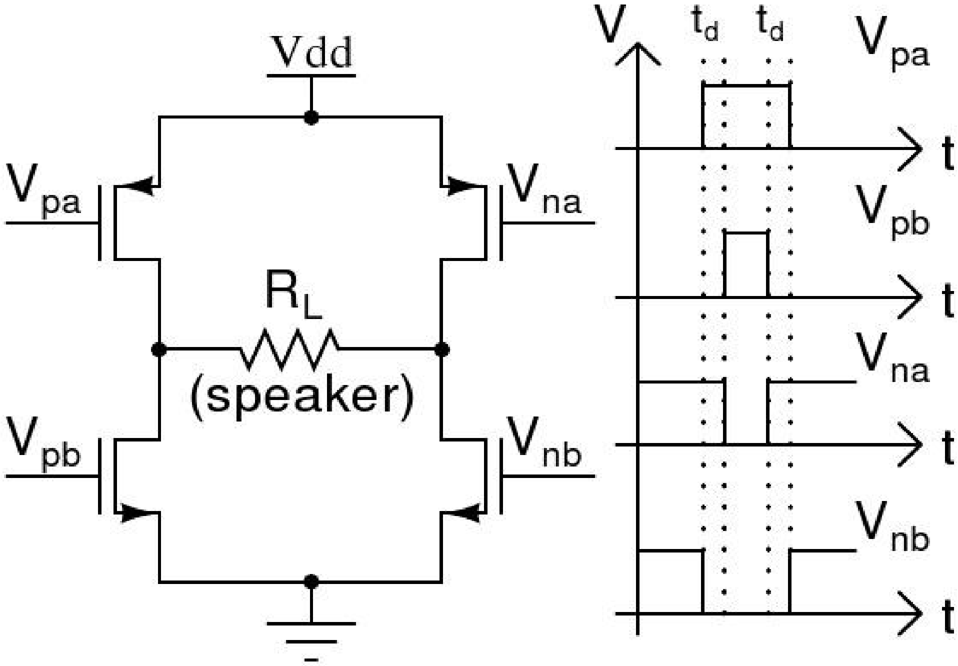
- Area: 250 um x 250 um
- Power
  - Interpolator - 17 %
  - Algorithm - 7 %
  - Noise shaper- 32 %
  - Time-DAC - 38 %
- SNDR = 95.662 dB
- THD = -102.225 dB

Analog driver amplifier



- Class D principle- good efficiency
- Vp,Vm are PWM input signals (digital DAC o/p)

H-Bridge driver

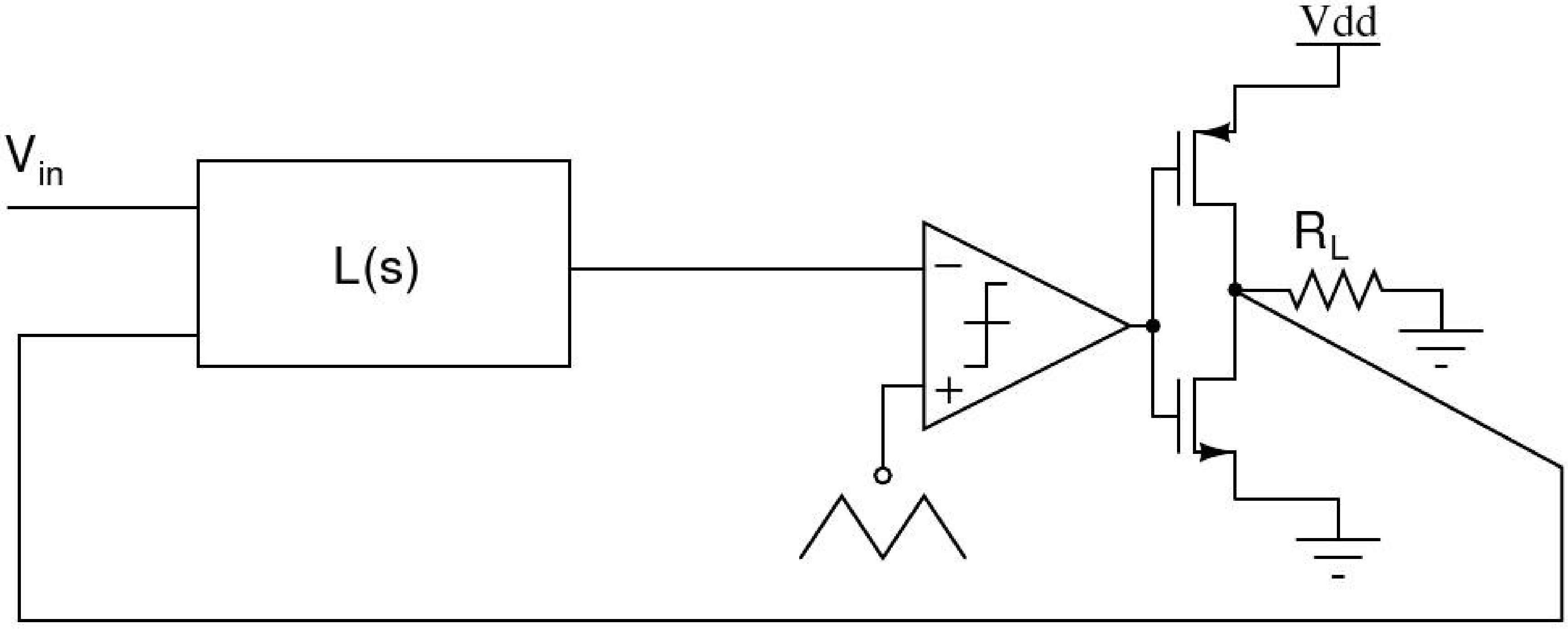


- I/p PWM signal must be non-overlapping to prevent supply shoot-through
- The actual speaker acts as a low-pass filter

Known problems with open loop

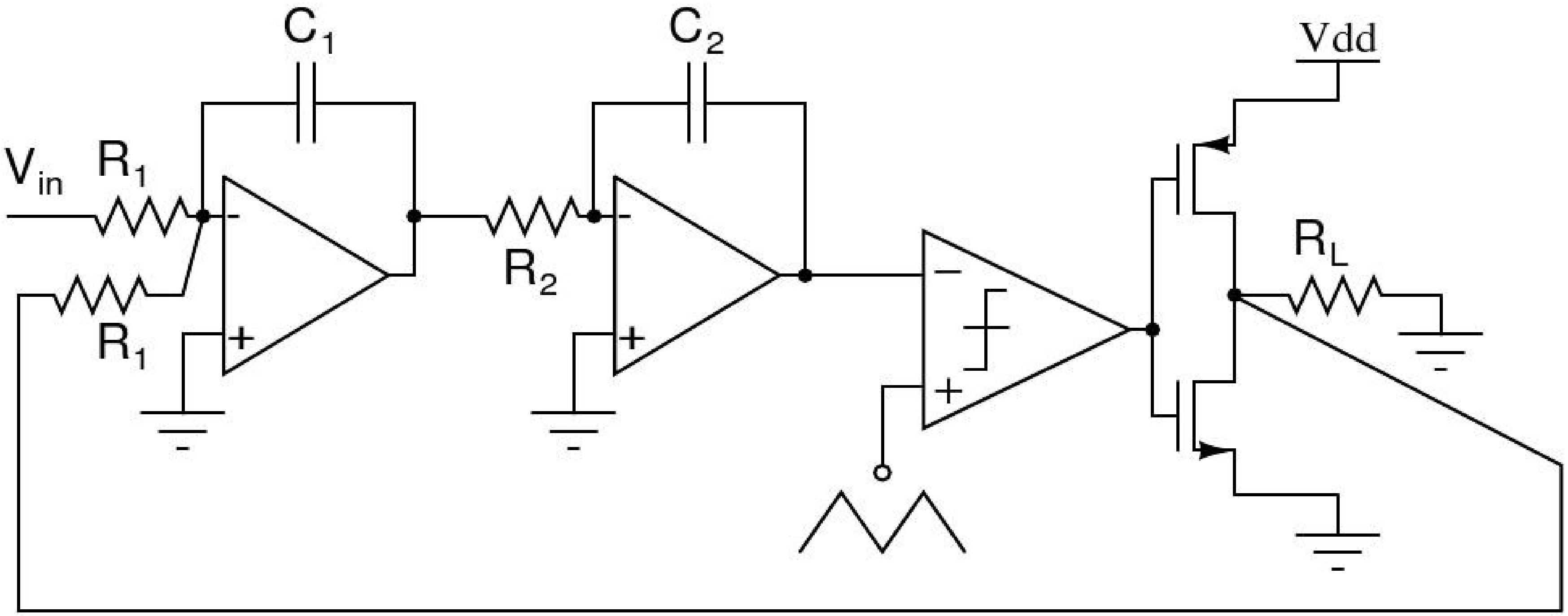
- Power supply noise modulates directly with the input signal
- Non-overlap-time non-linearities
- Finite rise and fall times of H-bridge
- Nonlinear triangular carrier generation
- Comparator offsets
- Load dependence

Forming a closed loop driver



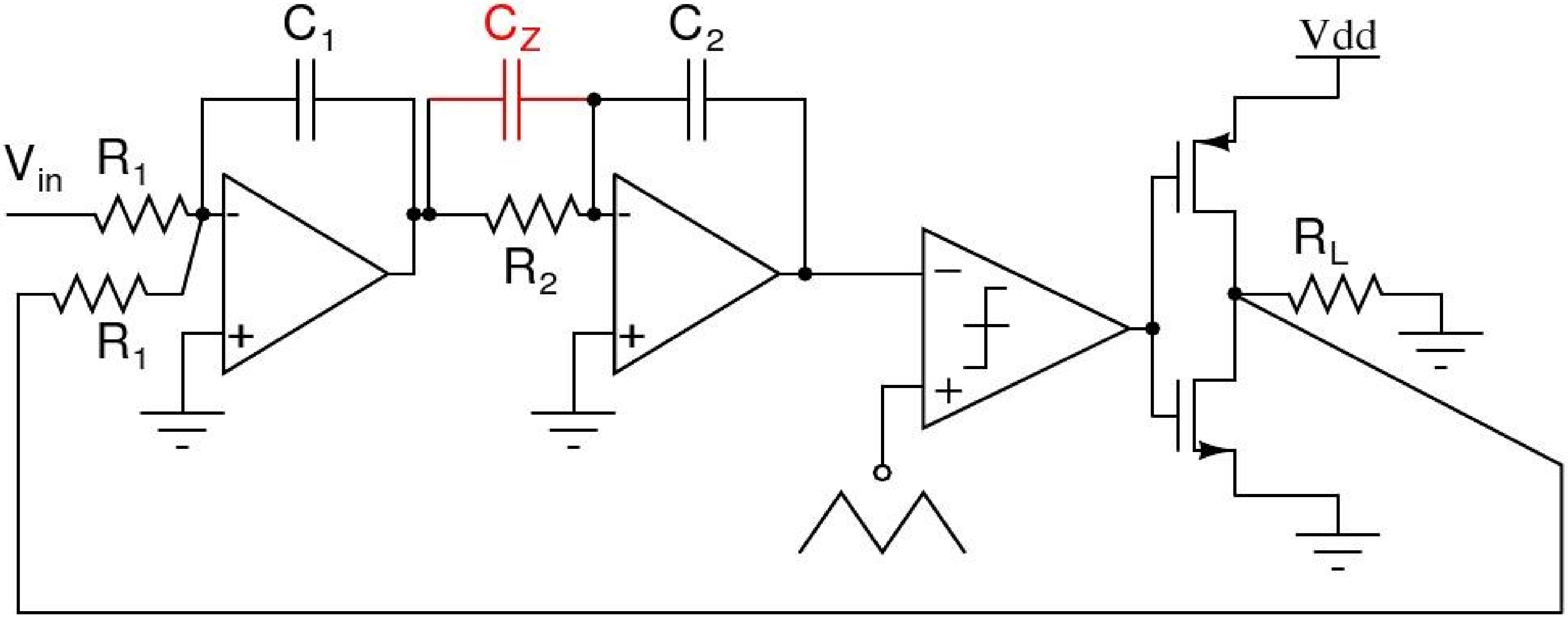
- Single ended version illustrated for compactness
- Vin is digital DAC's PWM o/p
- L(s) needs to be a low-pass filter

Closed loop – Loop filter

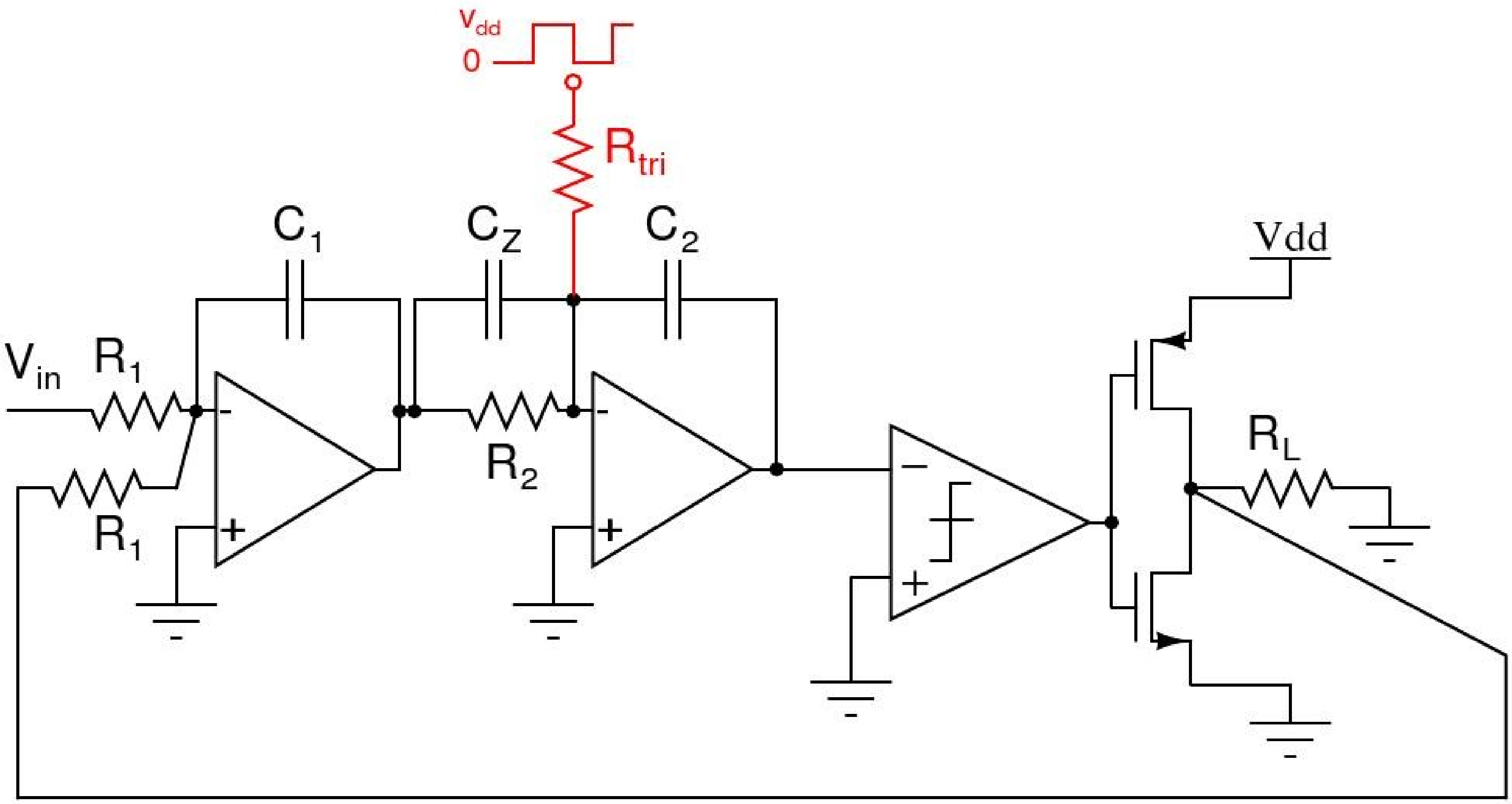


- L(s) is 2nd order integrator loop filter
- Coefficients chosen to give sufficient loop gain in signal band
- Triangular carrier chosen to be 640 kHz
- Loop's ugf fixed at 170 kHz

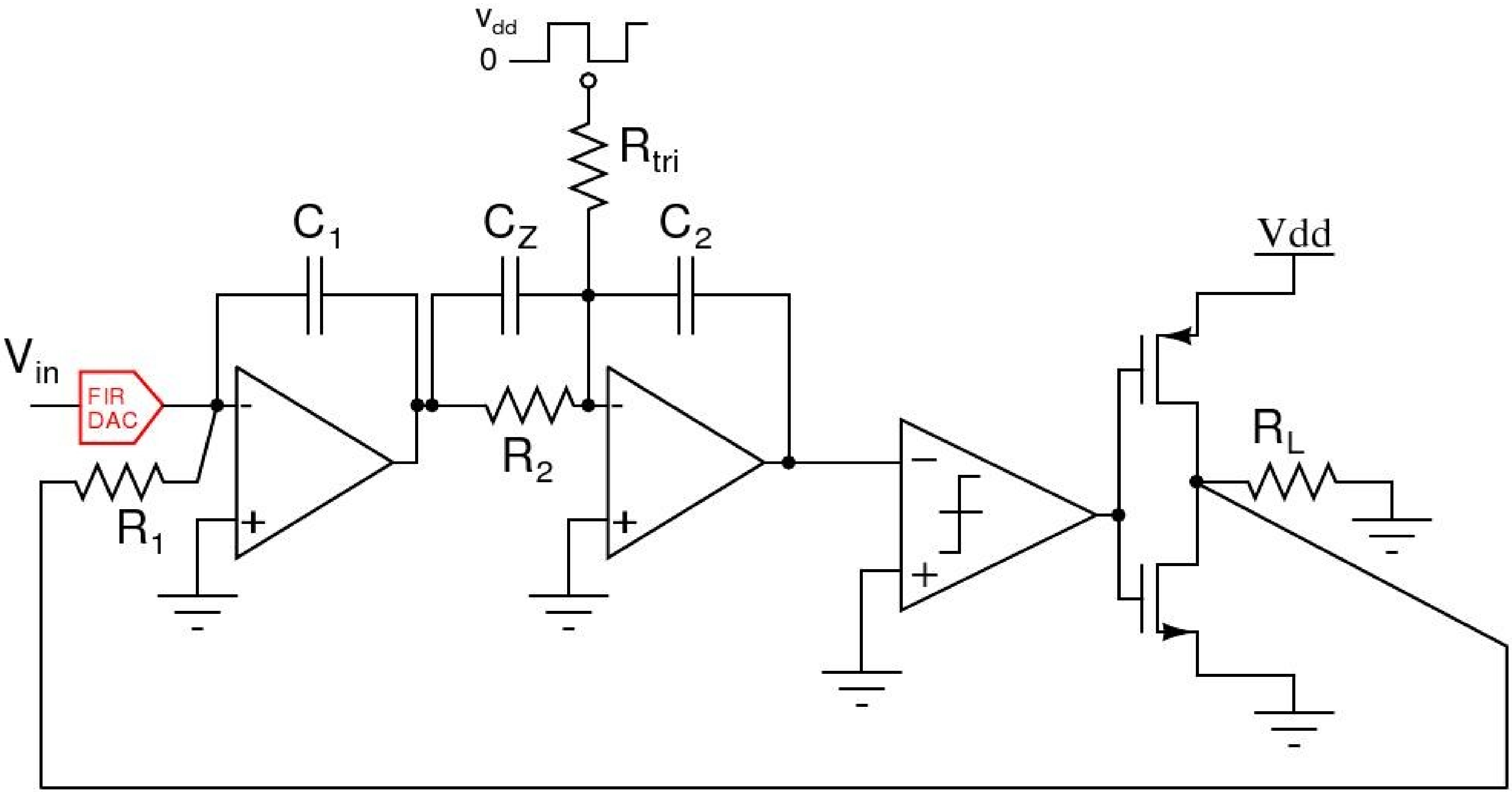
Loop- Compensation



- The loop cuts the ugf at -40 dB per decade
- Compensation achieved through Cz and C2
- Cz & C2 provides a path to bypass 2nd integrator above the Cz*R2 pole frequency

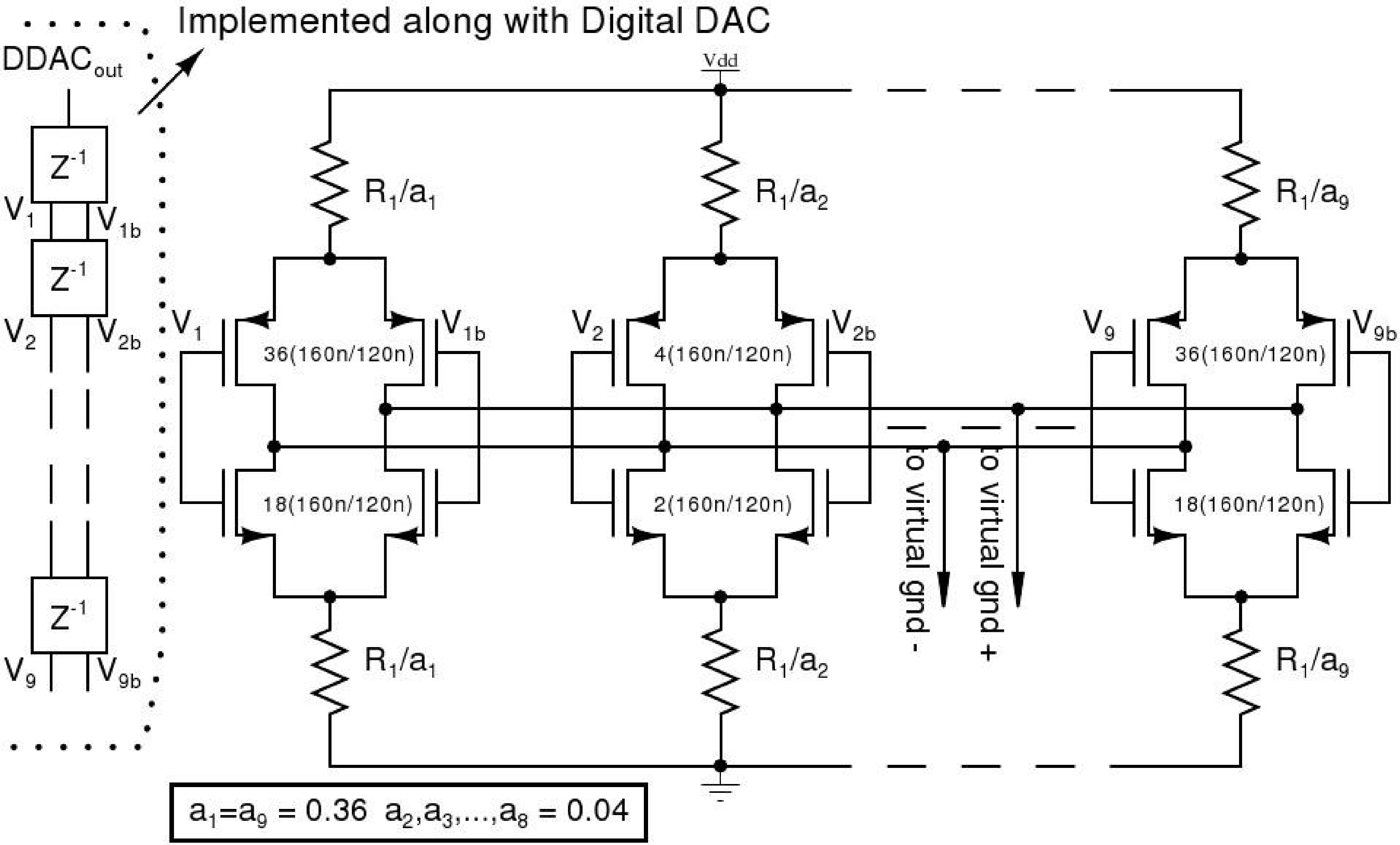


- Triangular carrier generation is done by integrating a square-wave voltage
- Rtri and C2 together decide triangle amplitude

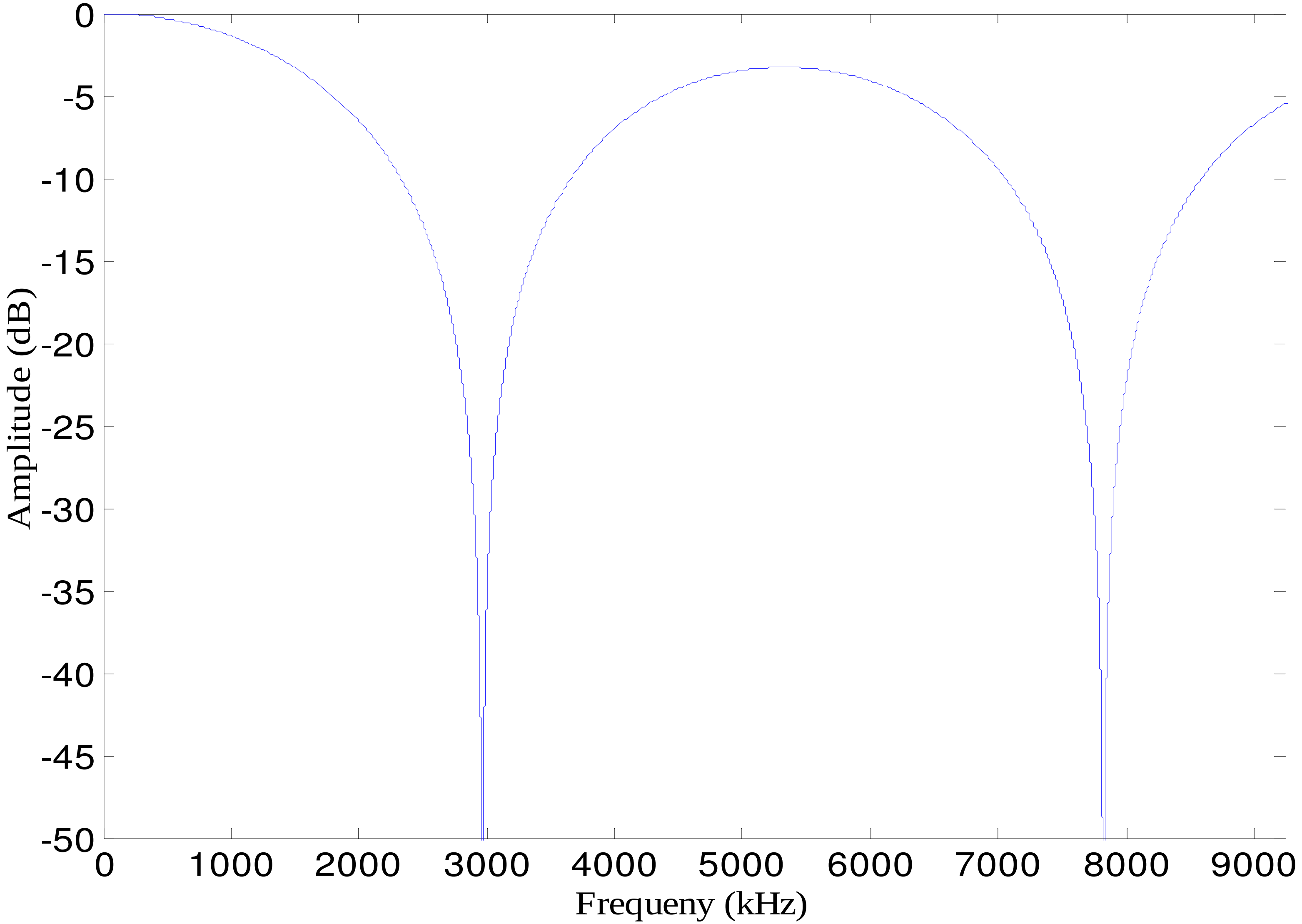


- Digital dac's o/p has large high frequency power
- Input resistor converted to an LPF
- Input resistor splitted into FIR structure
- Reduces high frequency jitter from digital clocks

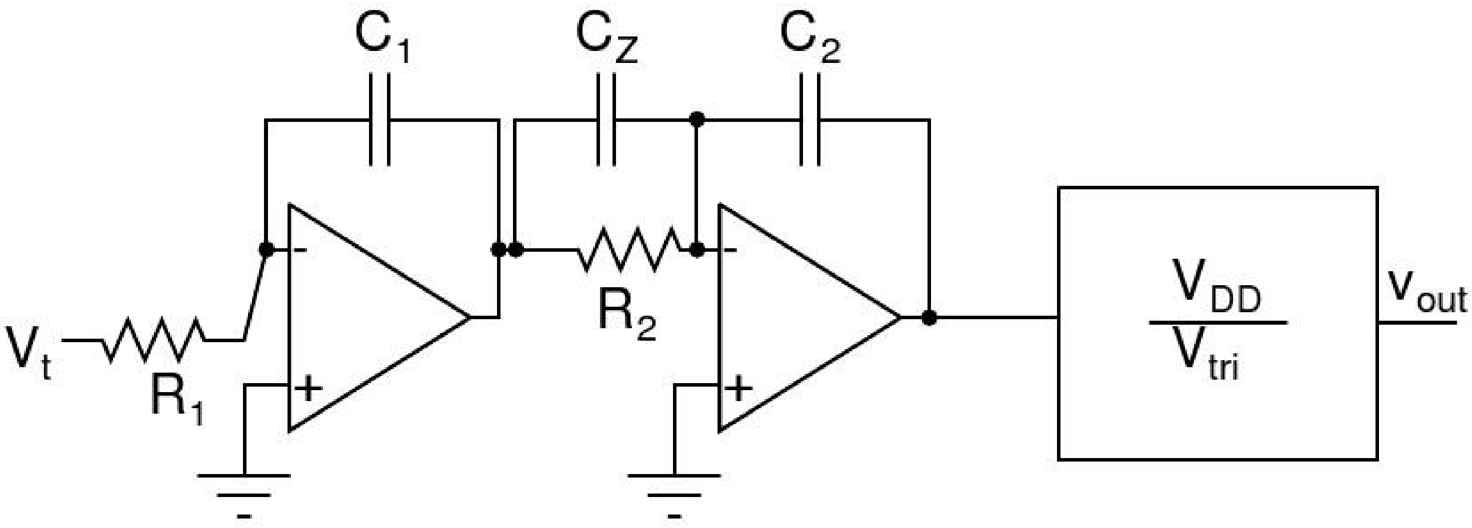
FIR-DAC Architecture



FIR-DAC frequency response

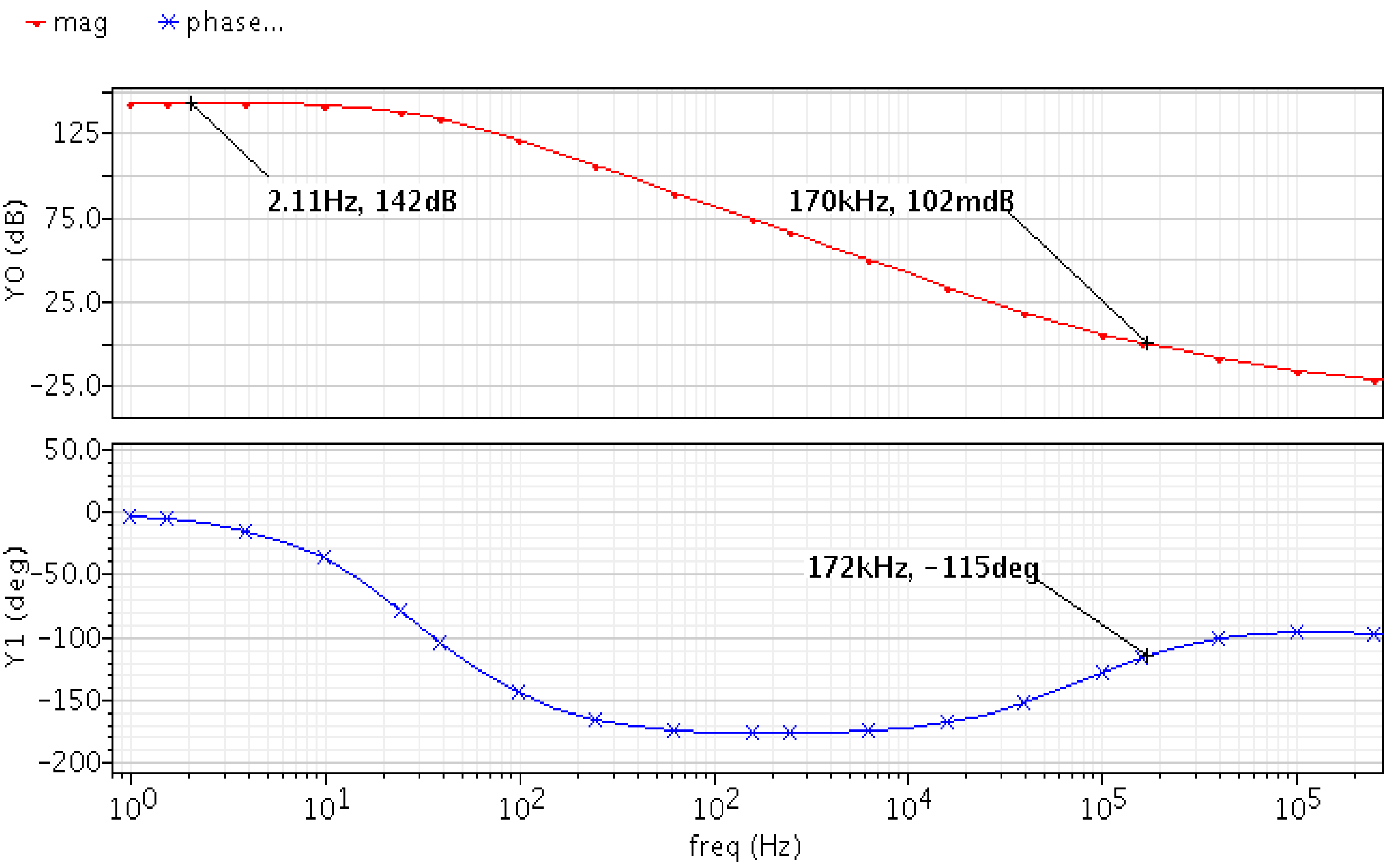


Linearizing the loop

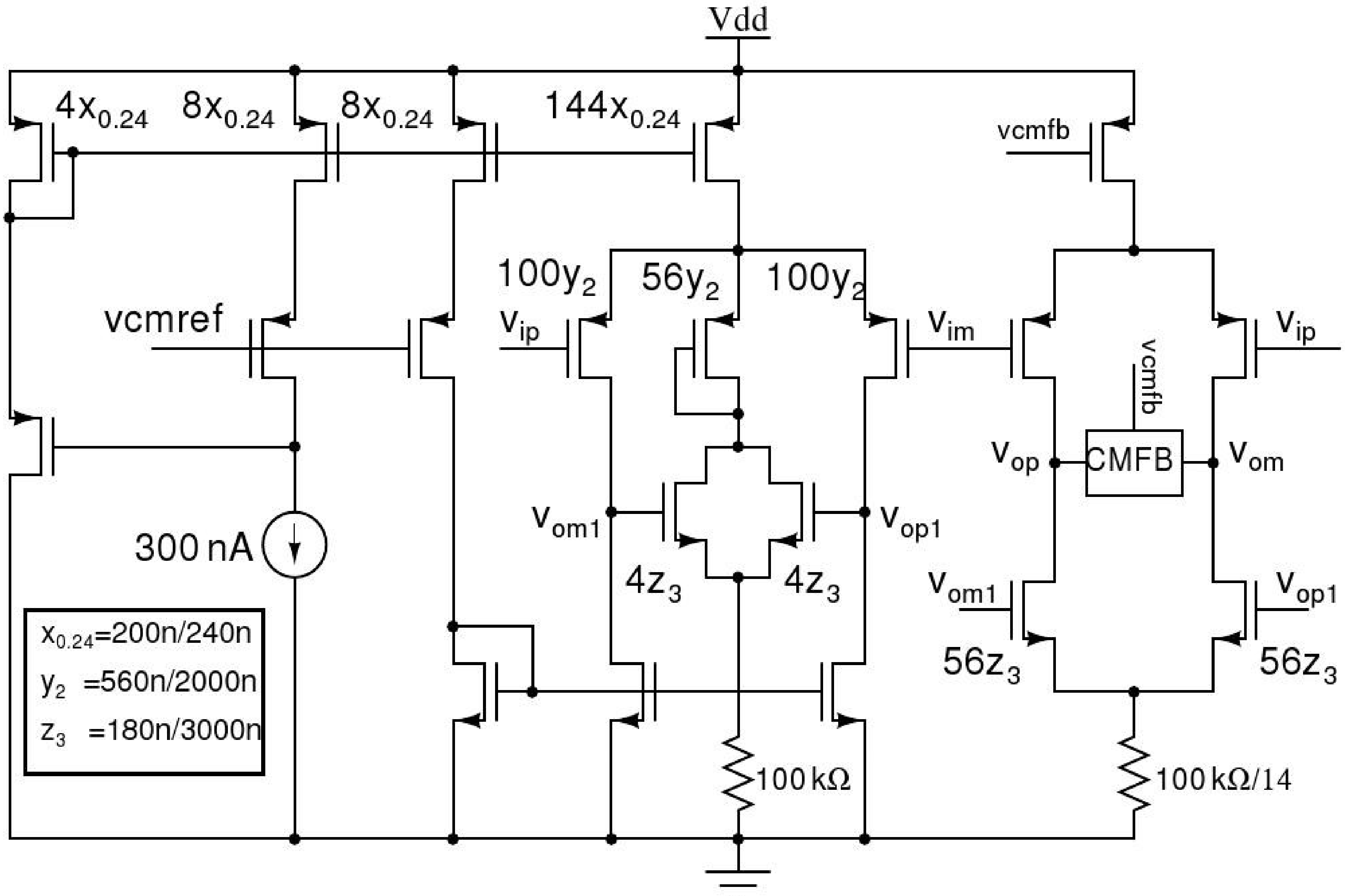


- The comparator with H-Bridge is linearized as Vdd/Vtri
- This linear model is valid at frequencies much lower than triangle frequency

Loop – frequency response



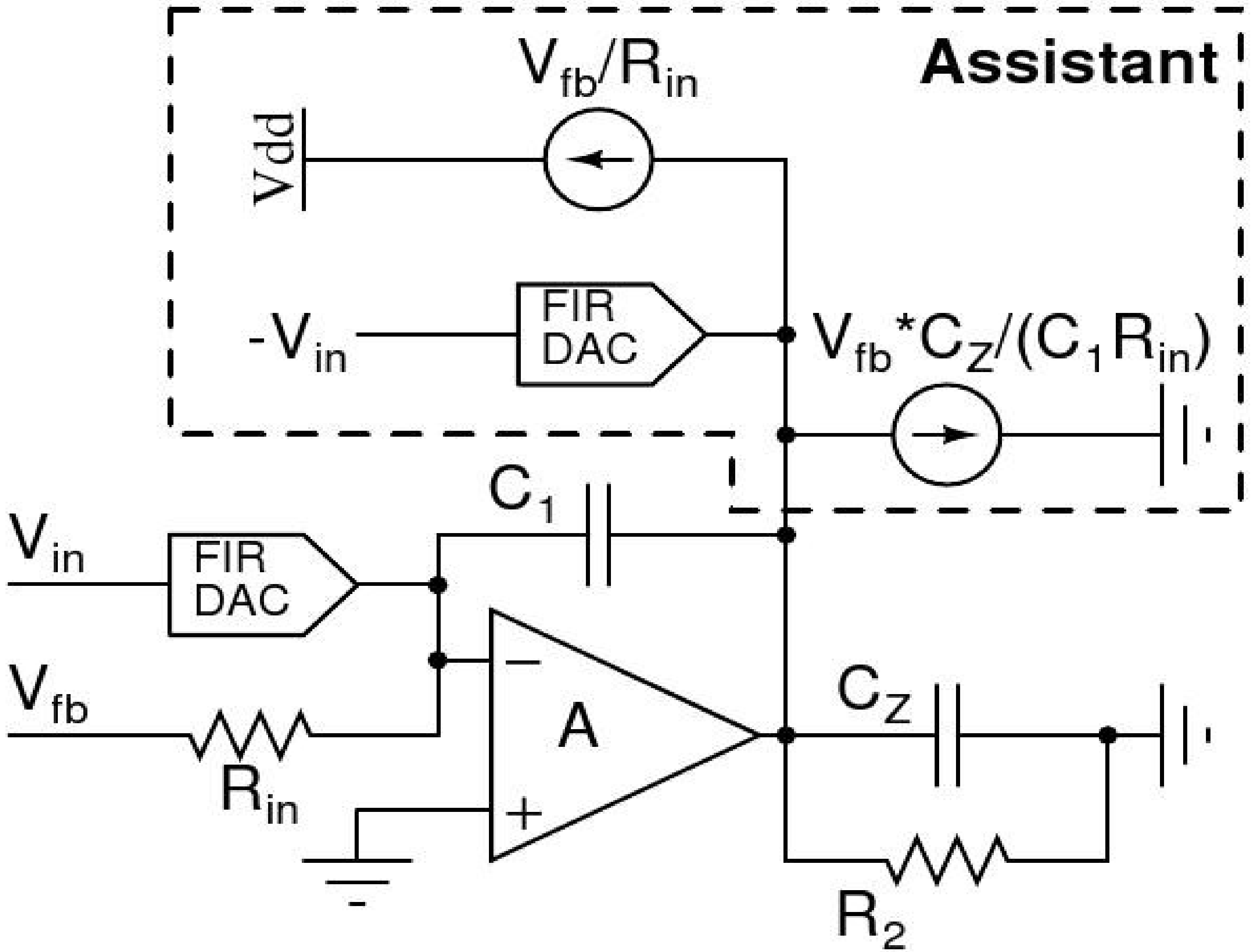
Integrator 1 - Amplifier



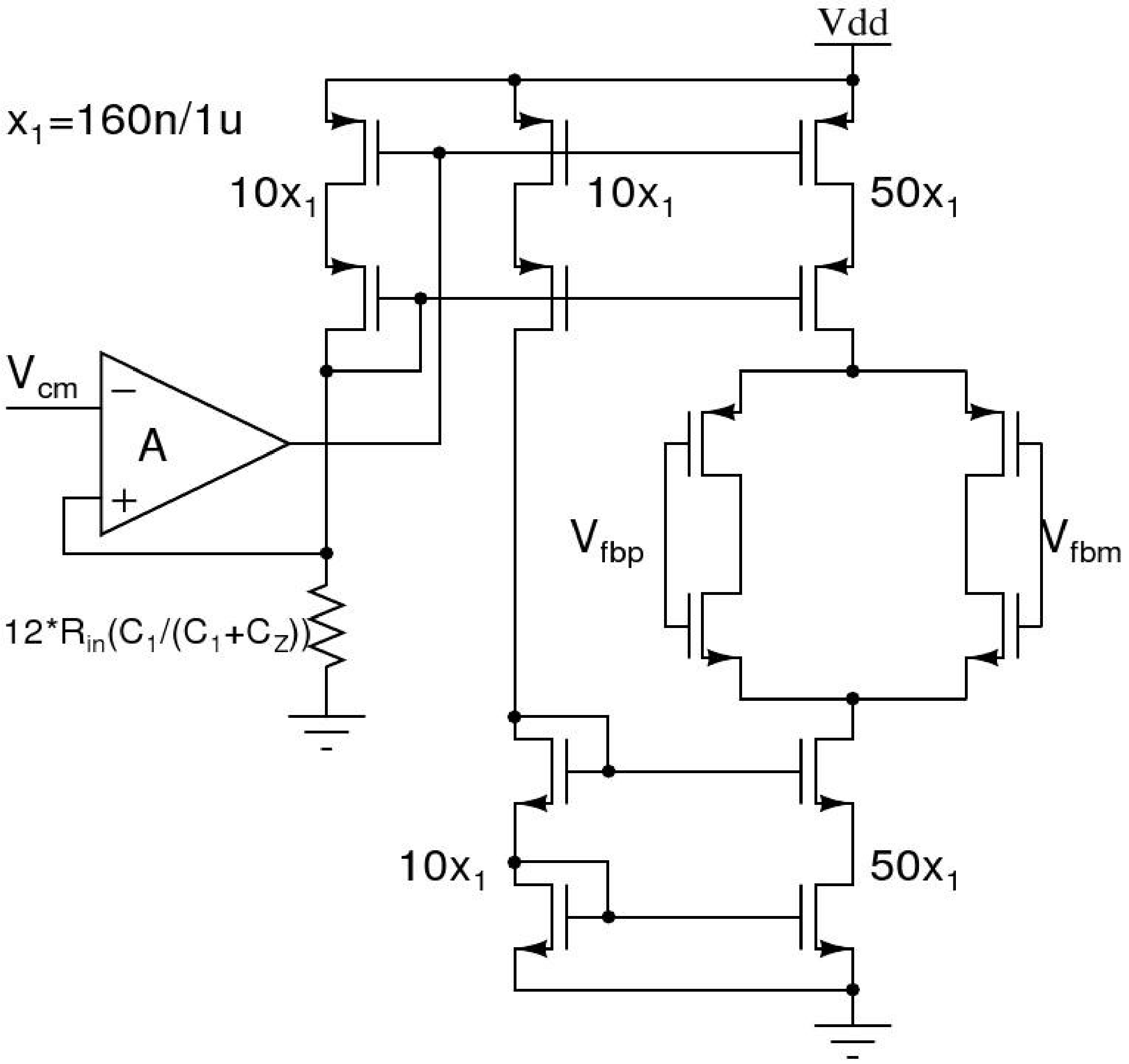
Improving linearity

- The output signal current to input signal voltage is nonlinear for a differential amplifier
- By making the output signal current 0, the input signal becomes 0 by virtue of negative feedback and hence implies no nonlinearity
- First amplifier needs to accept both feedback DAC signal and input FIR-DAC signal currents
- An alternate source is provided to accept these currents

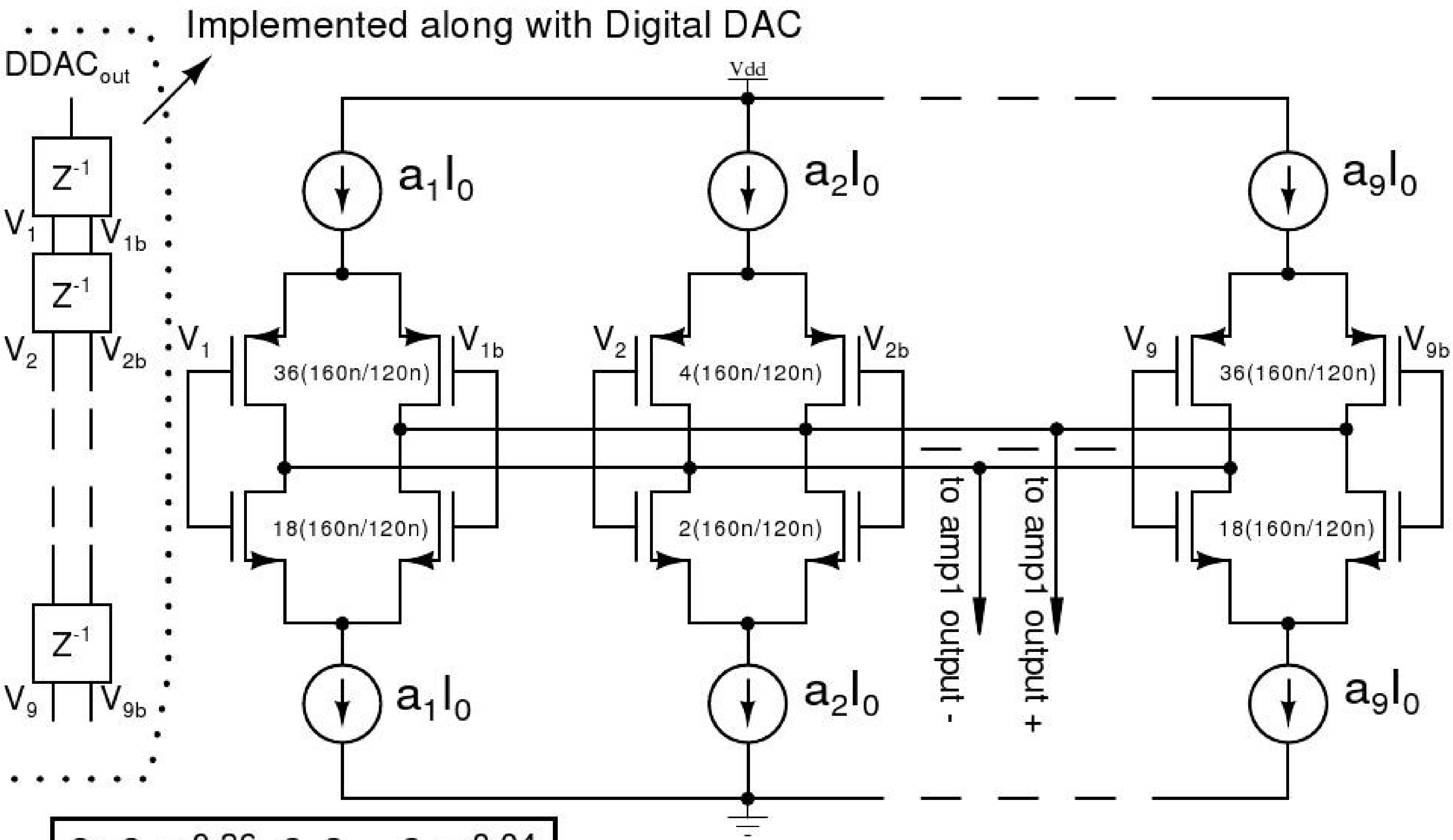
Assistant- Architecture



Assistant to feedback DAC

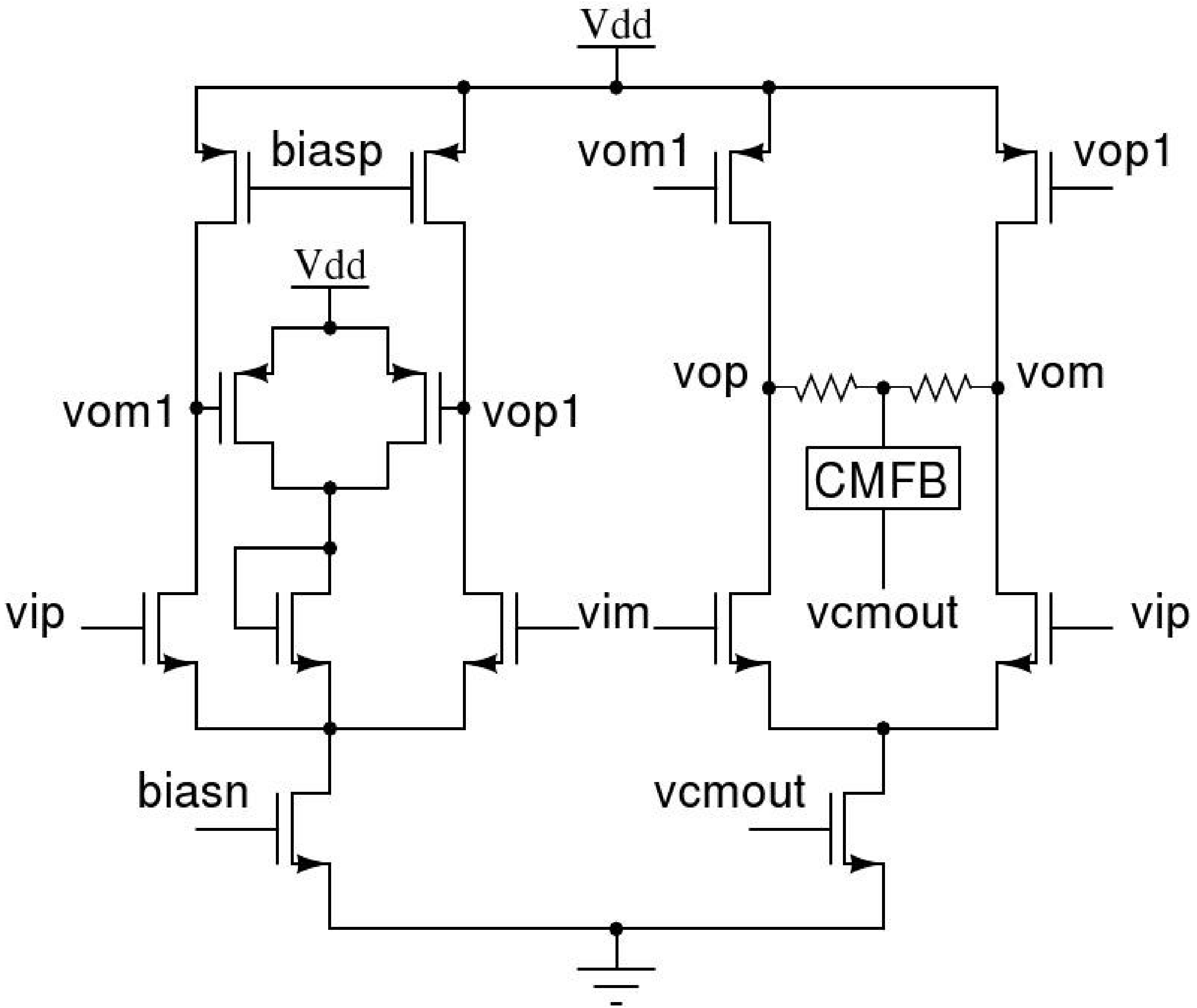


Assistant to input FIR-DAC

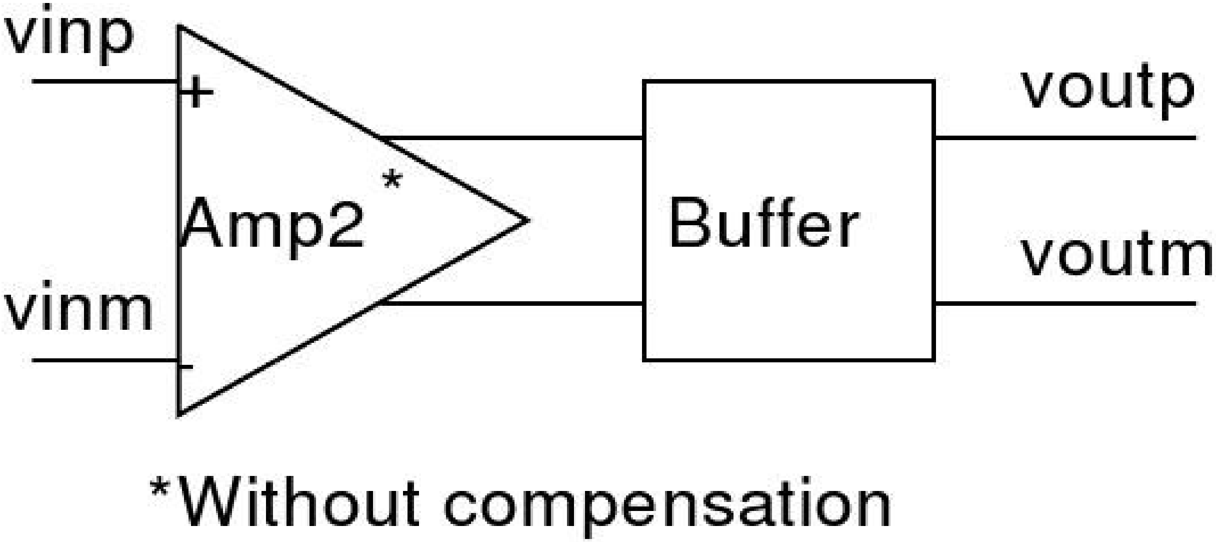


$a_1=a_9 = 0.36 \quad a_2,a_3,\ldots,a_8 = 0.04$

Integrator 2 - Amplifier

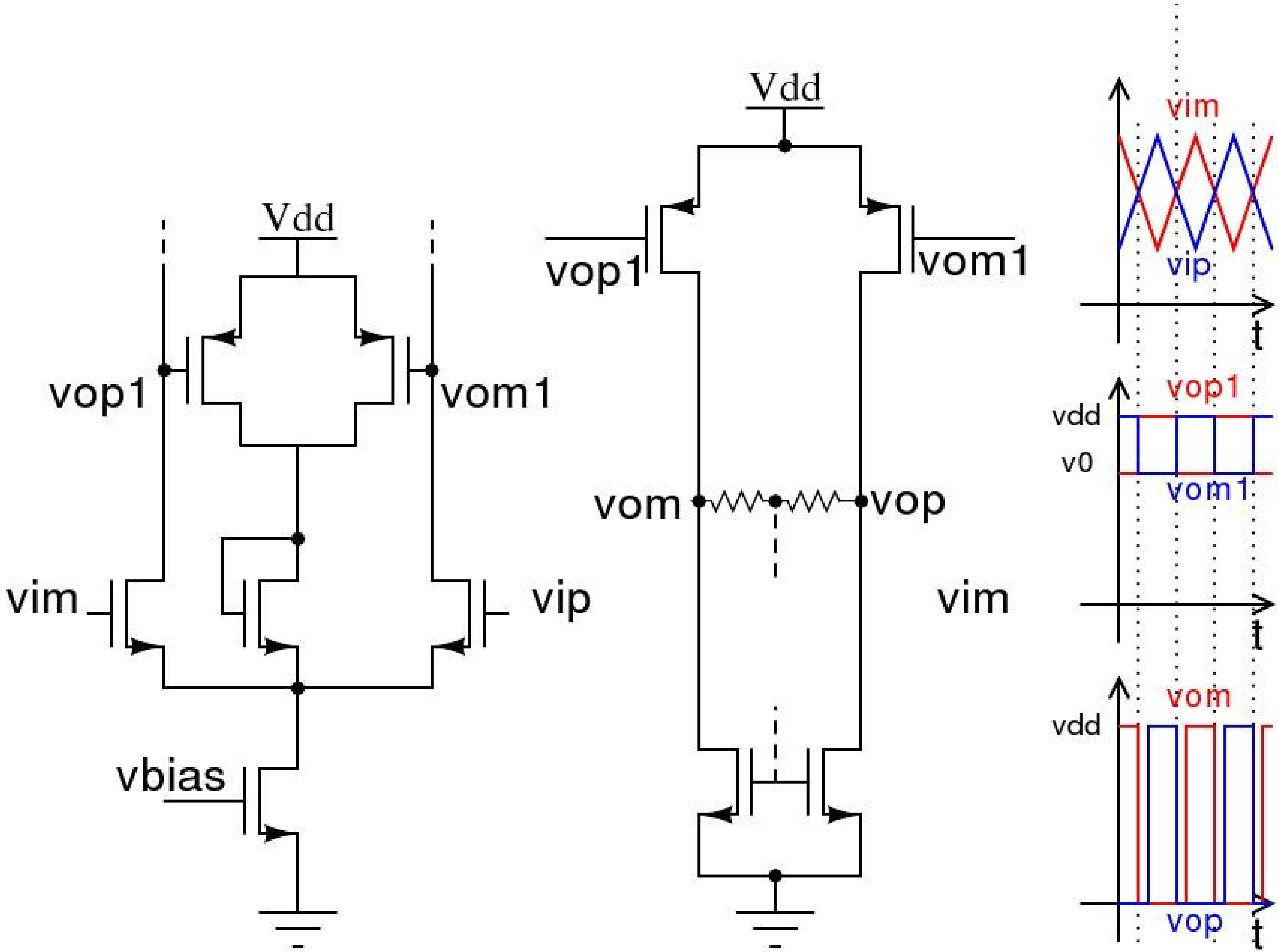


Comparator



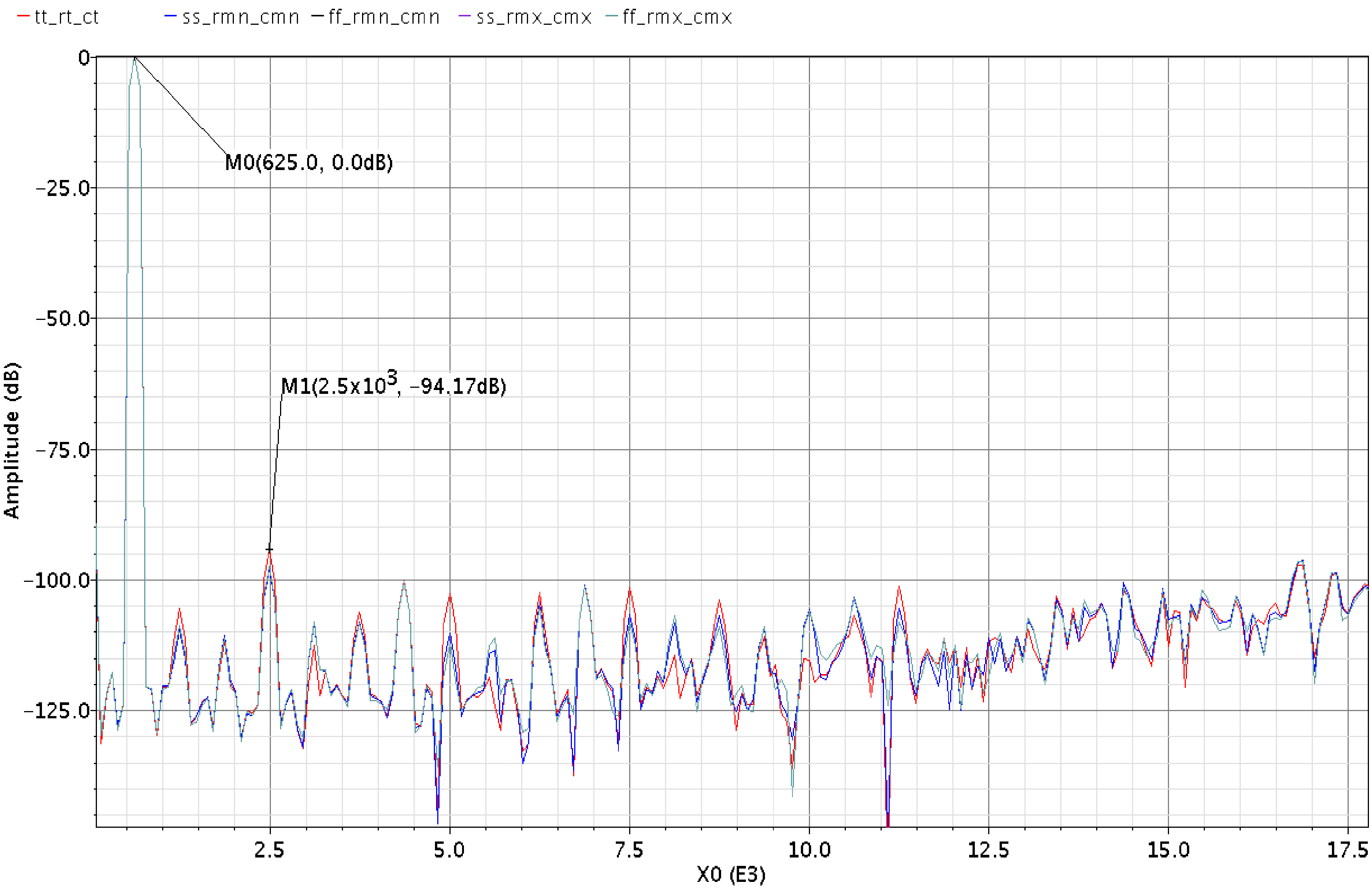
- Amplifier Schematic same as that of amp 2
- Buffer is just 2 inverters

Nonoverlap pulse generation



- 2-stage architecture adopted for comparator inherently makes it’s output non-overlapping
- Individual outputs of 1st stage swing only between vdd and vdd-2*(vdd-vcm1)
- This causes unequal drive strengths for the 2nd stage input transistors
- The above causes non-overlapping outputs

Simulation results



Performance summary

Power	Digital	33 uW
	Analog(Q)	84 uW
Area	Digital	250umx250um
	Analog	600umx700um
SNDR		90.37dB
THD		-92.68 dB
Output thermal noise		12 uVrms

References

[1] Berkhout, M., ``An integrated 200-W class-D audio amplifier,'' *IEEE Journal of Solid-State Circuits* volume 38, number 7, pages 1198 - 1206, 2003

[2] Chang, J.S. and Bah Hwee Gwee and Yong Seng Lon and Meng Tong Tan, ``A novel low-power low-voltage Class D amplifier with feedback for improving THD, power efficiency and gain linearity,'' in *IEEE International Symposium on Circuits and Systems*, ISCAS 2001, pp. 635 -638

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[4] Goldberg, J.M. and Sandler, M.B, ``New high accuracy pulse width modulation based digital-to-analogue convertor/power amplifier,'' in *IEE Proceedings- Circuits, Devices and Systems*, 1994, pp. 315 -324.

[5] Bah-Hwee Gwee and Chang, J.S. and Adrian, V, ``A micropower low-distortion digital class-D amplifier based on an algorithmic pulsewidth modulator,'' in *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 2005, pp. 2007-2022

[6] Adrian, V. and Bah-Hwee Gwee and Chang, J.S, ``,A Review of Design Methods for Digital Modulators,'' in ,*Integrated Circuits, 2007. ISIC '07. International Symposium on*, 2007, pp. 85-88