A True-1-V 300-μW CMOS-Subthreshold Log-Domain Hearing-Aid-On-Chip

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***Abstract*—This paper presents a true very low-voltage low-power complete analog hearing-aid system-on-chip as a demonstrator of novel analog CMOS circuit techniques based on log companding processing and using MOS transistors operating in subthreshold. Low-voltage circuit implementations are given for all of the required functions including amplification and automatic gain control filtering, generation, and pulse-duration modulation. Based on these blocks, a single 1-V 300-μA application specific integrated circuit integrating a complete hearing aid in a standard 1.2-μm CMOS technology is presented along with exhaustive experimental data. To the authors' knowledge, the presented system is the only CMOS hearing aid with true internal operation at the battery supply voltage and with one of the lowest current consumptions reported in literature. The resulting low-voltage CMOS circuit techniques may also be applied to the design of A/D converters for digital hearing aids.**

***Index Terms*—CMOS, CMOS analog integrated circuits, companding, hearing aid, log-domain, low-power electronics, low voltage, subthreshold.**

I. Introduction

THE increasing market demand on portable system-on-chip (SoC) applications requires new analog circuit techniques for very low-voltage and low-power operation. In this sense, hearing aids (HAs) are one of the SoC examples with the strongest supply limitations. Historically, HAs have been integrated using bipolar circuit techniques like those in [1]. However, during the last decade, such systems are being implemented through CMOS technologies in order to obtain low-power mixed SoCs. Currently, HA products can be roughly classified as either digitally programmable analog processors or embedded DSP platforms. Advantages of the former are lower cost and usually lower power consumption, while the latter can feature more complex processing algorithms and exhibit a shorter time to market. The critical design constrains in both cases come from the battery technology itself, which imposes a very low-voltage supply operation (down to 1.1 V) combined with low-power figures (below 1 mA) in order to extend battery life as long as possible (in practice, around one week). In order to overcome the very low-voltage restriction in CMOS technologies, supply multipliers based on charge pumps like those in [2] can be used. In most cases, doublers are included to boost the nominal voltage of 1.25 V supplied by the single battery, so that the internal operation of analog parts is at 2.5 V. In fact, to the authors' knowledge, all of the CMOS designs reported in literature for either digitally programmable analog [3]–[11] or fully digital [12]–[14] HAs follow this workround. Unfortunately, supply multipliers tend to increase both die area and the number of discrete components around the SoC. Also, power efficiency may be strongly reduced in a final product where battery life is of critical importance. Finally, some state-of-the-art HA implementations like that in [14] often make use of special CMOS process optimizations (e.g., deep junction isolation between analog and digital sections, low-noise bipolar devices, and low-threshold MOSFETs), which may increase the final integration cost.

This paper proposes an alternative design approach based on the log companding theory and implemented using the MOSFET in the subthreshold region. Due to the inner voltage dynamic range compression of such nonlinear processing, this novel CMOS circuit technique avoids the necessity of any supply multiplier, resulting in a programable HA-on-chip with internal operation at the true voltage of single-battery supply and very low current consumption. Furthermore, the SoC can be fully integrated in a standard CMOS technology without any process enhancement. An early report from the authors of this design example can be found in [15]. Section II describes in short the general specifications for the HA system, while Section III introduces the new CMOS proposal in the log-domain. Section IV details all of the novel low-voltage basic building blocks for amplification and automatic gain control (AGC), filtering, generation, and modulation, which are used in the HA-on-chip implementation example in Section V. Also, a complete set of experimental results of the SoC are reported in this section. Finally, conclusions are drawn in Section VI.

II. System Architecture

In general, complete HAs include amplitude compensation (i.e., amplifiers and AGC) as well as frequency-selective specifications (i.e., different types of filters) to perform different audiological corrections in the audio spectrum (from 100 Hz to 8–10 kHz). Such processing must be performed under the following restrictions: very low-voltage operation at the battery supply (down to 1.1 V), low power consumption (below 1 mA), and low area (below 10 mm^2).

Programmable analog HAs typically involve the functionalities of the system presented in top of Fig. 1. In this general

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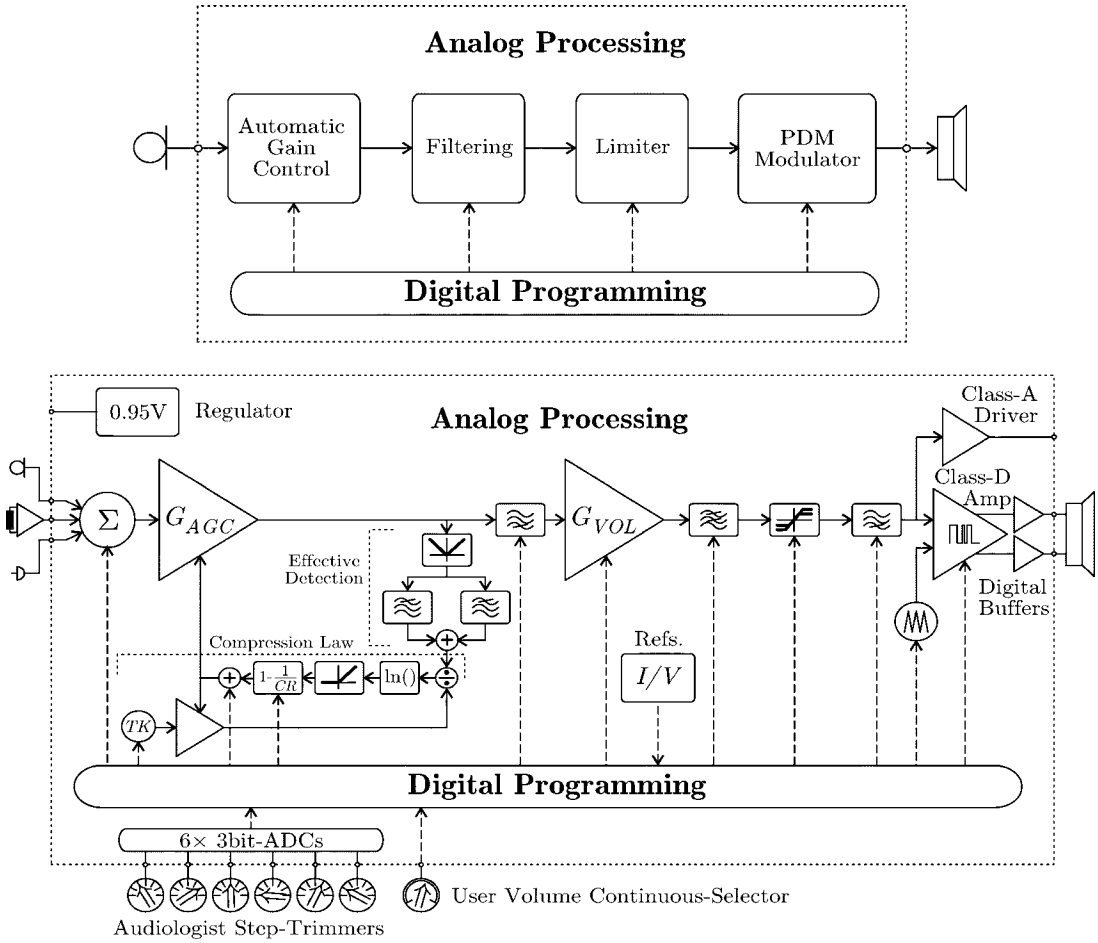

Fig. 1. Functional (top) and block level (bottom) description of the HA system presented in this paper.

model, signal processing is performed through an analog chain, while the digital control is intended for tuning the system to each particular model and user. In our case, high flexibility was desired to fit with the same chip the wide variety of HA models, ranging from behind-the-ear (BTE), which demand high gain and high output power, to completely-in-the-channel (CIC) series, with low-noise and small-size specifications. In order to meet such a level of adaptability, the system architecture shown in the bottom of Fig. 1 was chosen.

From a high-level viewpoint, the signal chain starts with a frontend to adapt the impedance of the different input sources (i.e., electret microphone, telecoil, and direct audio connector) and to mix them according to programmable weights. Furthermore, a built-in voltage regulator is also required to bias both the input microphone and the telecoil transducers.

The next stage consists of an adaptive AGC-I block which is in charge of all of the dynamic range corrections. The selected AGC algorithm [16] involves two log amplifiers for signal amplification and control of the threshold knee point (TK), respectively. The feedback loop computes the effective envelope through a combined fast and slow low-pass filters to ensure fast protection against overshoots and speech intelligibility, respectively. The rest of the loop synthesizes the steady-state compression ratio (CR) and the open loop gain (G_{AGC}) required by this application. All of these basic parameters can be tuned independently by the digital control. A detailed analysis of the AGC operation is provided when its implementation is discussed in Section IV-A.

Apart from the inherent filtering in the AGC loop, some high-pass and low-pass filters are inserted along the signal chain with selectable corner frequencies and filter orders.

Also, a limiter must be included to ensure that the user pain threshold is never reached. This block is preferably located after most of the processing chain, so its input is driven by effective signal and before the output power stage.

The intermediate amplifying stage G_{VOL} sets the overall system amplification according to the audiologist programming and the user volume selector, while the output power limiter ensures that the selected user pain threshold is never reached.

At the backend, the low-impedance receivers are driven by the Class-D output amplifier, which is based on a pulse-duration modulation (PDM) scheme to minimize quiescent consumption. Due to the wide variety of HA models, a programmable multifrequency approach has been selected to optimize high-frequency losses at the transducer. Alternatively, a Class-A driver is also included to enable the possibility of using receivers with built-in Class-D amplifiers.

Finally, optimization of the overall signal-to-noise ratio (SNR) is achieved by automatically adjusting G_{AGC} and G_{VOL} through the digital control. Furthermore, such a control can disable and bypass some stages in order to optimize power consumption.

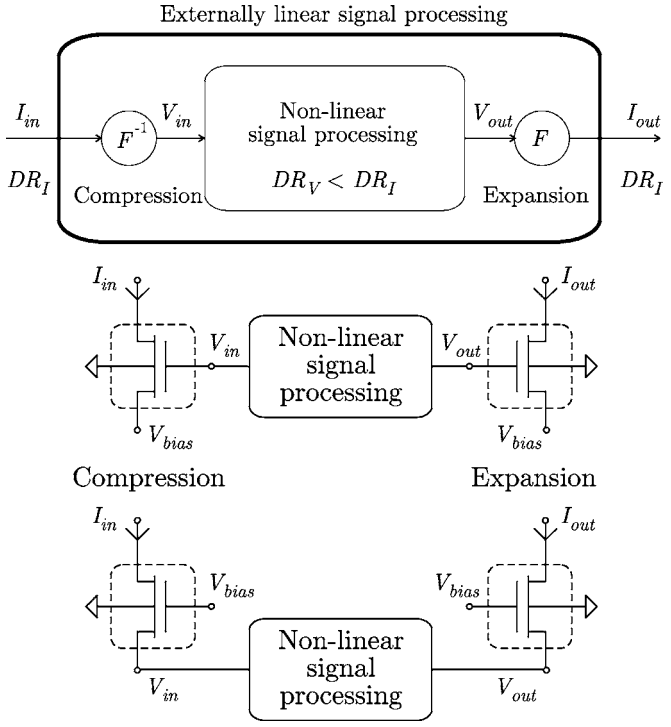

Fig. 2. General signal domains (top) and MOS cell proposals (bottom) within the log-companding processing.

III. Low-Power Basic Cell

Since our main constrains are the low-voltage and low-power requirements, the instantaneous companding approach [17] will be used here, which exploits the intrinsic nonlinear I–V characteristic of semiconductor devices to linearly process signals. A general scheme for this strategy is shown in the top of Fig. 2, where F stands for any companding function. First, incoming signals in the I domain are compressed as voltages. Then, a suitable nonlinear internal processing is performed in the V domain. After the expansion process, signals are again back to the I domain. At that point, the system behaves as externally linear, resulting in a reduction of the internal circuit dynamic range (DR) which makes this type of processing very suitable for low-voltage applications.

A widely accepted F function is the exponential law, also known as log companding [18], which is already available in bipolar devices (i.e., diodes and BJTs). However, in order to take advantage of CMOS technologies, we propose here the MOS transistor operating in weak inversion (i.e., subthreshold) as an interesting alternative. Unfortunately, log-domain CMOS circuits cannot be directly mapped from previous bipolar log techniques because of important differences at topology, device and technology levels. In weak inversion, the current–voltage relationship of the MOSFET can be taken from the EKV model [19]

$$I_D = I_S\, e[\frac{V_{GB}-V_{TO}}{nU_t}]\left(e[-\frac{V_{SB}}{U_t}]-e[-\frac{V_{DB}}{U_t}]\right), \quad V_{SB,DB} \gg \frac{V_{GB}-V_{TO}}{n} \tag{1}$$

$$I_S = 2n\beta U_t^2 \tag{2}$$

where I_S, n, β, V_{TO}, and U_t stand for the specific current, subthreshold slope, current factor, threshold voltage, and thermal potential, respectively. The above expression in forward saturation is simplified to

$$I_D \simeq I_S\, e[\frac{V_{GB}-V_{TO}}{nU_t}]\, e[-\frac{V_{SB}}{U_t}] \quad (V_{DB}-V_{SB}) \gg U_t. \tag{3}$$

As illustrated in the top of Fig. 2, two log-companding F functions at the transistor level can be proposed according to the terminal used to compress the internal voltage, either Gate (GD) and Source-driven (SD), as follows:[1]

$$I = F(V) = \begin{cases} I_S\, e[-\frac{V_{TO}+nV_{\rm bias}}{nU_t}]\, e[\frac{V}{nU_t}] & \text{GD} \\ I_S\, e[\frac{V_{\rm bias}-V_{TO}}{nU_t}]\, e[-\frac{V}{U_t}] & \text{SD} \end{cases} \tag{4}$$

where $V_{\rm bias}$ is a general reference level. From the circuit point of view, GD or SD basic cells can have more advantages depending on each type of signal processing to be implemented.

IV. Low-Voltage CMOS Basic Building Blocks

Based on the companding functions proposed in (4), this section describes how to implement in the log domain all of the functional parts of the HA-on-chip model presented in the bottom of Fig. 1 using the basic concept proposed in Section III.

A. Amplification

In general, the main purpose of any amplifying stage is to provide a linearly scaled copy of the input signal

$$I_{\rm out} \doteq GI_{\rm in} \tag{5}$$

where G stands for the gain factor. Applying the GD MOS companding function (4), to keep the system externally linear, the required processing in the compressed domain follows:

$$V_{\rm out} = \Delta V_{\rm gain} + V_{\rm in} \tag{6}$$

where $\Delta V_{\rm gain}$ is the gain control signal. Based on this idea, the general purpose amplifier of Fig. 3 is proposed, where boxed devices operate in weak inversion.[2] The main amplifying devices are the M1 and M2 pair, which correspond to the input compressor and output expander, respectively. The compressor M1 is controlled by the local feedback M3–M6, which provides a sufficiently low input impedance (typically below 100 Ω) as any ideal current-mode processing block. The same reasoning also applies to the expander M2 assuming that a similar control is provided by the next cascaded stage (not shown in the figure). The frequency compensation for a given parasitic input capacitance $(C_{\rm in})$ can be achieved through this loop by selecting the compensation capacitor $(C_{\rm comp})$ according to the damping factor

$$\zeta = \frac{1}{2}\sqrt{\frac{KC_{\rm comp}}{C_{\rm in}}}. \tag{7}$$

[1]There is a third alternative, corresponding to the Bulk-driven case, which is not considered in this proposal due to its incompatibility with the antilatchup rules of any CMOS technology.

[2]In what follows, all boxed devices in any figure are operated in weak inversion and with its bulk connected to the corresponding supply voltage.

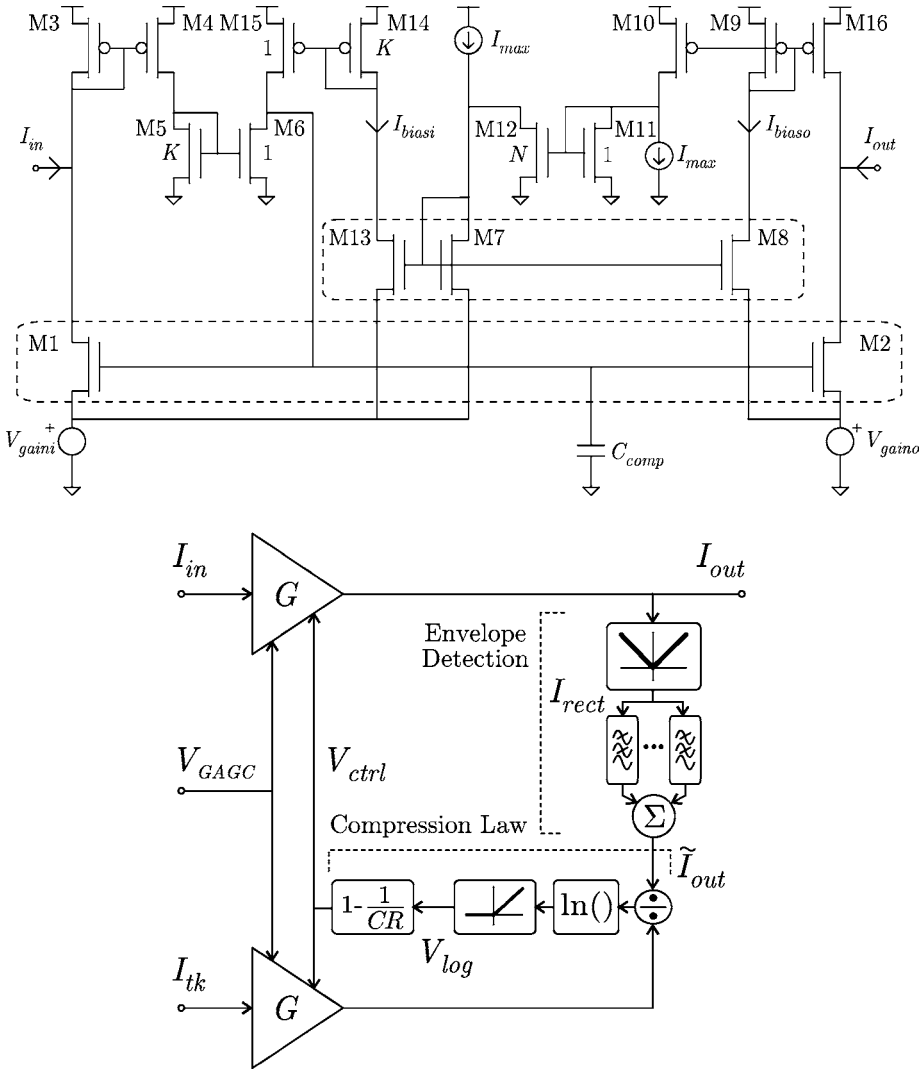

Fig. 3. Low-voltage log amplifier cell (top) and AGC scheme using such a block (bottom).

Biasing is performed through M7-M8, which act as a parallel amplifier controlled by the same gain and operated in open-loop as an attenuator (i.e., $I_{\rm biasi} = I_{\rm max}$), being $I_{\rm max}$ the maximum signal level allowed in compressors and expanders, typically in the range of 1–10 μA. The output of the biasing amplifier is permanently monitored by M9 and M10, so in case it exceeds the allowed range (i.e., $I_{\rm biaso} > I_{\rm max}$), the error amplifier M11 and M12 automatically corrects the $I_{\rm biasi}$ value, which is mirrored to the compressor M1 through M13–M15. Hence, the proposed scheme is compatible with either amplification or attenuation factors.

Applying the GD compression law (4) to both compressor and expander as follows:

$$\frac{I_{\rm out} + I_{\rm biaso}}{I_{\rm in} + I_{\rm biasi}} = e^{\frac{V_{\rm gaini} - V_{\rm gaino}}{U_t}} \tag{8}$$

the resulting gain expression of this log amplifier is

$$G\,[\text{dB}] = 20\log(e)\frac{V_{\rm gaini} - V_{\rm gaino}}{U_t} = 20\log(e)\frac{\Delta V_{\rm gain}}{U_t}. \tag{9}$$

The basic advantages of splitting the gain control signal $\Delta V_{\rm gain}$ into two grounded sources $V_{\rm gaini}$ and $V_{\rm gaino}$ is to simplify its circuit implementation and to supply two independent ports for controlling the gain. In practice, these gain control signals[3] are usually in the range of $0 < V_{\rm gaini,o} < 7U_t$, which corresponds to a total programmable amplification range as large as $\pm$60 dB. Section IV-D faces the synthesis of proportional to absolute temperature (PTAT) voltage references to cancel first-order thermal dependency in G due to U_t. In general, the control of $(V_{\rm gaini} - V_{\rm gaino})$ allows electronic gain tuning for either fixed or programmable amplification and attenuation factors, like $G_{\rm VOL}$ in the bottom of Fig. 1.

B. Automatic Gain Control

The linear relation in decibels from (9) is of special interest for the synthesis of finite compression ratios as in the detailed AGC algorithm of the bottom of Fig. 3, where $I_{\rm tk}$ stands for the threshold-knee point while the $\tilde{I}$ operator means the steady-state envelope of I. In this scheme, the output effective envelope $(\tilde{I}_{\rm out})$ is first computed applying full-wave rectification and some low-pass filtering to the signal-amplifier output. Then, the

[3]A typical value for the gain sensitivity is around 0.43 dB/mV at room temperature.

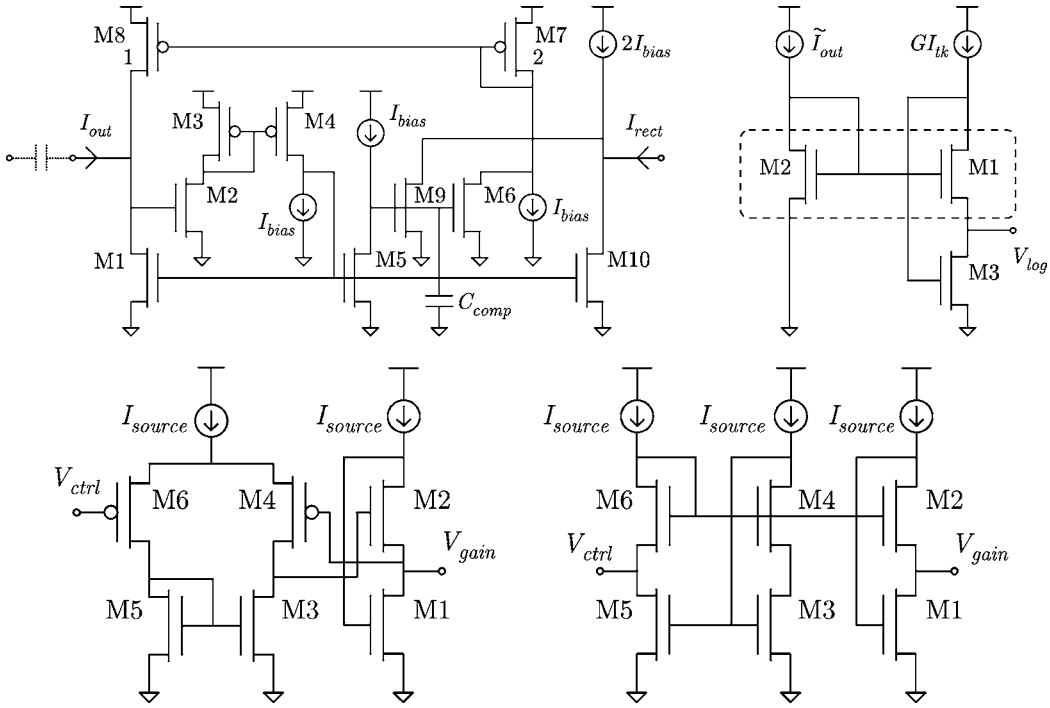

Fig. 4. Low-voltage precision full-wave rectifier (top left) and first-quadrant only log divider (top right), and gain control sources for low technology-mismatching (bottom left) and low noise (top right).

error signal $(V_{\log})$ is obtained from the log comparison between $\tilde{I}_{\rm out}$ and the output of a parallel amplifier fed at $I_{\rm tk}$. The close loop CR is generated by scaling $V_{\log}$ and injecting such a signal $(V_{\rm ctrl})$ to the attenuation port of both amplifiers (i.e., $V_{\rm gaino}$ in the top of Fig. 3). The remaining control port of both amplifiers (i.e., $V_{\rm gaini}$ in the top of Fig. 3) is devoted to configure the open-loop gain $G_{\rm AGC}$ using a programmable PTAT reference $(V_{\rm AGC})$. Finally, the resulting input–output compression curve is

$$\tilde{I}_{\rm out} = \begin{cases} \tilde{I}_{\rm in} & \tilde{I}_{\rm in} \le I_{\rm tk} \\ I_{\rm tk}^{1-\frac{1}{CR}} \tilde{I}_{\rm in}^{\frac{1}{CR}} & \tilde{I}_{\rm in} > I_{\rm tk} \text{ and } 1 < CR < \infty. \end{cases} \tag{10}$$

Note that AGC compressing must not be confused with the companding approach itself, since the latter operates instantaneously, restores the original dynamic range at the output, and is directly synthesized at the transistor level. From the above discussion, it is clear that in addition to the controllable amplifier cell shown in the top of Fig. 3, the other blocks in the bottom of Fig. 3 are needed to implement the complete AGC loop. In this sense, a full-wave rectifier is presented in the top left of Fig. 4. The rectifier consists of two loops controlling the positive (M1–M4) and the negative phases (M5–M9) to obtain a final summation in M10. This circuit proposal allows high-precision rectification from $I_{\rm out}$ to $I_{\rm rect}$ by combining a low-enough input impedance for dc decoupling, as well as a very low current bias level $(I_{\rm bias})$, typically few nanoamps. The effective envelope in the model shown in the bottom of Fig. 1 is computed through two combined fast and slow low-pass filters, which define the dynamic behavior of the AGC stage in terms of attack $(t_{\rm att})$ and release times $(t_{\rm rel})$ according to [20]. For this purpose, the basic building blocks for filtering described in Section IV-C can be employed. The divider, log function, and first-quadrant-only operators of the AGC loop are compacted in the circuit proposal of top right of Fig. 4, where $\tilde{I}_{\rm out}$ is coming from the envelope detector, resulting in

$$V_{\log} = \begin{cases} 0, & \tilde{I}_{\rm out} \le GI_{\rm tk} \\ U_t \ln\left(\frac{\tilde{I}_{\rm out}}{GI_{\rm tk}}\right), & \tilde{I}_{\rm out} > GI_{\rm tk}. \end{cases} \tag{11}$$

Due to the reduced voltage dynamic range in the log domain of the gain control signal $V_{\rm ctrl}$ of Fig. 3, the remaining scaling factor (i.e., $1 - 1/CR$) to synthesize the compression ratio can be implemented applying conventional resistive dividers to $V_{\log}$ based on well layers or simple MOS resistive circuits (MRCs).

In order to control any of the gain ports of the log amplifier shown in the top of Fig. 3, two low-voltage followers are shown in the bottom of Fig. 4, where $V_{\rm ctrl}$ stands for a high-impedance PTAT reference or control signal. Although both schemes use a similar output stage M1–M2, the first proposal depicted in Fig. 4 (bottom left) is optimized for low technology-mismatching as the differential error signal is computed by the small group M3-M6, while Fig. 4 (bottom right) proposes a lower noise solution by reducing the local-loop gain.

C. Filtering

The CMOS circuit technique proposed for the synthesis of frequency-selective stages in the log domain is illustrated here through a low-pass prototype, like the envelope detector of the AGC scheme of Fig. 3 (bottom). Such a case study can be described by the following linear ordinary differential equation (ODE) in the I domain:

$$\frac{{\rm d}I_{\rm out}}{{\rm d}t} = 2\pi f_o (I_{\rm in} - I_{\rm out}) \tag{12}$$

where f_o stands for the -3-dB corner frequency. Now, after applying the SD companding function proposed in (4), the equivalent nonlinear processing in the V domain to keep the filter externally linear results in a nonlinear ODE as follows:

$$\frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t} = 2\pi f_o U_t \left(1 - e^{\frac{V_{\mathrm{out}} - V_{\mathrm{in}}}{U_t}}\right). \tag{13}$$

In order to finally obtain a circuit implementation, the internal state-space variable V_{out} is stored across a grounded linear capacitor (C). Then, the above expression can be rewritten as follows in the charge domain (Q) as a nonlinear circuit transconductance driving the capacitor C:

$$\begin{aligned}\frac{\mathrm{d}Q_{\mathrm{out}}}{\mathrm{d}t} &= \underbrace{C\frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t}}_{I_{\mathrm{cap}}} \\ &= I_{\mathrm{tuno}} e^{\frac{V_{\mathrm{out}}}{U_t}} \left(e^{-\frac{V_{\mathrm{out}}}{U_t}} - e^{-\frac{V_{\mathrm{in}}}{U_t}}\right) \qquad (14) \\ I_{\mathrm{tuno}} &= 2\pi f_o U_t C \qquad (15)\end{aligned}$$

where I_{cap} and I_{tuno} stands for the capacitor current and the tuning parameter,[4] respectively. Such an expression can be mapped into the low-voltage CMOS implementation proposed in the top of Fig. 5, in this case a second-order cascaded structure. First, M1 acts as the input compressor translating I_{in} to V_{in}, while M3–M5 generate the suitable biasing levels. Then, the term enclosed in brackets of (14) is implemented by M6 (M7 for the second stage) even operating in nonsaturation. The remaining part of the expression is obtained through M8 (M9 in the second stage). Finally, the expander M2 translates the compressed signal back to the linear I domain. The VF block corresponds to a voltage follower, which is mandatory to supply a low-impedance copy of V_{out}. In this sense, the circuits shwon in the bottom of Fig. 4 are fully compatible with this cell.

As depicted in the top of Fig. 5, the filter order can be easily selected through bypass NMOS switches without any voltage supply problem, as the common mode of the compressed signals is typically below 200 mV. Again, suitable PTAT current references to cancel thermal dependencies in frequency tuning are discussed in Section IV-D. A more general study on arbitrary CMOS log filtering from these authors can be found in [21].

D. PTAT Generation

From the basic building blocks proposed in the previous subsections, it is clear at this point the necessity of both voltage and current PTAT references for gain and frequency tuning, respectively. Hence, a built-in PTAT generator is included in the SoC model of Fig. 1 (top) in order to supply to the digital control all of the required analog references for tuning. In this sense, a low-voltage and compact CMOS circuit is proposed in Fig. 5 (bottom). The core pair, M1–M2, operates at weak inversion, while the feedback path, M3–M8, forces a $1/P$ for the pair current ratios. Then, the voltage reference is given by

$$V_{\mathrm{ref}} = U_t \ln P \tag{16}$$

which allows its use for gain tuning of (9). From the current generation viewpoint, two different operation modes can be distinguished. In case the switch is off and there is no R_{ref} (i.e., all-MOS implementation), the MOS impedance M10–M11 is attached to the voltage reference port through M9 and operated in strong inversion saturation and conduction, respectively, causing

$$I_{\mathrm{ref}} = Q\left[\frac{\ln P}{2(M+1)}\left(\sqrt{\frac{M}{N}} + \sqrt{\frac{M}{N+M+1}}\right)\right]^2 I_{S11} \tag{17}$$

which is a specific-current based expression, suitable to generate signal biasing levels like $I_{\max}$ in the top of Figs. 3 and 5. On the other hand, provided that the switch is on and a R_{ref} exists, the resulting expression changes to

$$I_{\mathrm{ref}} = Q\frac{U_t}{R_{\mathrm{ref}}} \ln P. \tag{18}$$

Due to the PTAT behavior, I_{ref} is devoted in this case to the frequency tuning of (14). Nevertheless, the new topology of Fig. 5 (bottom) exhibits very low-voltage capabilities in both operation modes to ensure correct biasing for the rest of the SoC even at the end of battery life.

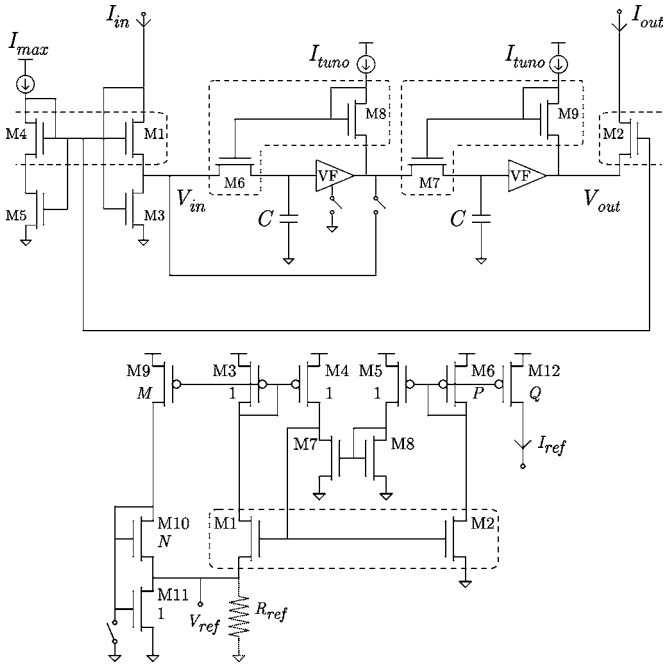

Fig. 5. Low-voltage low-pass filtering example (top) and PTAT generation proposal (bottom).

E. Pulse-Duration Modulator

In general, a PDM signal (V_{PDM}) can be obtained from a 1-b comparison between the base-band input (I_{in}) and a higher frequency triangle waveform (I_{tri}), as shown in Fig. 6 (top). Since comparators are easily implemented in the I domain, efforts are focused on the synthesis of I_{tri}. In this sense, such a waveform can be obtained by integrating a constant reference (I_{ref}), which is periodically inverted according to an output window defined by I_{thmin} and I_{thmax}. From the linear domain viewpoint, we have

$$\frac{\mathrm{d}I_{\mathrm{tri}}}{\mathrm{d}t} = \pm\frac{I_{\mathrm{ref}}}{\tau} \qquad I_{\mathrm{thmin}} < I_{\mathrm{tri}} < I_{\mathrm{thmax}} \tag{19}$$

[4]A typical value for the corner sensitivity is about 0.16 kHzpF/nA at room temperature.

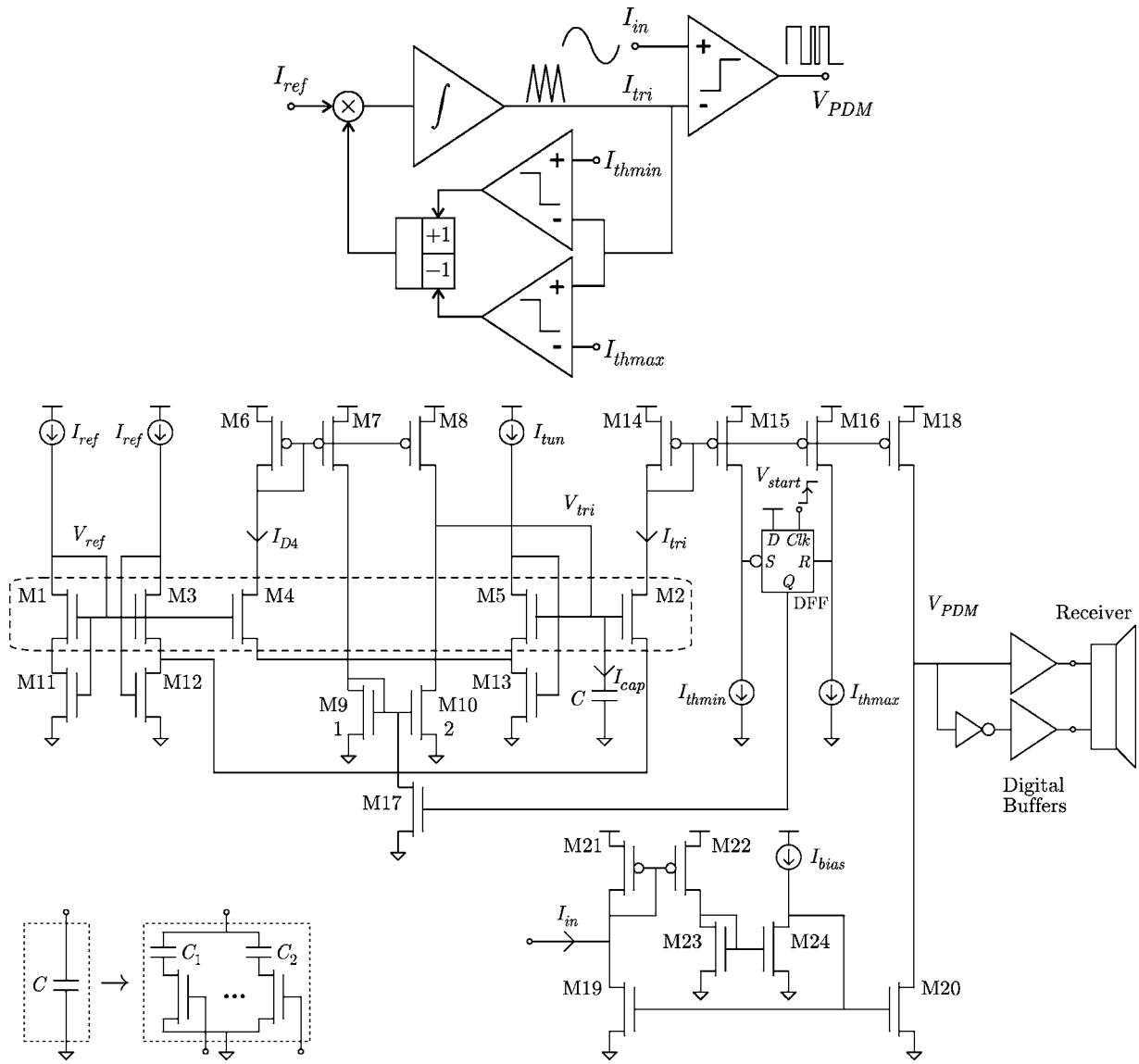

Fig. 6. Block-level description of the PDM modulator (top) and low-voltage CMOS proposal (bottom).

where τ stands for a generic time constant. In this case, after applying the GD companding function (4), the above linear ODE is translated into the compressed V domain as follows:

$$\frac{\mathrm{d}V_{\mathrm{tri}}}{\mathrm{d}t} = \pm\frac{nU_t}{\tau}e^{\frac{V_{\mathrm{ref}}-V_{\mathrm{tri}}}{nU_t}}. \tag{20}$$

In case of storing the compressed signal V_{tri} across a grounded linear capacitor (C), the final nonlinear ODE to be implemented in the Q domain can be understood as a nonlinear transconductance driving the integrator capacitor through I_{cap}

$$\frac{\mathrm{d}Q_{\mathrm{tri}}}{\mathrm{d}t} = \underbrace{C\frac{dV_{\mathrm{tri}}}{\mathrm{d}t}}_{I_{\mathrm{cap}}} = \pm I_{\mathrm{tun}}e^{\frac{V_{\mathrm{ref}}-V_{\mathrm{tri}}}{nU_t}} \qquad I_{\mathrm{tun}} \doteq \frac{nU_tC}{\tau} \tag{21}$$

where I_{tun} stands for the tuning current, which controls the period of the triangular oscillator (T_{tri}) according to

$$T_{\mathrm{tri}} = 2\frac{nU_tC}{I_{\mathrm{tun}}}\left(\frac{I_{\mathrm{thmax}}-I_{\mathrm{thmin}}}{I_{\mathrm{ref}}}\right). \tag{22}$$

A low-voltage CMOS implementation of the modulator is shown in Fig. 6 (bottom). The triangle oscillator is displayed at the upper part of the figure and built through transistors M1–M18. Basically, this oscillator consists of: the input compressor, M1, generating V_{ref}, the nonlinear transconductance pair, M4–M5, driving the integrator capacitor C through M6–M10, and the output expander, M2, attached to the compressor common reference through the low-impedance source M3 and M12. Transistor M11 is used to ensure proper operation of telescopic devices M12 and M13. Oscillation is forced by the feedback window comparator M15–M16, which alternatively changes the sign of the slope stored in a D-type flip-flop (DFF). This memory element sets the charge and discharge phases of the capacitor C by switching the mirror M9–M10, so forcing $I_{\mathrm{cap}} = \pm I_{D4}$. Also, an impedance adapter M19–M24 is included to supply a low-enough input impedance. Finally, the input signal is compared to the triangle waveform through M20 and M18, generating the voltage PDM signal (V_{PDM}). In practice, due to the wide variety of load

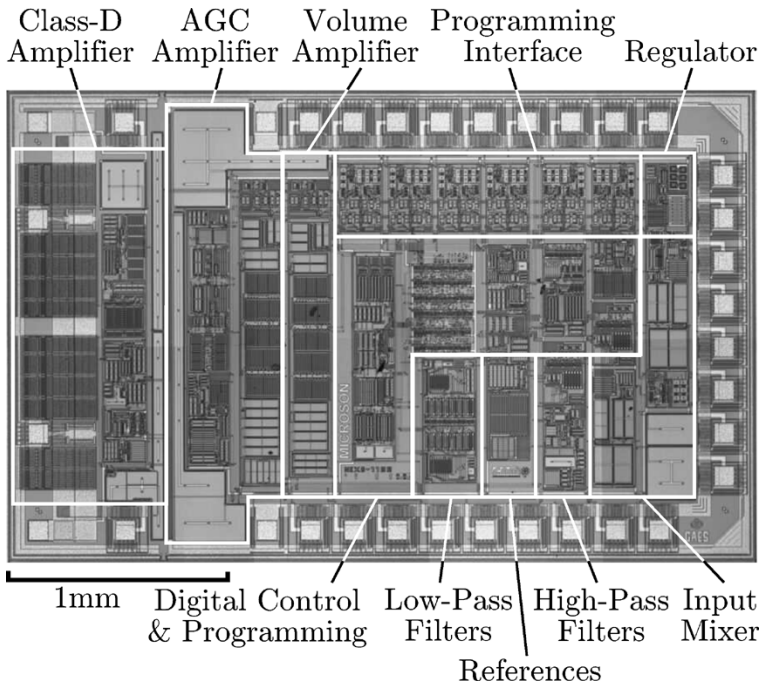

Fig. 7. Microscope photography of the HA-on-chip.

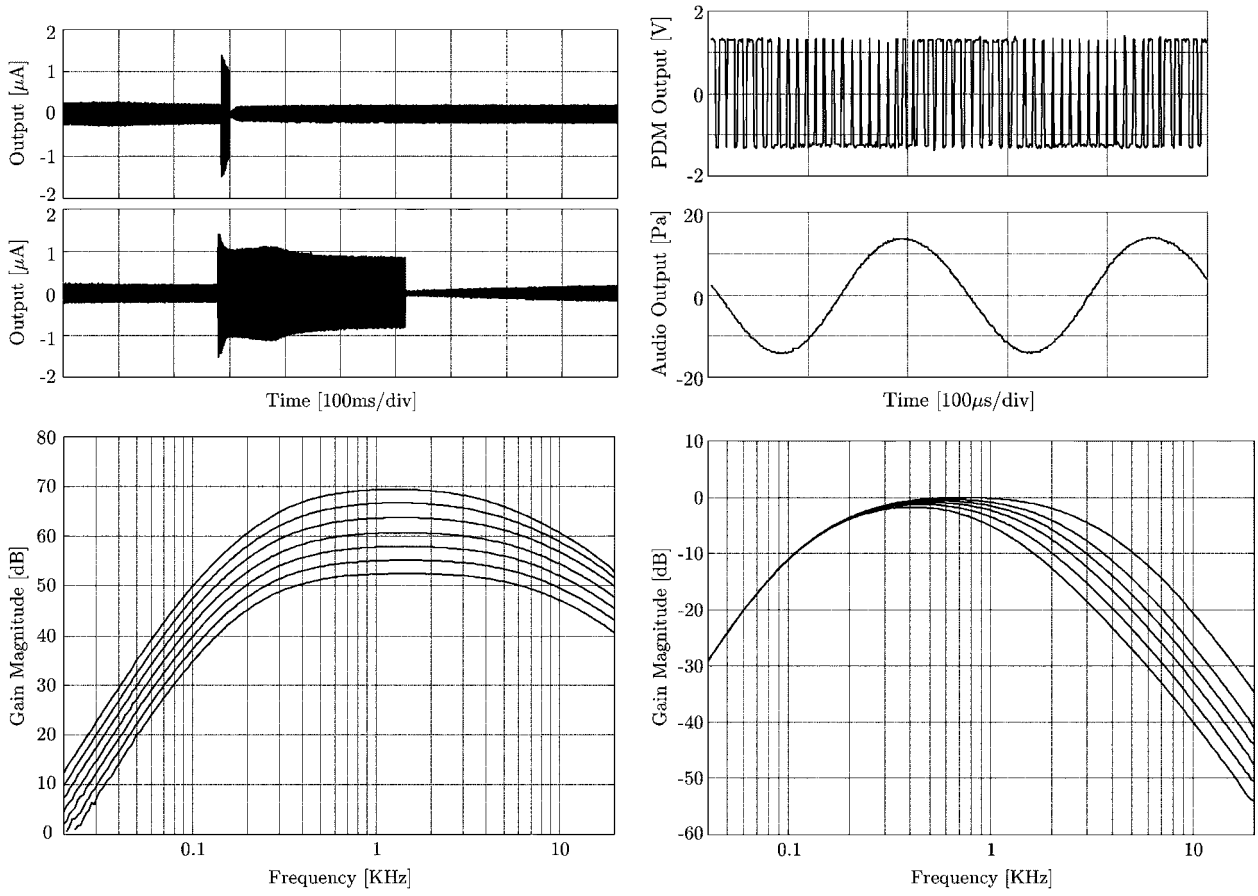

Fig. 8. Experimental AGC output for different ±25-dB input burst durations (top left), differential PDM and acoustic signal at receiver for a half full-scale 4-kHz input (top right), frequency transfer functions versus system gain (bottom left), and normalized transfer functions versus low-pass tuning (bottom right).

receivers for the SoC application, a multi-frequency approach is requested to minimize high-frequency losses at the transducer. For this purpose, a capacitor array is built according to the same Fig. 6 (bottom) with NMOS selection switches to ground. Hence, different C values can be programmed from the digital control.

TABLE I
OVERALL EXPERIMENTAL RESULTS OF THE HA-ON-CHIP

Parameter	Conditions	Value	Units
Min. supply voltage		1.0	V
Max. $V_{TON}+\|V_{TOP}\|$		1.3	V
Queiscent power	w/o Class-D w Class-D	<200 <300	μA μA
Max. gain		70	dB
Equivalent input noise	100Hz-10KHz	6	μV_{rms}
Max. SNR	100Hz-10KHz	70	dB
Max. THD at half full-scale	w/o Class-D w Class-D	0.1 <1	% %
Si area	including pads	7.5	mm^2

V. ASIC IMPLEMENTATION AND EXPERIMENTAL RESULTS

Based on all CMOS circuit techniques proposed in the previous section, the complete HA model of Fig. 1 (bottom) was integrated in a 1.2-μm double-polySi double-metal CMOS process. Although the same circuits could have been designed for a submicrometer ULSI technology, this VLSI process was selected in this case for its low cost. The final ASIC prototype can be seen in Fig. 7.

The development of the complete SoC involved the full custom design of about 5000 MOS transistors. System full scale was chosen as $I_{\max} = 2\ \mu\mathrm{A_{peak}}$. Both AGC and volume amplifiers were built to allow wide gain range operation $-35\ \mathrm{dB} < G_{\mathrm{AGC,VOL}} < +35\ \mathrm{dB}$. In the case of the dual envelope detection for AGC, the tuning current was set to $I_{\mathrm{tuno}} = 10$ nA, equivalent to a 2.5-MΩ resistance, which in conjunction with external capacitors of 4.7 and 100 nF allow the implementation of $t_{\mathrm{att}} = 15$ ms and $t_{\mathrm{rel}} < 500$ ms, respectively. In fact, the release time is adapted to the duration of the perturbation as depicted in Fig. 8 (top left), resulting in an improved speech intelligibility. For the Class-D output stage, the switching frequency can be programmed from 80 to 150 kHz, while power buffers can drive up to 20 $\mathrm{mA_{peak}}$ across the bridge. In this sense, Fig. 8 (top right) shows the PDM signal driving the receiver and its equivalent acoustic audio output measured at the transducer.

A summary of the experimental results is given in Table I for both configurations, driving the receiver through the built-in Class-D output amplifier or using an external Class-D by means of the additional Class-A output included in the ASIC. The overall gain and its fine digital programmability in 3-dB steps can be seen in Fig. 8 (bottom left). The system also allows coarse digital control of such parameters in a range of 60 dB. In this sense, an external supply capacitor is recommended for high-gain and low-impedance receiver configurations (i.e., BTE) as the power-supply rejection ratio (PSRR) of the basic building blocks is typically 60 dB in-band. Fig. 8 (bottom right) illustrates the tuning capabilities of the low-pass filter banks through different codes. Although not shown, such control also includes order selection for the filtering. The flexibility of the adaptive AGC stage is illustrated in Fig. 9, where the compression ratio, the threshold knee point, and the open-loop gain are independently changed according to the digital control. Concerning the unavoidable output offset due to technology mismatching, Monte Carlo simulations of the Class-D amplifier were performed to limit by design the static current of this stage to the target values referred to in Table I. A typical HA product based on this SoC only requires the following external components (apart from transducers): a reference resistor for the PTAT generator, a couple of capacitors for the dual AGC, and another one for the full-wave rectifier. In order to demonstrate the robustness of the presented SoC, exhaustive tests have been applied to 50 samples taken from the preproduction series. Some of the statistical results are presented in Fig. 10 in terms of gain, corner frequency, and compression ratio programming, respectively. From all of the collected data, deviations (at $\pm 2\sigma$) are shown to be around 1.7 dB for the gain, 3.5% for the frequency tuning, and about 8% for the offset referred to full scale.

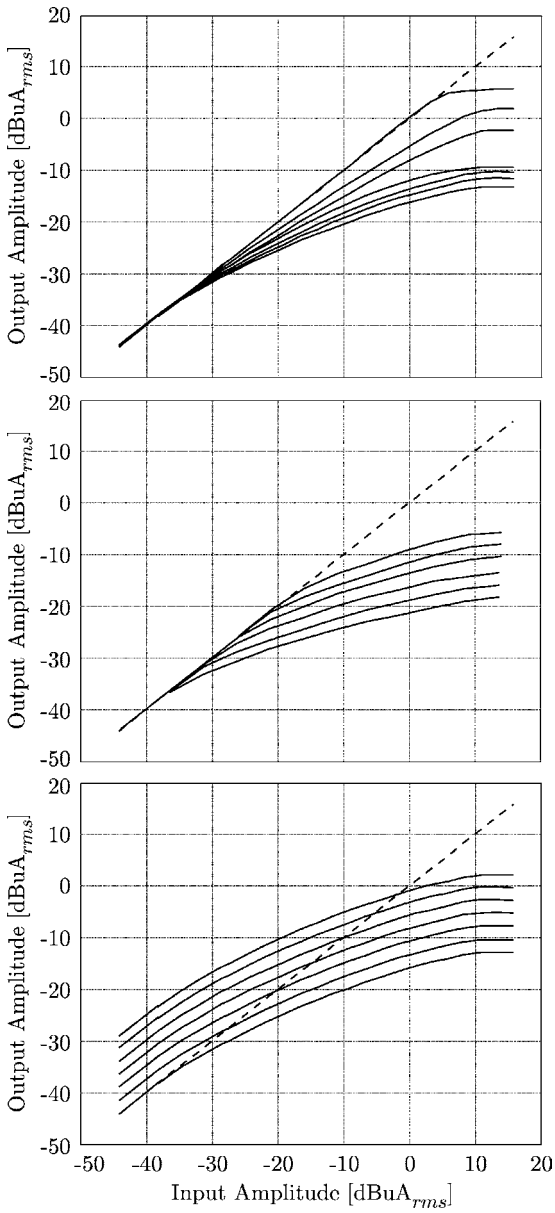

Fig. 9. Experimental AGC steady-state input–output normalized response versus CR (top), TK (middle), and G_{AGC} (bottom) tuning.

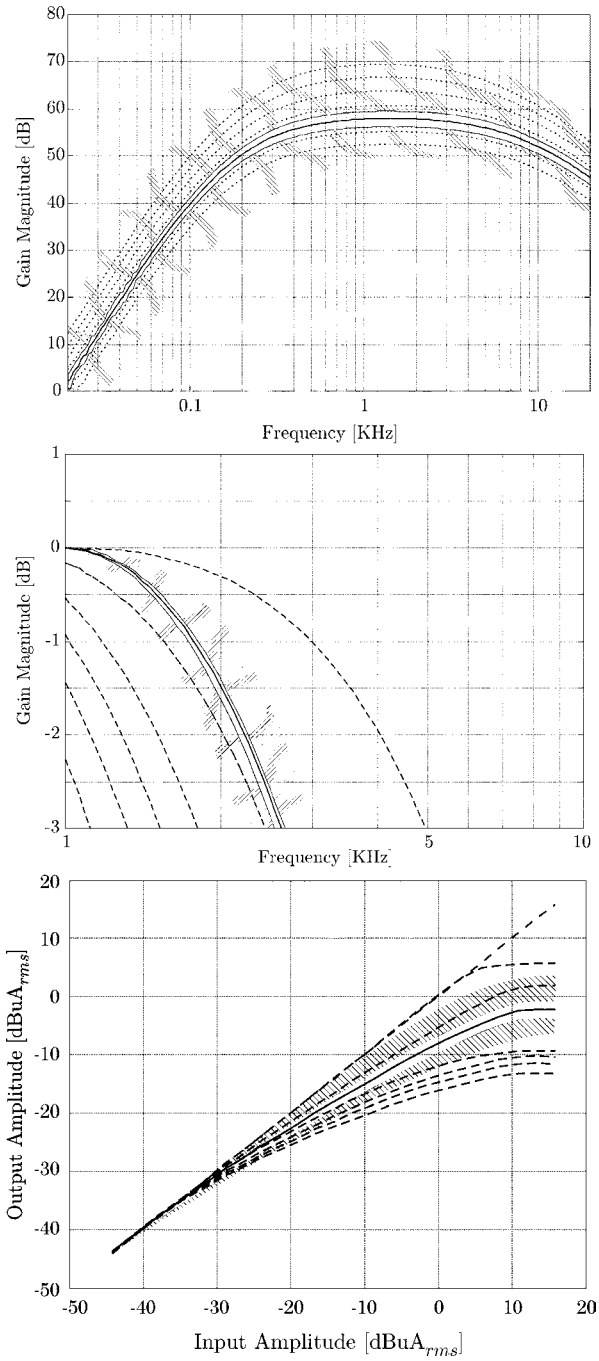

Fig. 10. Example of experimental deviations ($\pm 2\sigma$ within the striped areas) around nominal programming (solid line) and other digitally programmable responses (dashed line) for the overall gain (top), high-cut corner frequency (middle). and compression ratio (bottom).

VI. Conclusion

A complete programmable HA-on-chip has been designed and integrated in a CMOS technology using a new design technique which allows very low-voltage operation (down to 1 V) and low-power consumption (below 300 μA). The system makes use of of both the log-companding theory and the MOSFET operating in weak inversion to allow true operation with a single-battery supply. Following this strategy, a complete set of basic building blocks for amplification, AGC, filtering, PTAT generation, and PDM modulation are given. The experimental data in terms of nominal response and yield demonstrate the feasibility of the proposed design technique. The resulting high-gain, low-power, low-area, low-distortion, high-flexibility, and low-cost HA-on-chip meets the targeted specifications. Hence, using this single IC, all of the HA products (i.e., BTE, in-the-ear, in-the-channel, and CIC models) can be built changing only programming and some external elements like transducers. To the authors' knowledge, the presented SoC example is the first analog CMOS circuitry, for either programmable analog HAs or for the A/D frontend in digital HA products, to truly operate at the real battery voltage without the need for any charge-pump for supply multiplying and exhibiting one of the lowest current consumptions. Furthermore, compared to state-of-the-art digital HAs of similar signal processing complexity like that in [14], this SoC can be integrated in half of the Si area through standard CMOS technologies exhibiting half of the process scaling, resulting in a substantial cost reduction.

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