8.2 A Fully Integrated Digital Hearing-Aid Chip with Human-Factors Considerations

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Recently, the design of biomedical devices [1] has focused on how to accommodate individual user differences for performance optimization and better comfort. That is, human factors should be taken into account early in the design process. Usually, a digital hearing aid (DHA) chip incorporates the human factors after the chip fabrication by the gain fitting and verification process shown in Fig. 8.2.1. However, the post fitting operation has many intrinsic problems. Since the amount of compensated gain varies widely from 0dB to 25dB [2], the conventional gain compensation scheme, especially the completely in the canal (CIC) type, takes a long time and often cannot provide sufficient gain because of its narrow dynamic range. In addition, the probe-tube microphone verification method generates errors due to the position of the probe-tube. The functional gain method also has poor test-retest reliability and limited frequency resolution [3].

To overcome these problems, a pre-fitting verification algorithm (PREVA) along with its implemention and use in a highly programmable DHA chip is presented. The PREVA obtains the gain fitting in two steps, coarse- and fine-gain fittings, enabling objective, accurate and fast gain fitting, and verification. The ear canal modeling filter circuit (EMC) enables coarse fitting based on the physical shape of the external ear without ambiguous feedback from the patient. After the coarse fitting by EMC, the fine fitting verification can be executed with little additional patient interaction.

The EMC models the individual ear to obtain the natural resonance values as shown in Fig. 8.2.1. Based on an X-ray image of the patient, the exact 3D shape of his/her external ear can be formed. Then, a distributed L or C filter is derived to model the acoustic filter characteristics of the external ear [4]. The LC filter, or EMC, can be included into the DHA chip design process to enable so called human-chip co-design. That is, the detailed characteristics of the individual external ear can be included into the design of the DHA. Even the volume change of the ear canal after the DHA is inserted into the external ear can be considered by modifying the EMC appropriately. The external 11b control signals, labeled SEMC, are used to modify the structure of the filter according to the shape of the individual ear. The parameters from the EMC enable the DSP in the DHA to achieve the user-optimized gain fitting in accordance with the hearing loss audiogram of the patient. The parameters for the fine-gain fitting can be input to the DHA through a serial interface. The proposed DHA chip is illustrated in Fig. 8.2.1. In this test chip, the EMC is composed of 14 fixed taps and 16 variable taps, for a total of 30 taps. Of course, the total number of taps and the number of variable taps can be increased further. The 11b SEMC signals modify the number of taps and LC values according to the individual ear shape. Among the 11b SEMC signals, a 1b signal is used to distinguish between the L and the C. Each L (C) is composed of four L (C) values to enable trimming with a 2b signal, and a 4b signal is allocated to select one tap among the 16 variable taps.

The proposed chip consists of 3 major blocks: the EMC unit, the parameter acquisition unit (PAU) and the DHA unit. The DHA block includes a dual-threshold preamplifier, an adaptive-SNR ΔΣ ADC [5], a dedicated DSP [6], a heterogeneous ΔΣ DAC [6], and a receiver driver. The PAU is composed of a peak detector (PD), a successive approximation ADC (SAADC), and a parameter generator (PG).

The PD of Fig. 8.2.2 provides the peak gain value as a function of frequency in steps of 1kHz from 1kHz to 8kHz. The digitized resonance value of the individual ear is processed by the PG, which receives both the coarse compensation gain (CCG) parameters and the fine compensation gain (FCG) parameters.

The architecture of the proposed PAU with PREVA is shown in Fig. 8.2.2. The pre-fitting of the PREVA is realized by choosing the resonance value, which is the largest influence to the gain fitting. The EMC output at 4kHz is always selected because it highly affects the amount of gain compensation. The largest value (G1) among the outputs of the 5b SAADC (G1) and the output value at 4kHz (G1) determines the amount of the CCG. The FCG has a default initial value that can be changed by the external parameter inputs (G1 and PS) set at the post gain verification step. The peak value of the gain (G1) and the gain at 4kHz (G1) are used as a FCG parameters. The CCG parameters and FCG parameters are combined to provide the total DHA gain (G1) of the DSP gain.

The block diagram of the 5b SAADC is shown in Fig. 8.2.3. The standby power consumption is reduced compared with the conventional SAR [7], by adopting the gated clock signals GCS. Moreover, switching off the capacitor array logic decreases the power dissipation further when the comparison phase is over.

Figure 8.2.4 shows the measured results of the proposed PAU. After the peak values of the resonance signals are detected and inputted to the PAU (a), the gain values are measured (b) and digitized (c). Two gain values, the largest one and one at the 4kHz, are selected to acquire the verification gain (d). The overall operation of the proposed DHA is explained in Fig. 8.2.5. A hearing loss audiogram of a patient, presented in Fig. 8.2.5(a), shows losses at 1kHz and 4kHz. In order to compensate for such hearing losses, EMC is modified to provide a coarse gain compensation of Fig. 8.2.5(b). The dotted line is the desired gain compensation and the solid line is the measured gain compensation by the coarse compensation only. Figure 8.2.5(c) shows the final results with the fine gain verification. In this case, the preamplifier gain is selected as 1 to verify the performance of the PAU. Compared with the conventional DHA, the proposed system enables accurate and fast on-chip fitting verification by incorporating the human factors. The DHA chip with PAU is shown in Fig. 8.2.6 and occupies a core area of $3.12\times1.2mm^2$ in a standard 0.18μm CMOS technology. The power consumption is 120μA using a single 0.9V supply. Figure 8.2.7 summarizes the features of the fabricated chip.

References:

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[4] D. R. Raichel, "The Science and Applications of Acoustics," 1st ed., Springer, 2000.

[5] S. Kim, et al., "An Energy-Efficient Analog Front-End Circuit for a Sub-1-V Digital Hearing Aid Chip," *IEEE J. Solid-State Circuits*, vol. 41, pp. 876-882, Apr., 2006.

[6] S. Kim, et al., "A 0.9V 96μW Digital Hearing Aid Chip with Heterogeneous sigma-delta DAC," *Dig. Symp. VLSI Circuits*, pp. 68-69, June, 2006.

[7] M.D. Scott, et al., "An Ultralow-Energy ADC for Smart Dust," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1123-1129, July, 2003.

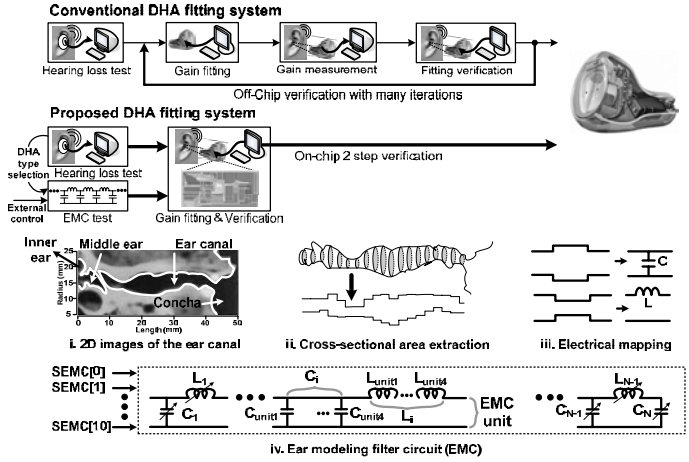

Figure 8.2.1: Conventional and the proposed DHA.

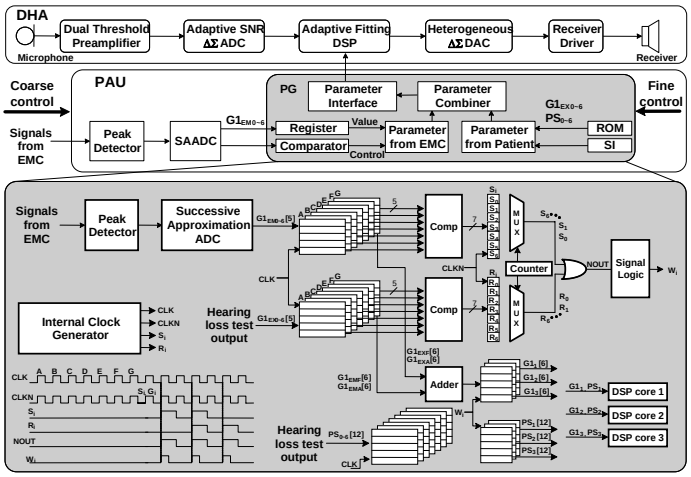

Figure 8.2.2: Block diagram of the DHA chip and PAU.

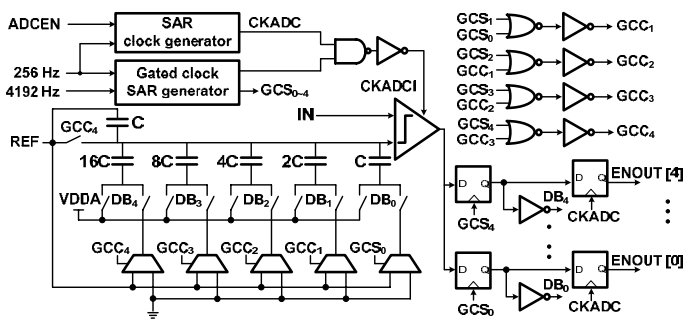

Figure 8.2.3: Architecture of the proposed SAADC.

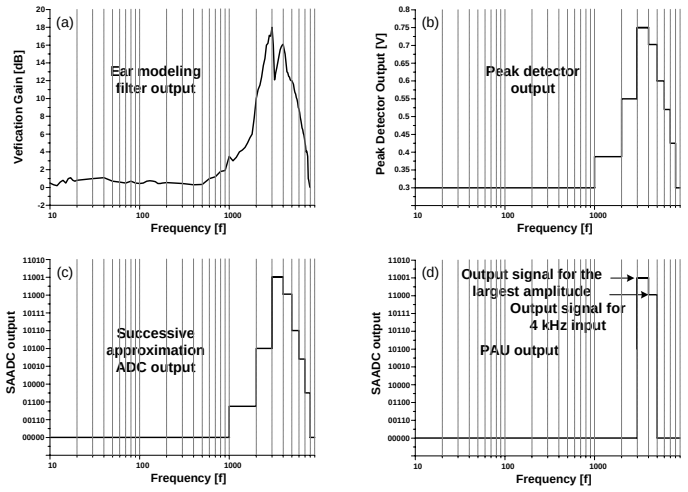

Figure 8.2.4: Measured results of the proposed PAU.

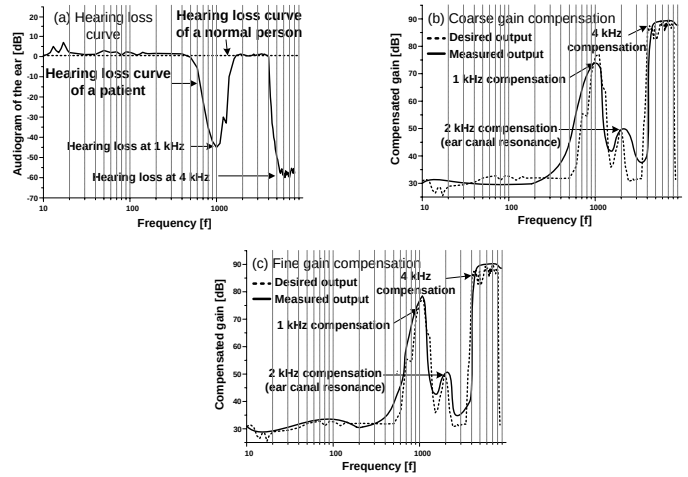

Figure 8.2.5: Measured results of the hearing compensation operation.

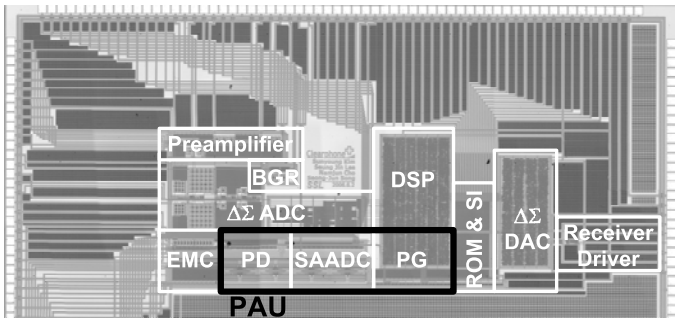

Figure 8.2.6: Chip micrograph of the DHA system.

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Supply voltage	**0.9V**
Peak SNR (overall system)	81dB
Power dissipation	**78μA (Analog) / 40.5μA (Digital)**
-3 dB bandwidth	8kHz
Input referred noise	$4.2\mu V_{rms}$
Core area	$3.12 \times 1.2mm^2$
Process	0.18μm CMOS technology

Pre amp	Max. gain	38dB				**DSP & PG**	Gate count	43K	
	$DR_{Threshold}$	0.45V~0.8V					DSP clock freq.	32kHz	
ΔΣ ADC	Type	1	2	3	4		Channel	8 / 3	
	SNR_{Peak} (dB)	75	85	77	89	**SA ADC**	Sampling rate	256	
ΔΣ DAC	Gate count	16K					On current	0.8μA	
	Input freq.	512kHz					Standby current	55pA	
	Clock freq.	2.048MHz					ENOB (2kHz)	5.7	

Figure 8.2.7: Performance summary.

