8.2 A Fully Integrated Digital Hearing-Aid Chip with Human-Factors Considerations

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A digital hearing-aid chip integrates a pre-fitting verification algorithm to obtain gain fitting in two steps: coarse and fine. The internal ear canal modeling filter circuit enables the coarse fitting based on the shape of the external ear. Fine fitting verification is performed with external inputs. The 3.74mm² chip draws less than 120μA from a single 0.9V supply in a 0.18μm CMOS technology.

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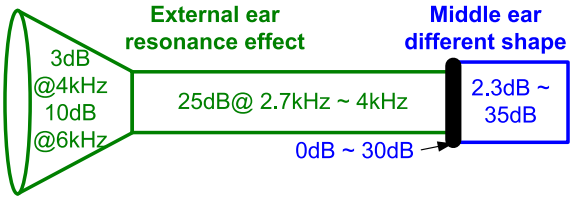
Outline

- **Motivation**
- **Digital Hearing Aid (DHA) Architecture**
  - Ear modeling filter circuit (EMC)
  - Pre-fitting verification algorithm (PREVA)
- **Low Power Techniques**
  - Dual-threshold preamplifier
  - Adaptive-fitting digital signal processor
  - Gated successive approximation ADC
- **Implementation Results**
- **Conclusion**

Importance of Ear Modeling



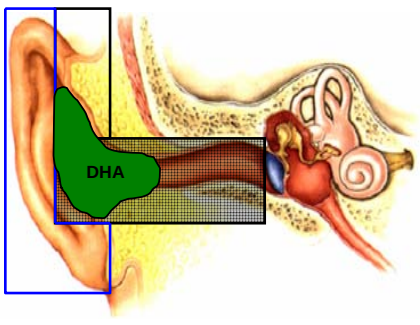
- **Individual ear requires different gains!**
  - People have different ear shapes
  - Digital hearing aids have various shapes
- **Ear modeling is required!**

Design Requirements Shift

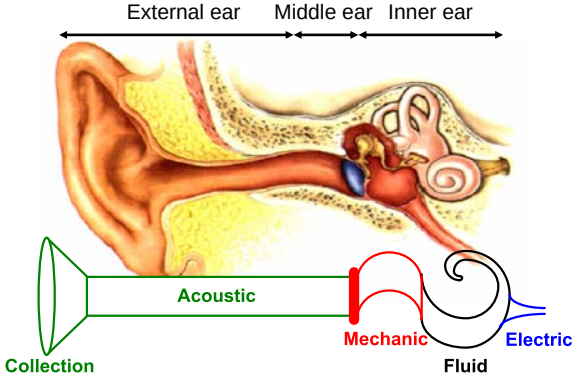
- **Conventional Designs**
  - No customized design
  - Post gain-fitting design
  - One chip for all types of DHA
- **Problems**
  - Many iterations
  - Long verifications
  - Narrow gain dynamic range
  - Limited frequency resolution

External Ear Effect – ITE Type

Audio input can utilize only partial pinna resonance

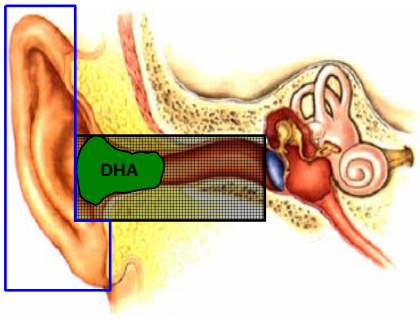


Ear Anatomy



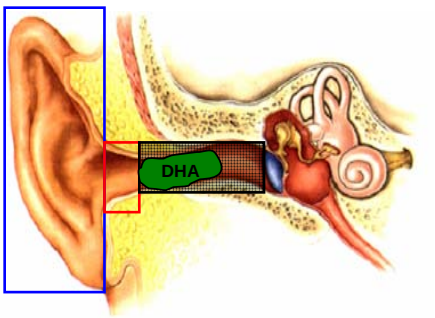
External Ear Effect – ITC Type

Only pinna resonance

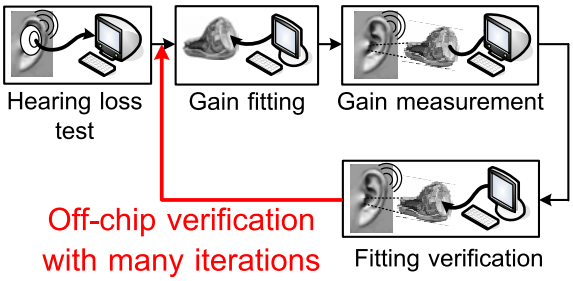


External Ear Effect – CIC Type

Pinna resonance + Partial canal resonance



Conventional DHA Fitting Topology

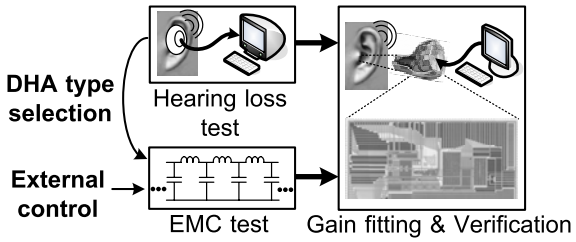


Importance of Ear Modeling

- **Paradigm Change in DHA**
  - Customized design
  - High programmability
  - High comfort level
  - Fast gain fitting

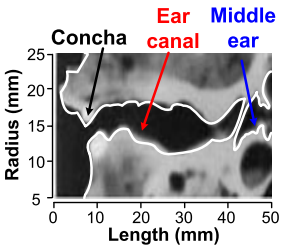
  ➡ **Human factors should be considered early in the design process**
- **This Work**
  - Digital hearing aid chip with
    - ➢ Human ear modeling filter (EMC)
    - ➢ Pre-fitting verification algorithm (PREVA)
  - Low power consumption: 107μW@ 0.9V supply

Proposed DHA Fitting Topology

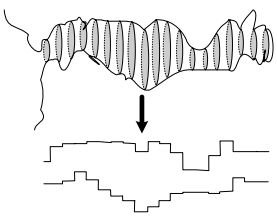


On-chip 2-step verification

Ear Modeling Filter Circuit Design



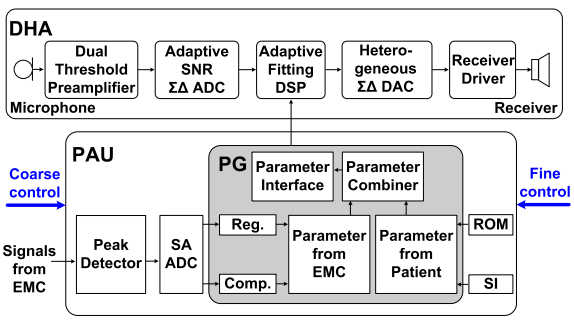
2D X-ray images of the ear canal



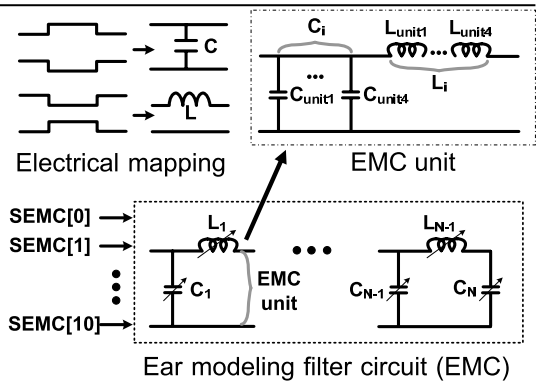
Cross-sectional area extraction

Pre-Fitting Verification Algorithm

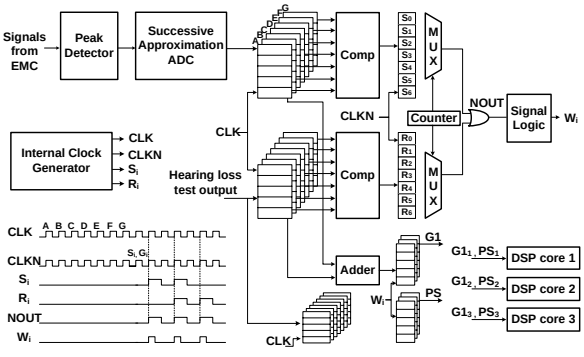
- **Two-Step Gain Fitting and Verification Method**



Ear Modeling Filter Circuit Design



Architecture Overview – PAU & PREVA



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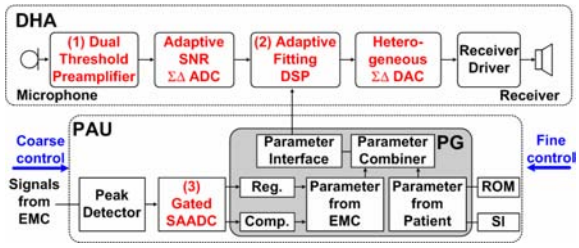
Low Power Techniques



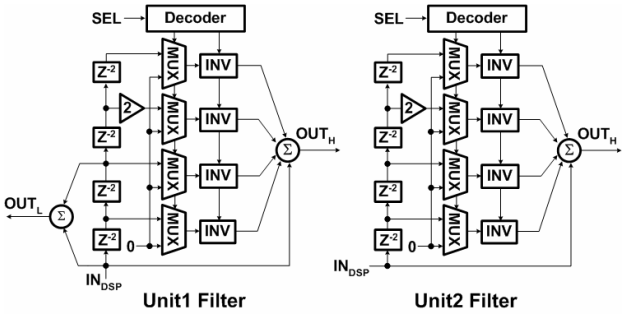
(1) Dual-threshold preamplifier

(2) Adaptive-fitting digital signal processor

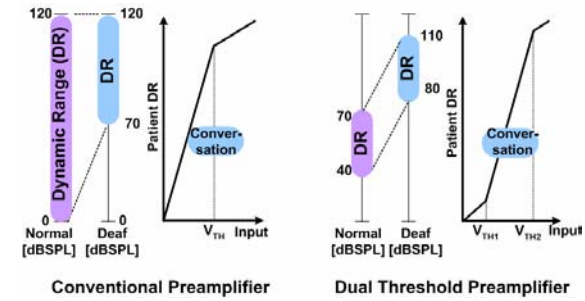
(3) Gated successive approximation ADC (SAADC)

Adaptive-Fitting DSP (2/2)

- Low Power Filter Architecture



Dual-Threshold Preamplifier (1/2)



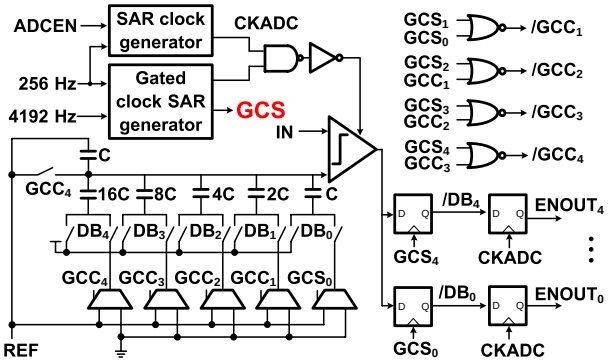
Edge distortion

Narrow conversation range

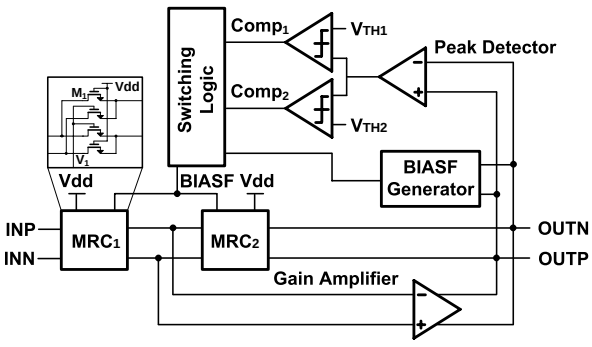
Eliminate edge distortion

Wide linearity

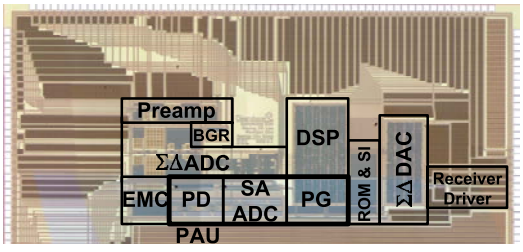
Gated Successive Approximation ADC



Dual-Threshold Preamplifier (2/2)



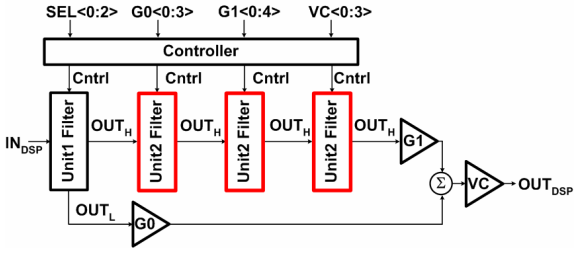
Chip Microphotograph



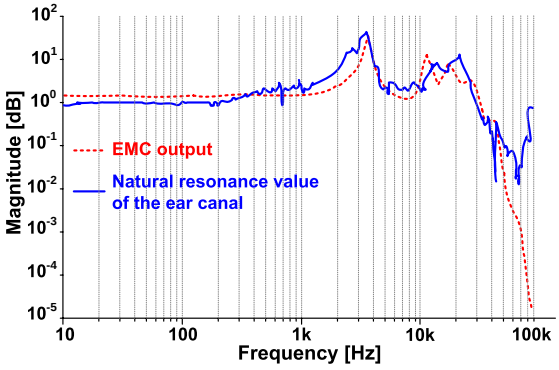
- 0.18μm 6M CMOS technology
- 3.12 x 1.20mm²
- 0.9V power supply
- 107μW power consumption

Adaptive-Fitting DSP (1/2)

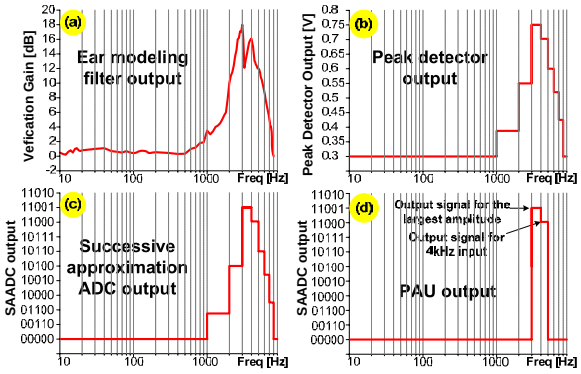
- **Solution: DSP Filter Reuse**
  - Reduce design difficulties by reusing Unit2 Filter
  - Simplification of transfer function



Natural Resonance Value



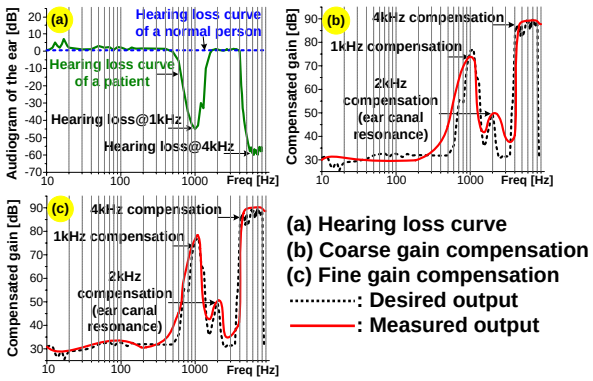
PAU Measurement Results



Comparison of DHA Chip

	JSSC 1997 Neuteboom, et.al.	JSSC 2004 Serra-Graells, et.al.	This work
Supply voltage	1.3V	1V	0.9V
Peak SNR	77dBA	70dB	81dB
Power consumption	2mW	200μW	107μW
Type	Digital	Programming	Digital
Design techniques based on human factors	No	No	Yes (EMC, PREVA)
# of DSP band	4	-	8
CMOS technology	Low V_{TH} 0.8μm	1.2μm	0.18μm

Hearing Compensation Example

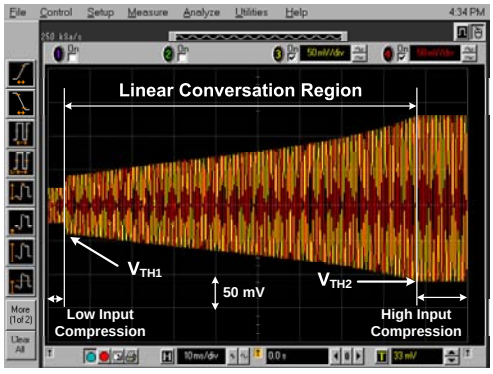


(a) Hearing loss curve
(b) Coarse gain compensation
(c) Fine gain compensation
.....: Desired output
——: Measured output

Conclusion

- **A Digital Hearing-Aid Chip with Human-Factors Considerations**
  - Ear modeling filter circuit (EMC)
  - Pre-fitting verification algorithm (PREVA)
- **Low Power Techniques Utilized**
  - Dual-threshold preamplifier
  - Adaptive-fitting digital signal processor
  - Gated successive approximation ADC
- **Overall Power Consumption**
  - 107μW@ 0.9V supply

Dual-Threshold Preamplifier Output



Performance Summary

Supply voltage						0.9V		
Peak SNR (Overall Voltage)						81dB		
Power dissipation						70μW(analog) / 37μW(Digital)		
-3dB bandwidth						8kHz		
Input referred noise						4.2μVrms		
Human factor considered techniques						EMC / PREVA		
Core area / CMOS process						3.12 x 1.20 mm² / 0.18μm		
Pre amp	Max. gain	38 dB				DSP & PG	Gate count	43K
	DB_{TH}	0.45V~0.8V					Clock freq.	32kHz
ΣΔ ADC	Type	1	2	3	4		Channel	8/3
	SNR_{PEAK} (dB)	75	85	77	89	SA ADC	Sampling rate	256
ΣΔ DAC	Gate count	16K					On current	0.8μA
	Input freq.	512kHz					Standby current	55pA
	Clock freq.	2.048MHz					ENOB (2kHz)	5.7