A Fully Integrated Digital Hearing Aid Chip With Human Factors Considerations

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***Abstract*—A low-power digital hearing aid chip with consideration of the human external ear characteristics according to the each individual user is proposed and implemented. It adopts the pre fitting verification algorithm (PREVA) to obtain the fast and accurate gain fitting and verification in two steps, coarse and fine gain fittings. The ear canal modeling filter circuit (EMC) which models the human external ear into the distributed *LC* filter enables the coarse gain fitting based on the shape of the external ear of the patient. The fine fitting verification is performed by the external inputs from the hearing loss test results. To reduce the power consumption of the human factored hearing aid chip design, the multi-threshold preamplifier, the adaptive fitting digital signal processor (DSP) with the filter reuse technique and the gated successive approximation ADC are designed and embedded to the digital hearing aid chip. The dynamic range of the multi-threshold preamplifier exists from 0.45 V to 0.8 V and dissipates 32 μW from a single 0.9 V supply. The fabricated digital hearing aid chip achieves the peak SNR of 81 dB in the overall system with 4.2 μVrms of input-referred noise voltage. The fabricated chip occupies the core area of 3.12×1.20 mm^2 in a 0.18 μm standard CMOS technology and consumes only 107 μW from a single 0.9 V supply.**

***Index Terms*—Digital hearing aid, ear canal modeling filter circuit, external ear resonance gain, multi-threshold preamplifier.**

I. Introduction

RECENTLY, the design issues of the biomedical devices [1], [2] are changed to how to accommodate the individual differences for the performance optimization according to the each individual user and comfortable level enhancement [3]. That is, human factors should be taken into account early in the design process. Usually the digital hearing aid (DHA) chip incorporates the human factors after the chip fabrication by the external gain fitting and verification process through the hearing loss test. However the post gain fitting process has many intrinsic problems. One of the most important problems is the measurement difficulties of the individually required insertion gain. Conventional insertion gain verification method using the probe-tube microphone generates measurement errors due to the position of the probe-tube microphone in the completely in the canal (CIC) type hearing aid. Besides, the amount of compensated gain varies widely from 0 dB to 25 dB according to the conditions of the patient [4]. Therefore, the conventional gain compensation scheme, especially in CIC type, takes long time to verify the required gain and cannot provide the sufficient gain because of its narrow dynamic range. In addition, this method is hard to apply to the babies or the kids because it limits the body movement when the gain measurement is processed. To solve these problems, the 2 cc coupler method is widely used because of its measurement conveniences. It supposes that the volume of the external ear canal is uniformly 2 cc. However, it has fundamental errors due to the different ear canal and concha characteristics according to the individual users compared with the uniform 2 cc coupler. The functional gain verification method which measures the sound field threshold has also many limitations such as poor test-retest reliability, limited frequency resolution, inefficiency, and inability to provide any information about real-ear maximum output levels [5].

To overcome these problems, this paper presents the pre fitting verification algorithm (PREVA) and implements it in a high programmable DHA chip. The PREVA obtains the gain fitting in two steps, coarse and fine gain fittings to enable the objective, accurate and fast gain fitting and verification. The ear canal modeling filter circuit (EMC) enables the coarse gain fitting based on the physical shape of the external ear without ambiguous feedback from the patient. After the coarse gain fitting by EMC, the fine gain fitting and verification can be executed with little iteration of interview with patient using the external hearing loss test results.

The design considerations of the EMC modeling and implementation methods are presented in Section II. Section III describes the design methodologies and circuit techniques of the parameter acquisition unit (PAU) with PREVA in detail. Moreover, it includes the overall digital hearing aid architecture. In Section IV, low-power design techniques of the fabricated digital hearing aid chip are shown. It includes the details of the multi-threshold preamplifier, the adaptive fitting DSP with filter reuse technique, and the gated successive approximation ADC to reduce the power dissipation and enhance the programmability of the DHA chip. The real chip implementation and measurement results are presented in Section V. Finally, conclusions are made in Section VI.

II. Human Ear Modeling Considerations

Modeling of the human ear function has been described by adopting various approaches. The finite element method (FEM), a general numerical procedure, is usually used in modeling complex electro-mechanical biological system [6]. Although the FEM is accurate and intuitive method to model the human ear, it is hard to integrate the FEM algorithm into the digital hearing aid chip because of the seriously complex data processing algorithm of the FEM. In addition, the FEM obtains only approximate solutions and many input data are required.

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The conventional analog human ear model is constructed by converting the ear transfer function into the transformer circuit with passive or active analog circuit elements [7]. However, the inflexibility of the analog circuit and the excessively large values of the passive elements made it impossible to apply the conventional analog ear model to the digital hearing aid on a chip. To achieve the accurate and flexible ear modeling method with the consideration of the human factors, the ear canal modeling filter circuit (EMC) is newly implemented and embedded into the digital hearing aid on a chip.

A. Requirements of the Human Ear Modeling

The major roles of the human external ear are sound acquisition and gain resonance effect. Because of its closed-ended pipeline structure, each external ear canal has different resonance value. It changes the compensation gain of the digital hearing aid according to the each individual user. In addition, each middle ear also has its own gains due to the different ear shape and joint method among the parts of the middle ear [8]. Significant individual variation, up to 25 dB, exists in middle ear function at key hearing thresholds. Therefore, the value of the resonance gain varies from 30 dB to 50 dB according to the different shapes and characteristics of the human external ear and the middle ear. It requires the human ear modeling ahead of digital hearing aid chip design.

Moreover, the natural ear canal resonance value is affected according to the different types of the digital hearing aid. Fig. 1(a) shows the external ear resonance effect when the in the ear (ITE) type digital hearing aid is used. In this case, only the partial pinna resonance effect changes the gain of the digital hearing aid. It means the resonance effects of the remained part of the pinna and the whole ear canal are ignored when the gain of the digital hearing aid is first fitted. Fig. 1(b) presents the external ear resonance effect when the in the canal (ITC) type digital hearing aid is adopted. In this case, the whole pinna resonance effect affects the digital hearing aid when the gain fitting and verification are processed. However, the whole ear canal resonance effect is still ignored due to the location of the digital hearing aid in the human external ear. Fig. 1(c) shows the ear resonance effect when the completely in the canal (CIC) type digital hearing aid is putted on. In this case, the whole pinna resonance effect and the partial ear canal resonance effect influence to the gain of the digital hearing aid. However, the resonance effect of the remained partial ear canal is still neglected and cannot affect the resonance gain of the digital hearing aid. Since the type of the digital hearing aid highly affects the compensation gain of the digital hearing aid, it should be considered prior to the design of the digital hearing aid. By regarding the type of the digital hearing aid and calculating the required gain before the hearing aid is worn, the number of post gain fitting and verification process is reduced drastically. The type of the digital hearing aid can be considered by modeling the human external ear and estimating the remained volume of the ear after the digital hearing aid is putted on.

According to the mentioned results, the design paradigms of the digital hearing aid should be changed how to deliberate the individual differences of the human ear. In order to achieve both the high comport fitting process and the user optimized performance in design of the digital hearing aid chip, human factors should be cogitated primarily in the design process.

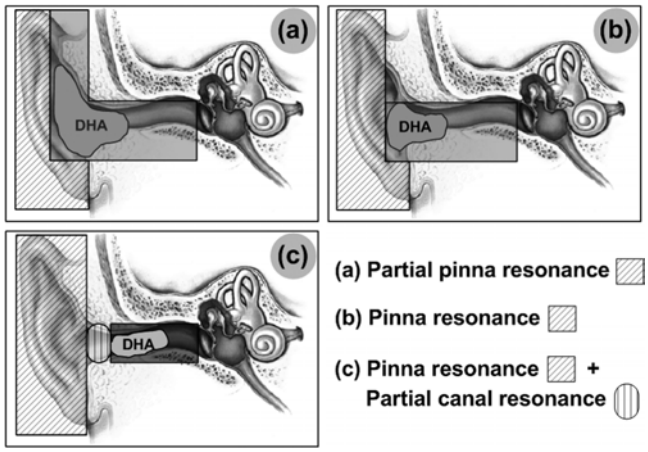

Fig. 1. Ear resonance effects due to the different types of the digital hearing aid.

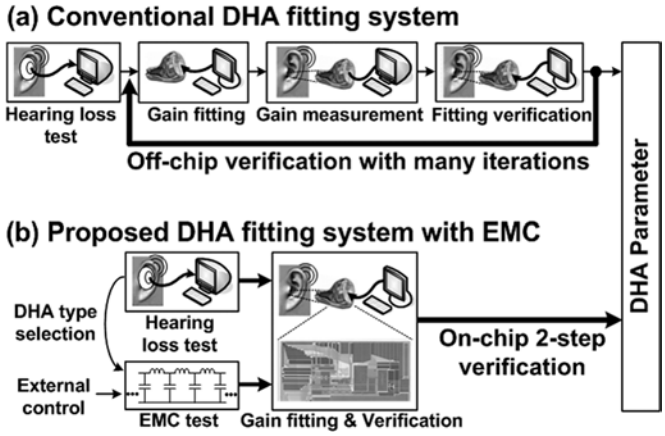

Fig. 2. Comparison of the conventional DHA and the proposed DHA with the EMC.

B. Acoustic Analogies

In the acoustic filter theory, the side branch or winding of the pipe can attenuate sound energy transmitted in a pipe. Moreover, the input impedance of the side branch determines whether the system can have as a low-pass, high-pass or bandpass filter [9].

A low-pass filter in Fig. 4 is consisting of an enlarged segment of a pipe of cross-sectional area S_1 and length L in a pipe of cross section S. At sufficiently low frequencies, the low-pass filter is viewed as a side branch with acoustic compliance C in the form of (1) as

$$C = \frac{S_1 L}{\rho_0 c^2} \tag{1}$$

where $S_1 L$ represents the volume of the expansion chamber.

In this case, the acoustic impedance of this branch is pure reactance and it is presented in the form of (2) as

$$R_g = 0, \quad X_g = -\frac{1}{C\omega} = -\frac{\rho_0 c^2}{A_1 L \omega}. \tag{2}$$

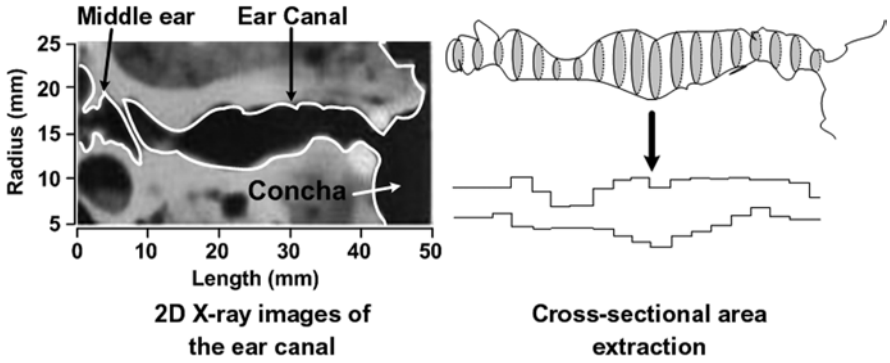

Fig. 3. Ear modeling filter circuit design.

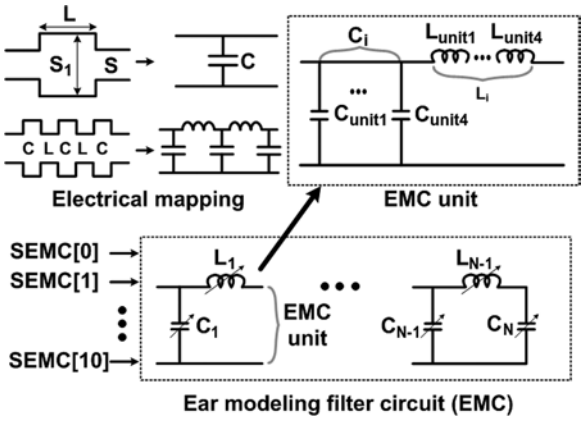

Fig. 4. Distributed *LC* filter design.

The human external ear can be modeled into the closed-ended pipe which has various windings or side branches. In addition the sliced disk of the human external ear which has unit length L is characterized into the low-pass filter according to the announced acoustic theory. By using these analogies between the closed-ended pipe of the acoustic filter and the human external ear canal, ear canal modeling filter circuit (EMC) is extracted. To design the acoustic networks using the cross-sectional area of the closed-end pipe, a ladder-type network is used as an acoustic filter. One value of inductor (L) and one value of capacitor (C) are constructed as a one unit of the proposed filter.

C. Fitting Topologies

Fig. 2(a) shows the conventional digital hearing aid fitting topology. First of all, the required gain for the fitting of the digital hearing aid is calculated and compensated to the digital hearing aid from the hearing loss test results. Next, the gain measurement is processed by wearing the gain compensated digital hearing aid. Then, the gain fitting and verification process is repeated again and again until the fitted gain value is suitable to the each individual user. However, this process requires long verification time and high fitting iterations. Fig. 2(b) presents the fabricated digital hearing aid fitting and verification topology which embeds the EMC unit. By adopting the results both from the EMC unit and the hearing loss test results, the coarse gain compensation is implemented. Then by using another hearing loss test results, the fine gain compensation is processed. This on-chip two-step verification reduces the gain fitting and verification time and error.

III. Proposed Digital Hearing Aid Circuits

A. Ear Canal Modeling Filter Circuit

Fig. 3 presents the fabricated EMC unit which models the individual ear to obtain the natural resonance values of the external ear. The exact 2-D shape of the impaired external ear can be formed based on the X-ray photo of the patient. By using the X-ray photo results the cross-sectional area of the external ear is extracted. Then, a distributed *L* or *C* filter is derived to model the acoustic filter characteristics of the external ear by using the achieved data from the X-ray photo in Fig. 4 [9]. The *LC* filter, or EMC unit, can be included into the DHA chip design process to enable so called human-chip co-design. That is, the detail characteristics of the individual external ear can be included into the design of DHA together. Even the volume change of the ear canal after the DHA is inserted into the external ear can be considered by modifying the L or C value of the EMC unit. The external control signal, 11 bit SEMC, is used to change the structure of the filter according to the shape of the individual ear to allow the high flexibility to the EMC unit. The gain parameters from the EMC unit enable the DSP in the DHA to achieve the user-optimized gain fitting in accordance with the personal hearing loss. The parameters for the fine gain fitting can input to the DHA through another serial interface. In the fabricated DHA test chip, the EMC unit is composed of 14 fixed taps and 16 variable taps, in total 30 taps. Of course total number of taps and the number of variable taps can be increased further. 11 bit SEMC signal modifies the number of taps and the *LC* values according to the individual ear shape. Among the 11 bits of the SEMC signal, 1 bit signal is to determine between the L and the C. Each L or C is composed of 4 of $L_{\rm unit}$ or $C_{\rm unit}$ to enable the trimming with 2 bit signals and 4 bit signals are allocated to select the tap among the 16 variable taps.

B. Overall Digital Hearing Aid Architecture

Fig. 5 presents the fabricated human factored digital hearing aid chip. It consists of three major blocks: the EMC unit, the parameter acquisition unit (PAU) and the DHA unit. The DHA block includes a multi-threshold preamplifier, an adaptive-SNR

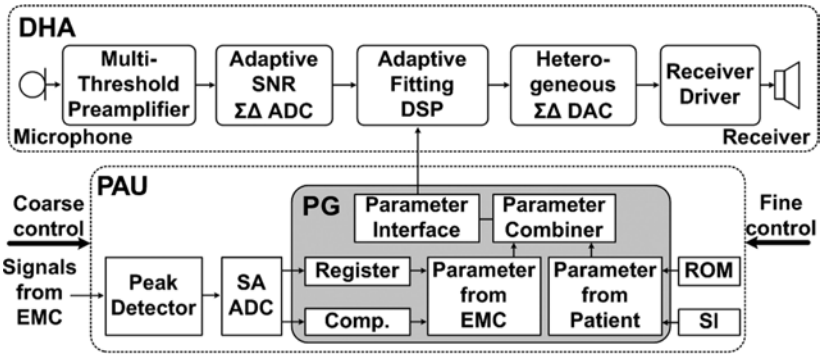

Fig. 5. Block diagram of the fabricated digital hearing aid chip.

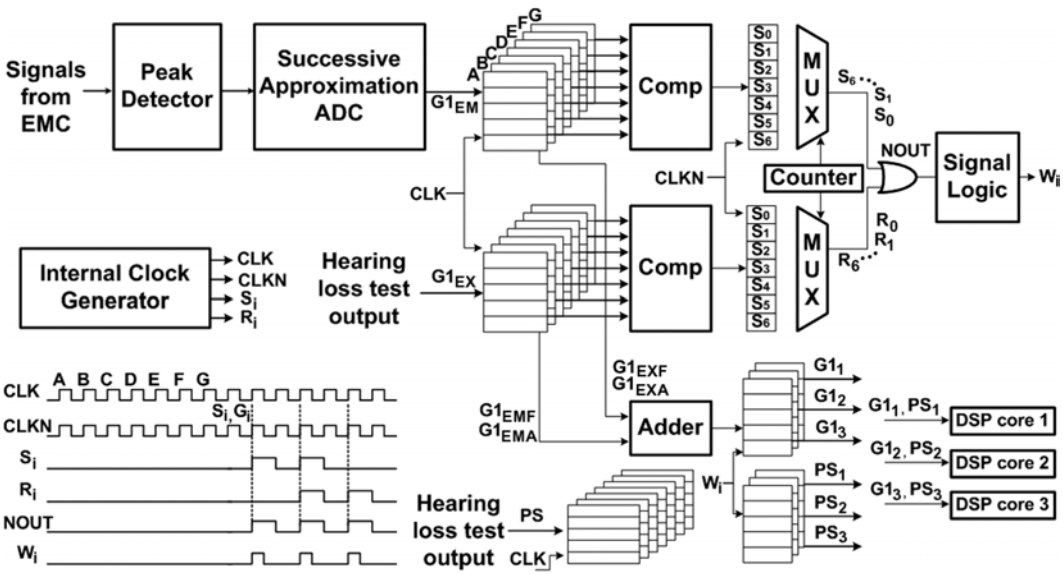

Fig. 6. Architecture of the proposed PAU with PREVA.

$\Sigma\Delta$ ADC [10], a multi-channel adaptive fitting DSP, a heterogeneous $\Sigma\Delta$ DAC [11], and a receiver driver. The PAU is composed of a peak detector (PD), a successive approximation ADC (SAADC), and a parameter generator (PG).

The PD provides the peak gain value as a function of frequency in steps of 1 kHz from 1 kHz to 8 kHz. The digitized resonance value of the individual ear is processed by the PG which receives both of the coarse compensation gain parameters and the fine compensation gain parameters. The parameters from the PG are used for the DSP of the DHA unit to achieve the user-optimized gain fitting in accordance with the personal hearing loss.

The architecture of the proposed PAU with PREVA is shown in Fig. 6. The pre fitting of the PREVA is realized by choosing the resonance value which affects the largest influence to the gain fitting. The EMC output at the 4 kHz is always selected because it highly affects the amounts of gain compensation. The largest value $(\mathrm{G1_{EMA}})$ among the outputs of the 5 bit SAADC $(\mathrm{G1_{EM}})$ and the output value at 4 kHz $(\mathrm{G1_{EMF}})$ determines the amount of the coarse compensation gain. The fine compensation gain has default initial value which can be changed by the external parameter inputs ($\mathrm{G1_{EX}}$ and PS) from the post gain verification. The peak value of the gain $(\mathrm{G1_{EXA}})$ and the gain at 4 kHz $(\mathrm{G1_{EXF}})$ are used as fine compensation gain parameters. The coarse compensation gain parameters and fine compensation gain parameters are combined to provide the total DHA gain (G1) of the DSP core.

IV. Low-Power Techniques

A. Multi-Threshold Preamplifier

Nonlinear characteristics of the human auditory system allow the native ability of the automatic gain control to enable the wide dynamic range of the human ear. In order to imitate the capability of the normal human ear which covers the wide dynamic range, the conventional preamplifier usually adopts the single threshold knee voltage with the high compression ratio of the dynamic range. However the high compression of the input dynamic range causes a serious edge distortion at the conversation region. It requires an arduous and laborious training of a patient when he or she wears the hearing aid for the first time. Moreover, the high compression of the conversation region degrades the articulation index of the hearing.

To eliminate these problems and allow a wide linearity in the normal conversation range, the programmable multi-threshold preamplifier is implemented. Fig. 7 shows the principle of the

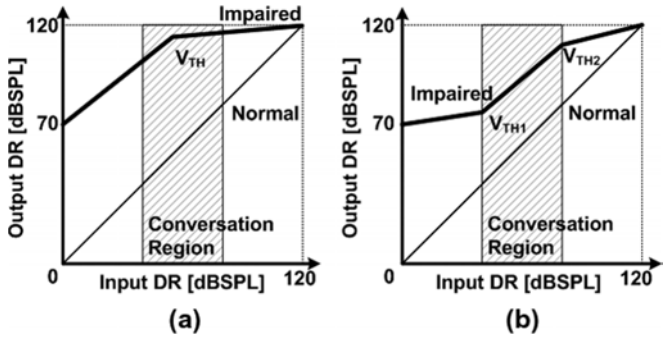

Fig. 7. Principle of the multi-threshold preamplifier. (a) Conventional preamplifier. (b) Multi-threshold preamplifier.

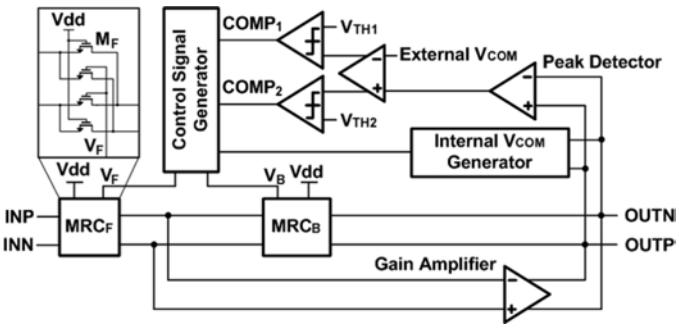

Fig. 8. Architecture of the fabricated multi-threshold preamplifier.

low-power multi-threshold preamplifier with programmable multi-threshold knee voltages. It enables the same dynamic range between the normal and the impaired ear in the conversation region. In addition, the dynamic range of the impaired ear mapped to the conversation region can be changed according to the characteristics of the each individual user by controlling the two threshold knee voltages, $V_{\rm TH1}$ and $V_{\rm TH2}$. It enhances the articulation index and flexibility of the digital hearing aid.

Fig. 8 shows the block diagram of the low-power programmable multi-threshold preamplifier. To reduce the power dissipation, only two MOS-resistive circuit (MRC) units with the gain amplifier are adopted instead of the conventional three MRC units to implement the automatic gain control function and exponential gain control function at the same time. The voltage gain of the implemented multi-threshold preamplifier is expressed in the form of (3) as

$$\begin{aligned} A_{\rm PREAMP} &= \frac{W_F L_B \left(1+\frac{V_{\rm DIF}}{V_{dd}-V_{\rm COM}}\right)}{W_B L_F \left(1-\frac{V_{\rm DIF}}{V_{dd}-V_{\rm COM}}\right)}, \\ V_F &= V_{\rm COM} - V_{\rm DIF} \\ V_B &= V_{\rm COM} + V_{\rm DIF} \end{aligned} \tag{3}$$

where V_F and V_B are negative and positive resistance control voltages, respectively, and $V_{\rm COM}$ is a volume control voltage which determines the common mode level of V_F and V_B. $V_{\rm DIF}$, the control voltage determined by the preamplifier output, decides the differential mode level of V_F and V_B. $V_{\rm TH1}$ and $V_{\rm TH2}$ are threshold voltages and W_F, W_B and L_F, L_B are the width and the length of the transistor M_F and M_B, respectively.

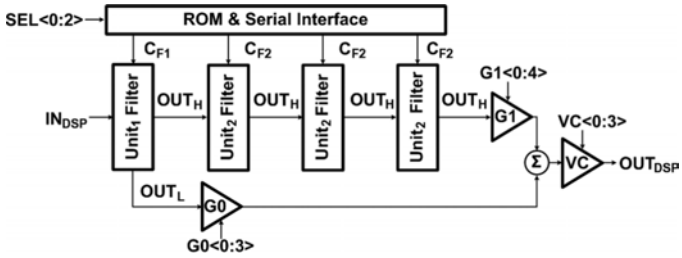

Fig. 9. Adaptive fitting DSP architecture.

When the input signal amplitude is smaller than $V_{\rm TH1}$ or larger than $V_{\rm TH2}$, the $V_{\rm DIF}$ value is selected as 0 and the V_F and V_B have the same value of $V_{\rm COM}$. Therefore, the voltage gain of the preamplifier is determined from the dimension of the MRC units and the value of the $V_{\rm COM}$. If the input signal has an amplitude value between the $V_{\rm TH1}$ and $V_{\rm TH2}$, the $V_{\rm DIF}$ has different values to provide a various gain according to the each individual user. Moreover the threshold gain is changed with the variation of the $V_{\rm COM}$ to prevent the howling problem due to the positive feedback of the input sound. By adopting this architecture, the preamplifier reduces the power consumption to 32 μW and the area occupation to 0.5 mm^2.

B. Adaptive Fitting DSP With Filter Reuse Technique

The proposed adaptive fitting DSP consists of the 1-stage $\rm unit_1$ filter and the 3-stage $\rm unit_2$ filter is shown in Fig. 9. To select the channel from 1 kHz to 8 kHz in steps of 1 kHz for low power and low area consumption, the transfer function of the DSP is implemented using symmetry formula.

Fig. 10 presents the architecture of the $\rm unit_1$ filter and the $\rm unit_2$ filter. According to the proposed symmetry formula, the transfer function of the 8 kHz channel selection has only 1 sign difference from the transfer function of the 1 kHz channel selection. Therefore, the transfer function of the 8 kHz channel selection can be designed with only adopting multiple inverters to the transfer function of the 1 kHz channel selection and it makes hardware design easy by filter reuse of the transfer function of the 1 kHz channel selection. At the same time, each transfer function between 2 kHz and 7 kHz, 3 kHz and 6 kHz, and 4 kHz and 5 kHz channel selection has only 1 sign difference with totally same formula. Among the 8 channels of the proposed DSP, the 3 channels are activated at the same time to reduce the design complexity and the power consumption. The different channels can be selected and activated according to the required frequency band of the each individual user. By using these two filters, the $\rm unit_1$ filter and the $\rm unit_2$ filter, alternatively according to the different transfer function of the DSP the adaptive fitting DSP consumes only 10 μW with the wide channel selection range.

C. Gated Successive Approximation ADC

The block diagram of the 5 bit gated successive approximation ADC (SAADC) is shown in Fig. 11. The standby current can be reduced compared with the conventional successive approximation register (SAR) [12] by adopting the control signal $\rm GCS_{0\sim4}$. Moreover, switching off the capacitor array

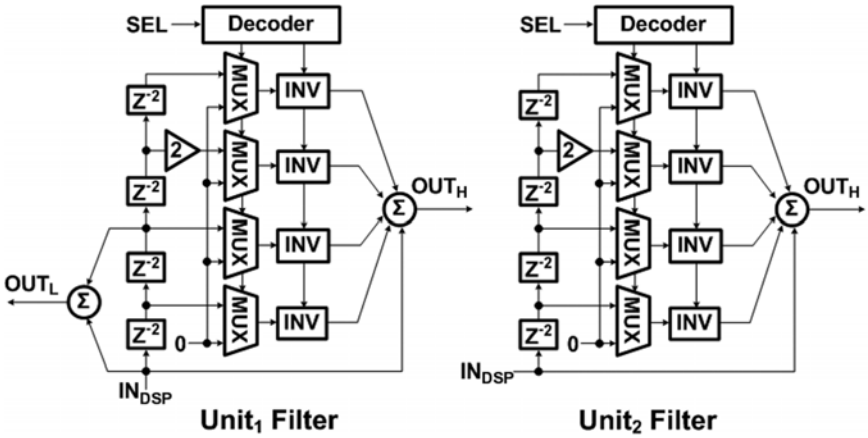

Fig. 10. Architecture of the unit_1 filter and the unit_2 filter.

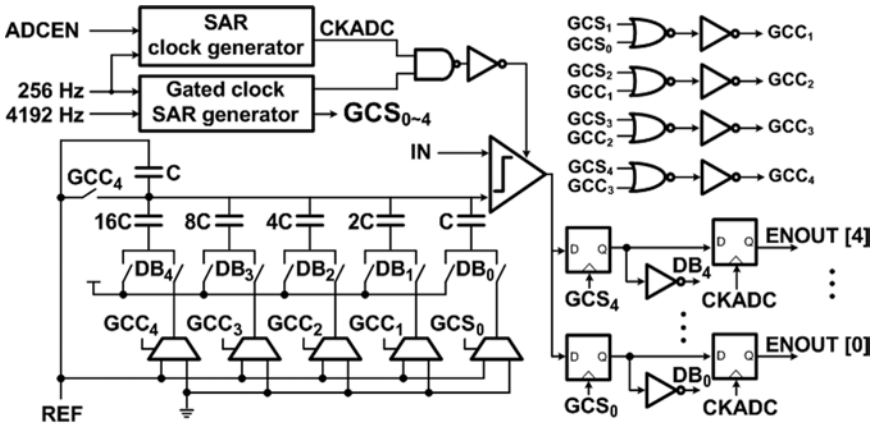

Fig. 11. Architecture of the gated successive approximation ADC.

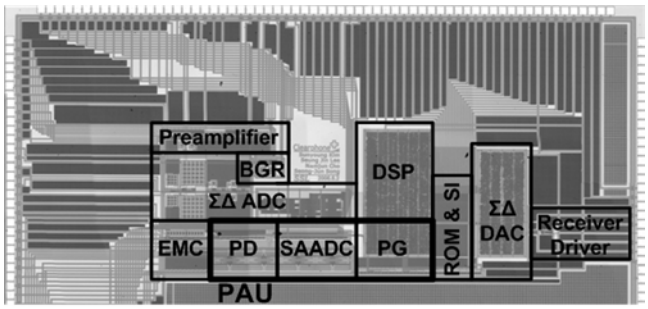

Fig. 12. Chip microphotograph of the digital hearing aid chip.

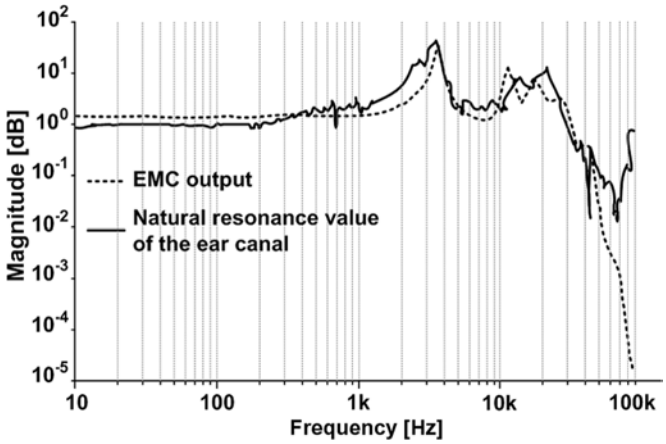

Fig. 13. Natural resonance value of the normal human ear and the EMC output.

logic decreases the power dissipation further when the comparating phase is over. The sampling rate of the designed SAADC is 256 and the effective number of bits (ENOB) is 5.7 bit when the input signal has 2 kHz frequency. The fabricated SAADC dissipates 0.8 μA on current and only 55 pA standby current.

V. Experimental Results

The chip microphotograph of the implemented digital hearing aid chip with human factors consideration is shown in Fig. 12. It was fabricated in a 0.18 μm standard CMOS technology with MIM process and its core area occupies 3.12×1.2 mm^2 [13].

Fig. 13 shows the natural resonance value of the human ear canal and fabricated EMC output. Within our interested frequency range from 1 kHz to 8 kHz, the frequency response of the EMC unit is well matched to the ear canal resonance value.

Fig. 14 shows the measured results of the proposed PAU. After the peak values of the resonance signals are detected and inputted to the PAU in Fig. 14(a), the gain values are measured in Fig. 14(b) and digitized in Fig. 14(c). Two gain values, the

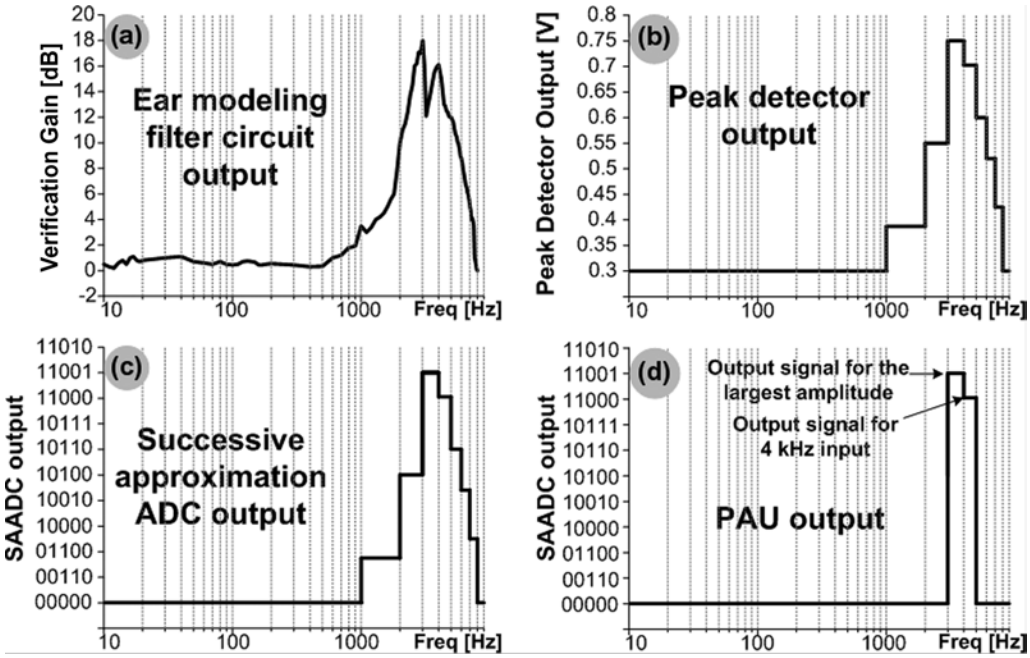

Fig. 14. Measured results of the designed PAU.

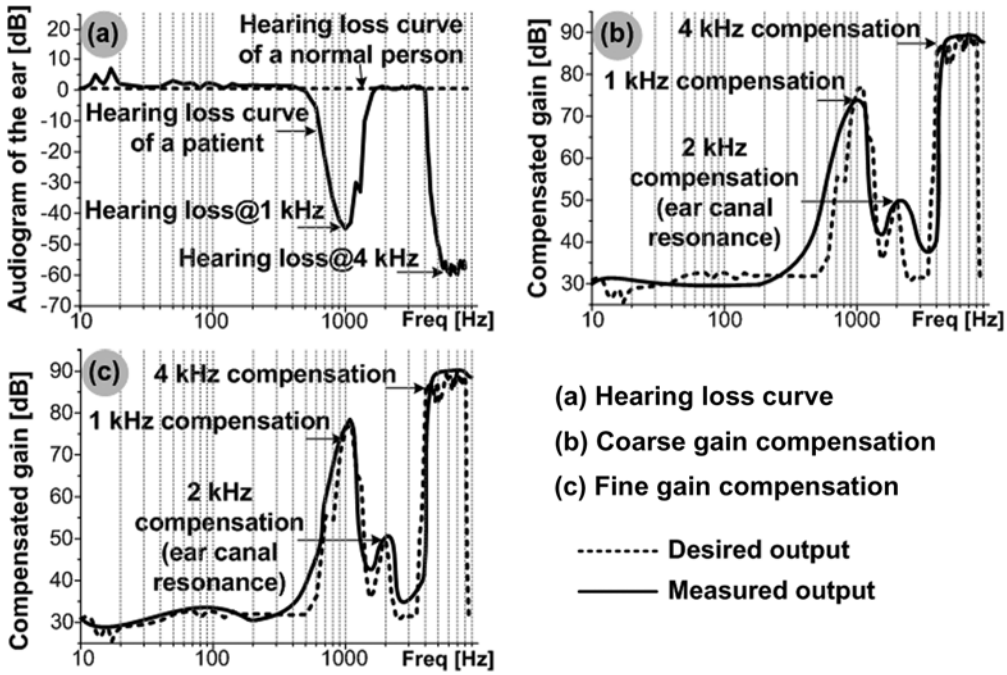

Fig. 15. Measured results of the hearing compensation operation.

largest gain value and the one at the 4 kHz, are selected to acquire the verification gain in Fig. 14(d). The overall operation of the proposed DHA is explained in Fig. 15. A hearing loss audiogram of a patient of Fig. 15(a) shows losses at 1 kHz and 4 kHz. In order to compensate such hearing losses, the EMC unit is modified to give coarse gain compensation of Fig. 15(b). The dotted line is the desired gain compensation and the solid line is the measured gain compensation by the coarse compensation only. Fig. 15(c) shows the final compensation results after the fine gain verification is processed. In this case, the preamplifier gain is selected as 1 to verify the performance of the PAU. The measured output of the multi-threshold preamplifier is shown in Fig. 16. The reported output dynamic range is from 0.45 V to 0.8 V [14].

Table I summarizes the measured features of the fabricated chip. To measure the input-referred noise voltage of the designed hearing aid chip, the output noise waveforms are recorded and divided by the digital hearing aid gain to generate a specific input-referred noise waveform [15]. The measured typical input-referred noise voltage is 4.2 μVrms and its power

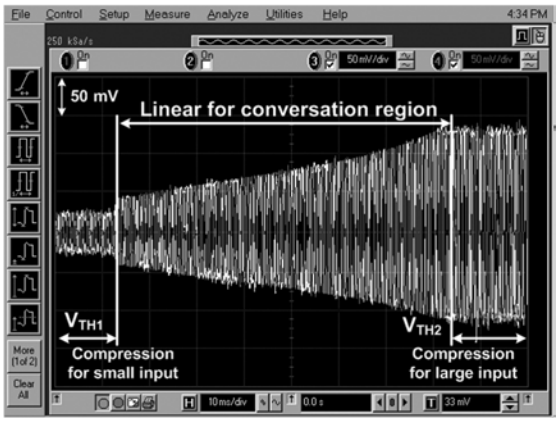

Fig. 16. Multi-threshold preamplifier output.

TABLE I
PERFORMANCE SUMMARY

Supply voltage						**0.9V**			
Peak SNR (overall system)						81dB			
Power dissipation						**70 μW(Analog) / 37 μW (Digital)**			
-3 dB bandwidth						8 kHz			
Input referred noise						4.2 μVrms			
Core area						3.12 X 1.20 mm^2			
Process						0.18 μm CMOS technology			
Pre amp	Max. gain	38 dB				**DSP & PG**	Gate count	43K	
	$DR_{Threshold}$	0.45 V - 0.8 V					DSP clock freq.	32 kHz	
ΣΔ ADC	Type	1	2	3	4		Channel	8 / 3	
	SNR_{Peak}(dB)	75	85	77	89	**SA ADC**	Sampling rate	256	
ΣΔ DAC	Gate count	16K					On current	0.8 μA	
	Input freq.	512 kHz					Standby current	55 pA	
	Clock freq.	2.048 MHz					ENOB (2 kHz)	5.7	

TABLE II
PERFORMANCE COMPARISON

	JSSC 1997 Neuteboom	**JSSC 2004 Serra-Graells**	**This work**
Supply voltage	1.3 V	1 V	**0.9 V**
Peak SNR	77 dBA	70 dB	**81 dB**
Power consumption	2 mW	200 μW	**107 μW**
Type	Digital	Programming	**Digital**
Design techniques based on human factors	No	No	**Yes (EMC, PREVA)**
# of DSP band	4	-	**8**
CMOS technology	Low V_{TH} 0.8 μm	1.2 μm	**0.18 μm**

consumption is 107 μW using a single 0.9 V supply. Table II presents the performance comparison with the other works related to the hearing aid chip. The main points in this table are design techniques based on the internal verification and the power dissipation. Compared with the conventional DHA, the fabricated digital hearing aid chip enables the accurate and fast on-chip gain fitting and verification by incorporating the human factors. As a result, this work newly introduces the EMC and the PREVA with the lowest power consumption.

VI. CONCLUSION

The human factors considered digital hearing aid chip is designed and implemented. The ear canal modeling filter circuit (EMC) models the human external ear into the distribute *LC* filter by adopting the analogies between the acoustic filters and the characteristics of the human external ear. It enables the coarse gain fitting based on the shape of the external ear. This chip adopts the pre fitting verification algorithm (PREVA) to achieve the gain fitting and verification in two steps, coarse and fine gain fittings accurately and rapidly. The fine gain fitting and verification is performed by the external inputs from the hearing loss test results. To reduce the power dissipation of the human factored digital hearing aid chip, the multi-threshold preamplifier is designed. The dynamic range of the multi-threshold preamplifier exists from 0.45 V to 0.8 V and dissipates only 32 μW from a single 0.9 V supply by using two MRC units with the gain amplifier. The multi-channel adaptive fitting DSP and the gated successive approximation ADC are implemented to reduce the power consumption further. The fabricated human factors considered digital hearing aid chip achieves the input referred noise voltage of 4.2 μVrms with the peak SNR of 81 dB in the overall system. It occupies the core area of $3.12 \times 1.20\,mm^2$ in a 0.18 μm standard CMOS technology and consumes only 107 μW from a single 0.9 V supply.

REFERENCES

[1] S.-J. Song, N. Cho, S. Kim, J. Yoo, and H.-J. Yoo, "A 2 Mb/s wideband pulse transceiver with direct-coupled interface for human body communications," in *IEEE ISSCC Dig. Tech. Papers*, 2006, pp. 558–559.
[2] S.-J. Song, N. Cho, S. Kim, J. Yoo, S. Cho, and H.-J. Yoo, "A 0.9 2.6 mW body-coupled scalable PHY transceiver for body sensor applications," in *IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 366–367.
[3] S. Kim, S. J. Lee, N. Cho, S.-J. Song, and H.-J. Yoo, "A fully integrated digital hearing aid chip with human factors considerations," in *IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 154–155.
[4] S. E. Voss and J. B. Allen, "Measurement of acoustic impedance and reflectance in the human ear canal," *J. Acoust. Soc. Amer.*, vol. 95, no. 1, pp. 372–384, Jan. 1994.
[5] P. G. Stelmachowicz, B. Hoover, D. E. Lewis, and M. Brennan, "Is functional gain really functional?," *Hearing J.*, vol. 55, no. 11, pp. 38–42, Nov. 2002.
[6] R. Z. Gan, B. Feng, and Q. Sun, "Three-dimensional finite element modeling of human ear for sound transmission," *Ann. Biomed. Eng.*, vol. 32, no. 6, pp. 847–859, Jun. 2004.
[7] R. L. Goode, M. Killion, K. Nakamura, and S. Nishihara, "New knowledge about the function of the human middle ear: Development of an improved analog model," *Amer. J. Otol.*, vol. 15, no. 2, pp. 145–154, Mar. 1994.
[8] R. Aibara, J. T. Welsh, S. Puria, and R. L. Goode, "Human middle-ear sound transfer function and cochlear input impedance," *Hearing Res.*, vol. 152, no. 2, pp. 100–109, Feb. 2001.
[9] D. R. Raichel, *The Science and Applications of Acoustics*, 1st ed. New York: AIP Press, 2000.
[10] S. Kim, J.-Y. Lee, S.-J. Song, N. Cho, and H.-J. Yoo, "An energy-efficient analog front-end circuit for a sub-1-V digital hearing aid chip," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 876–882, Apr. 2006.
[11] S. Kim, N. Cho, S.-J. Song, D. Kim, K. Kim, and H.-J. Yoo, "A 0.9-V 96- μW digital hearing aid chip with heterogeneous $\Sigma - \Delta$ DAC," in *Symp. VLSI Circuits Dig. Tech. Papers*, 2006, pp. 68–69.
[12] M. D. Scott, B. E. Boser, and K. S. J. Pister, "An ultralow-energy ADC for smart dust," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1123–1129, Jul. 2003.
[13] S. Kim and H.-J. Yoo, "A fully integrated digital hearing aid with human external canal considerations," Patent pending.
[14] S. Kim and H.-J. Yoo, "Dual threshold preamplifier for a digital hearing aid," Patent pending.
[15] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.

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