An Energy-Efficient Analog Front-End Circuit for a Sub-1-V Digital Hearing Aid Chip

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***Abstract*—A low-power energy-efficient adaptive analog front-end circuit is proposed and implemented for digital hearing-aid applications. It adopts the combined-gain-control (CGC) technique for accurate preamplification and the adaptive-SNR (ASNR) technique to improve dynamic range with low power consumption. The CGC technique combines an automatic gain control and an exponential gain control together to reduce power dissipation and to control both gain and threshold knee voltage. The ASNR technique changes the value of the signal-to-noise ratio (SNR) in accordance with input amplitude in order to minimize power consumption and to optimize the SNR by sensing an input signal. The proposed analog front-end circuit achieves 86-dB peak SNR in the case of third-order $\Sigma\Delta$ modulator with 3.8-μVrms of input-referred noise voltage. It dissipates a minimum and maximum power of 59.4 and 74.7 μW, respectively, at a single 0.9-V supply. The core area is 0.5 mm^2 in a 0.25-μm standard CMOS technology.**

***Index Terms*—Adaptive-SNR technique, analog front-end, combined-gain-control technique, digital hearing aid.**

I. Introduction

RECENTLY, the rapid expansion of the biomedical-electronic market has necessitated low-power and low-voltage biomedical systems [1], [2]. Since battery power is used for most of the portable biomedical devices, expanding battery lifetime with low power dissipation systems is very crucial. In the digital hearing-aid applications, the battery is typically made of zinc–air and should offer a life span of at least two weeks at 10 hours use per day [3]. Moreover, the digital hearing aid requires wide dynamic range, high performance, more programmability, and small form factor. Hence, it is necessary to achieve low power dissipation, high-performance, and programmability to expand battery lifetime and to offer convenient hearing to the users.

Adopting extremely low supply voltage is an attractive solution to reduce power dissipation because the power dissipation of a system is strongly dependent upon its supply voltage. However, low supply voltage generally causes significant degradation of the system performance and complicates the analog circuit design. For example, the accuracy and the dynamic range of the analog front-end circuit may suffer from the low supply voltage due to reduced voltage headroom. By adopting a smart power management unit, the power consumption can be reduced. However, extra power dissipation due to the power management unit can occupy a large part of total system power because a digital hearing aid consumes extremely low total power. In addition, it is very hard to design a low-power high-performance power management unit.

In this paper, we introduce two design techniques, combined-gain-control (CGC) and adaptive-SNR (ASNR) techniques to design a low-power and high-performance analog circuit achieving high accuracy and wide dynamic range for digital hearing aid.

This paper is organized as follows. The design considerations of a hearing-aid system and the proposed low-power design methodologies are presented in Section II. Section III describes in detail the low-power design methods and circuits of the analog front-end with the proposed low-power techniques. In Section IV, real chip implementation and its measurement results are presented. Finally, conclusions are made in Section V.

II. System Design Considerations

There have been continual attempts to design hearing-aid systems which satisfy both low-power and high-performance characteristics [4]–[6]. Generally, a high-performance hearing aid needs high-performance building blocks, especially in analog and mixed parts. This tradeoff has been an obstacle to the design of a low-power and high-performance hearing-aid system.

In order to achieve a high-performance hearing-aid system, various circuit techniques have been used such as adaptive noise reduction [7]. This achieved wide dynamic range with personal calibration to attenuate noise level independently in each frequency band. However, this algorithm is only focused on performance improvement and consumes extra power due to additional functional blocks. This is clear evidence that a high-performance hearing-aid system inevitably dissipates excessive power and needs a distinct power management unit to control power consumption.

The conventional digital hearing-aid system consists of five blocks: a preamplifier, a $\Sigma\Delta$ analog-to-digital converter, a digital signal processor, a $\Sigma\Delta$ digital-to-analog converter, and a receiver driver. Among these individual blocks, the analog front-end that comprises a preamplifier and an $\Sigma\Delta$ modulator accounts for most of the power consumption: about 74% [8], [9]. The analog front-end should consume less than 370 μW if the allowed power budget of the digital hearing aid is 500 μW. Therefore, to reduce the power consumption and enhance the performance of the digital hearing aid, this work will be focused

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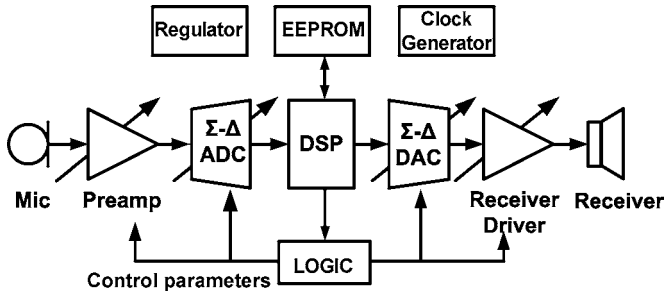

Fig. 1. Block diagram of proposed hearing-aid system.

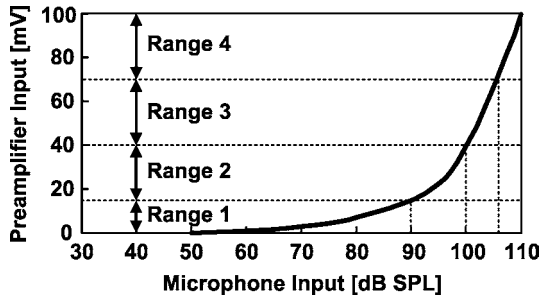

Fig. 2. Characteristics of microphone for digital hearing aid.

on the power reduction of the analog front-end of the digital hearing aid.

In order to obtain both low power and high performance, this paper proposes a design method with dynamically varying structure. Fig. 1 shows the proposed hearing-aid system. By controlling both the structure and clock frequency adaptively, the proposed hearing-aid system changes the signal-to-noise ratio (SNR) value dynamically and accomplishes both the low power dissipation and high performance. The gain and threshold voltage of the preamplifier can be modified to reduce the power further according to the input amplitudes.

III. Proposed Analog Front-End Circuits

An automatic gain control (AGC) is necessary for the preamplifier to maintain hearing ability of the users against sudden temporal changes and unnecessary external loud sound. These unexpected variations of sound may exceed the dynamic range of the user's hearing ability and they feel pain, and even their ability to hear may be damaged [10]. By suppressing the amplitude of the output signal of the hearing aid beyond the threshold knee point of AGC, the hearing ability of the patients can be preserved. The exponential gain control (EGC) circuit is required as a volume control because the human sensibility of sound operates on a logarithmic scale. In a conventional preamplifier, these two functional blocks are designed separately because of the design difficulties in standard CMOS technology [11], [12].

In this work, we devise a CGC technique to combine AGC and EGC successfully into a single block and the power consumption can be far reduced with accurate preamplification. The CGC brings about even the gain controllability. In contrast to the fixed threshold voltage of the conventional preamplifier, the proposed CGC preamplifier can change the gain threshold voltage with an external control signal.

The conventional $\Sigma\Delta$ modulator uses only one clock and has only one SNR value. On the contrary, the ASNR $\Sigma\Delta$ modulator can have, by the combination of two different clock frequencies and two different configurations, four different SNR values. In addition, by controlling both the order and clock frequency according to the input conditions, the proposed ASNR $\Sigma\Delta$ modulator can achieve wide dynamic range with low power consumption.

Fig. 2 shows the relationship between the input of the microphone and the input of a preamplifier. The preceding study revealed that a normal sound level common in human daily life ranges from 30- to 90-dB SPL, which corresponds to Range 1 [13]. In this range, the amplitude of the input sound is so small that a high-gain analog front-end must be used. On the other hand, above 90-dB SPL, from Range 2 to Range 4, the sound level is sufficiently large that the analog front-end needs not to provide high SNR. Since many dangerous signal levels such as automobile horns or fire alarms are usually over the 100 dB SPL, these ranges are essential for the user's safety.

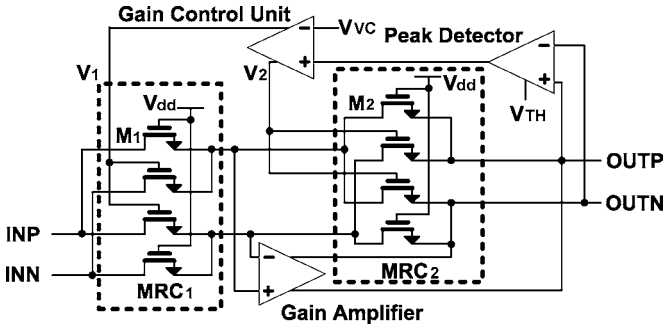

Fig. 3. Proposed preamplifier with CGC technique.

If we use a high performance analog front-end for all sound regions, the analog front-end produces excessively high performance and dissipates large power needlessly. In the design of the proposed analog front-end, the input sound level is divided into four parts to control the SNR separately at each range so as to optimize power and performance. To classify and extract control parameters, the proposed analog front-end includes an off-chip DSP.

A. Low-Power Low-Voltage Adaptive Analog Front-End Design

Fig. 3 shows the proposed preamplifier with the CGC technique. The conventional preamplifier is usually composed of an operational amplifier and three feedback MOS resistive circuit (MRC) blocks to implement the AGC function [14]. However, in this preamplifier, only two MRC blocks are used as feedback resistors to get the exponential gain characteristics with the gain amplifier.

The threshold gain and the threshold knee point of the preamplifier can be changed by varying $V_{\rm VC}$ and $V_{\rm TH}$, respectively. To control the threshold knee voltage, the peak detector senses the outputs of the gain amplifier and generates the scaled envelope. In this scheme, if the amplitude of the generated envelope is larger than control signal $V_{\rm TH}$, the generated envelope is applied to the gain control unit directly. However, if it is not, a fixed control signal determined by $V_{\rm TH}$ is applied to the gain control unit instead of the envelope of the gain amplifier output.

The threshold gain can be changed with the variation of the $V_{\rm VC}$. The control signal $V_{\rm VC}$ acts as a common-mode voltage level of the integrator which is composed of two MRC blocks and the gain amplifier. When the value of $V_{\rm VC}$ is low, the threshold gain is decreased and the power dissipation of the preamplifier is reduced. On the other hand, when the value of $V_{\rm VC}$ is high, the threshold gain increases and the required resolution of the next-stage $\Sigma\Delta$ modulator is decreased.

To achieve the exponential gain characteristics in the case of CMOS technology, a pseudo-exponential polynomial as given in (1) is used to approximate the logarithmic function:

$$\text{gain} = \left(\frac{1+x}{1-x}\right). \tag{1}$$

In Fig. 3, by using two MRC blocks as feedback resistors, the gain of the proposed preamplifier is given as follows:

$$A_V = \frac{R_{\rm MRC2}}{R_{\rm MRC1}} = \frac{W_1 L_2 (V_{dd} - V_1)}{W_2 L_1 (V_{dd} - V_2)}. \tag{2}$$

Therefore, the voltage gain of the proposed preamplifier is expressed in the form of (1) as

$$A_V = \frac{V_{\rm OUT}}{V_{\rm IN}} = \frac{W_1 L_2 \left(1 + \frac{V_X}{V_{dd} - V_{\rm VC}}\right)}{W_2 L_1 \left(1 - \frac{V_X}{V_{dd} - V_{\rm VC}}\right)}, \quad \begin{matrix} V_1 = V_{\rm VC} - V_x \\ V_2 = V_{\rm VC} + V_X \end{matrix} \tag{3}$$

where $V_{\rm TH}$ is the threshold knee voltage control parameter and V_1 and V_2 are resistance control voltages generated by the gain control unit. $V_{\rm VC}$ is a volume control voltage that determines the common-mode level of V_1 and V_2. V_X decides the differential-mode level of V_1 and V_2. W_1, W_2 and L_1, L_2 are the widths and lengths of the transistors M_1 and M_2, respectively. V_{dd} is the supply voltage of the analog front-end circuit. The exponential gain control function can be implemented by controlling $V_{\rm VC}$ and V_X, respectively, with the gain amplifier and only two MRC blocks.

To avoid the effects of the supply voltage fluctuation from the clock generator, the power supply of the preamplifier and $\Sigma\Delta$ modulator is separated from the logic blocks. Moreover, a bandgap voltage reference circuit is used to reduce the power supply noise. Therefore, the $R_{\rm MRC}$ value has noise immunity enough to guarantee the performance of the preamplifier although the MRC block uses the supply voltage V_{dd} as one of its control signal.

To design an adaptive analog front-end, the proposed $\Sigma\Delta$ modulator should provide various SNR values to reduce power dissipation according to the input amplitudes. By changing the clock frequency, the $\Sigma\Delta$ modulator achieves different SNR characteristics. However, high clock frequency incurs a number of difficulties in the design of an analog circuit such as an operational transconductance amplifier (OTA). This is because the unity-gain frequency of the OTA should be at least four times higher than the clock frequency of the $\Sigma\Delta$ modulator in the single-loop topology of this study [15]. A high-order $\Sigma\Delta$ modulator is an alternative approach to modify SNR values. However, the higher order single-loop $\Sigma\Delta$ modulator of more than third order seriously suffers from instabilities caused by the saturation of the integrator and nonlinearities of the 1-bit quantizer due to the large input level [16]. It limits the enhancement of SNR through increasing the order of the $\Sigma\Delta$ modulator.

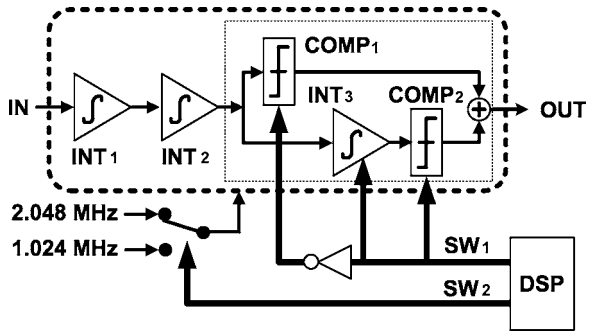

Fig. 4. Proposed $\Sigma\Delta$ modulator exploiting adaptive-SNR technique.

One possible method to reduce power dissipation is to adopt the dynamic structure variation technique [17]. By selecting the appropriate structure among the multi-subsystems, the desired system can reduce its power dissipation dynamically, but it occupies a great deal of chip area. Therefore, to adopt the adjustable system structure for low power dissipation with little area penalty, we introduce the ASNR $\Sigma\Delta$ modulator technique. For easy analog circuit design, the clock frequency is selected between 1.024 and 2.048 MHz. In order to minimize side effects of the higher order $\Sigma\Delta$ modulators, the order is limited under three.

The proposed $\Sigma\Delta$ modulator is described in Fig. 4. SW_1 determines the order of the $\Sigma\Delta$ modulator between the second and the third while SW_2 decides its clock frequency. A combination of these switches allows the $\Sigma\Delta$ modulator to obtain four different SNR values. The control parameters of the $\Sigma\Delta$ modulator are externally stored and applied by the control register and the DSP for easy and convenient management. By selecting the proper parameters according to the input amplitudes, the $\Sigma\Delta$ modulator obtains optimal SNR value in terms of power consumption and performance.

Fig. 5 shows the detailed architecture of the $\Sigma\Delta$ modulator. When the $/SW_1$ is closed, it operates in the second order by bypassing the output from the second integrator to the OUTN or OUTP. Because the resistance value of the conventional N-type switch varies according to the drain voltage level, the output signal of the second integrator is degraded seriously when it passes through $/SW_1$. To prevent signal distortion, a high-performance switch, of which resistance value is constant under the entire range of the drain voltage, is necessary. However, the high-performance switch is difficult to design and consumes additional power. Therefore, we adopt $\rm COMP_1$, which converts the second integrator output into a PWM signal and transfers signals through the $/SW_1$ without distortion. Because the outputs of the $\rm COMP_1$ and $\rm COMP_2$ are digital signals, i.e., V_{dd} or V_{ss}, the noises such as clock feedthrough or kick-back caused

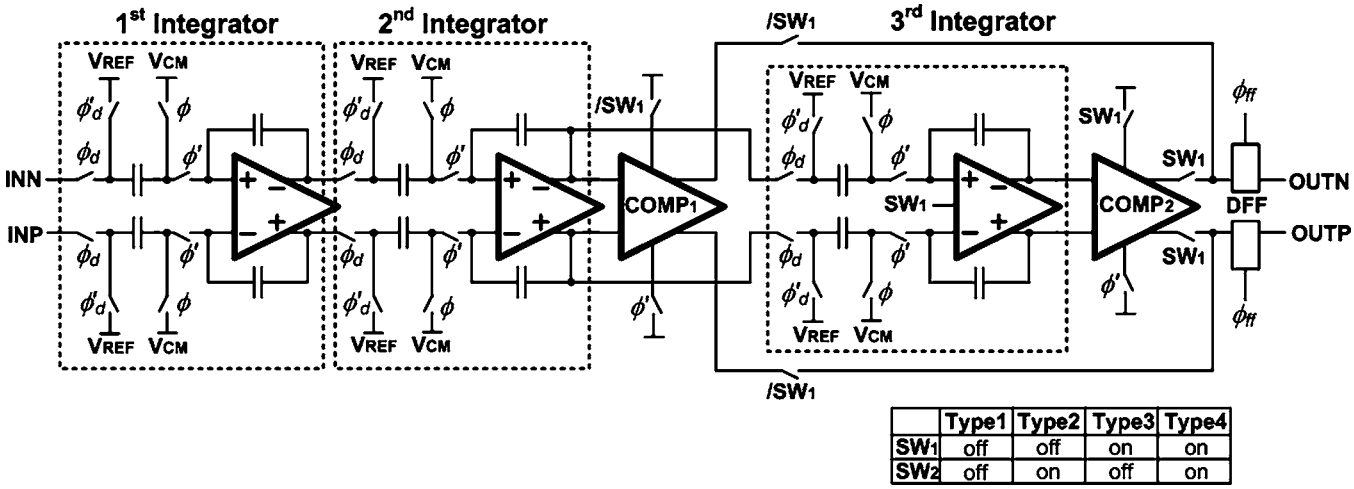

Fig. 5. Detailed $\Sigma\Delta$ modulator architecture.

TABLE I
PERFORMANCE SUMMARY

Order		2nd order		3rd order	
SW_1 & SW_2		00 (Type1)	01(Type2)	10(Type3)	11(Type4)
Clock frequency		1.024-MHz	2.048-MHz	1.024-MHz	2.048-MHz
Peak SNR		72-dB	81-dB	78-dB	86-dB
Power dissipation	Σ-Δ modulator	26.4-μW	26.8-μW	35.7-μW	36.7-μW
	Preamplifier	V_{VC}=0.75-V	V_{VC}=0.8-V	V_{VC}=0.85-V	
		33-μW	35-μW	38-μW	
	Analog front-end	59.4~74.7-μW (According to the parameter value)			
-3dB bandwidth		8-kHz			
Input-referred noise		3.8-μVrms			
Supply voltage		0.9-V			
Core area		0.5-mm^2			
Technology		0.25-μm standard CMOS technology			

by switch nonidealities seldom degrade the SNR of the proposed $\Sigma\Delta$ modulator.

When the COMP_1 is activated, the third integrator and COMP_2 are completely turned off so as to eliminate extra power consumption. On the other hand, if the $/SW_1$ is opened, the third integrator accepts the output of the second integrator as an input and performs the third-order modulation. In this phase, COMP_1 is turned off to avoid extra power dissipation. By turning SW_2 on and off, the clock frequency is changed between 2.048 and 1.024 MHz, respectively.

By changing SW_1 and SW_2 separately, four configurations of the $\Sigma\Delta$ modulator having different kinds of SNR are obtained, as summarized in Table I. With SW_1 open, the second-order $\Sigma\Delta$ modulators of type 1 and type 2 are achieved by turning SW_2 off and on, respectively. With SW_1 closed, the third-order $\Sigma\Delta$ modulators of type 3 and type 4 are realized by turning SW_2 off and on, respectively.

To avoid the discontinuity problems which can happen when the order or clock frequency is changed, the proposed $\Sigma\Delta$ modulator uses the gain control unit of the preamplifier in Fig. 3. This gain control unit adopts the envelope of the output signal and modifies the preamplifier gain by controlling the V_{VC} value to preserve the continuity of the SNR characteristics of the $\Sigma\Delta$ modulator.

B. Building Block Circuits Design

In Fig. 6, a circuit design of a low-power OTA for the proposed $\Sigma\Delta$ modulator is shown. It has a compensated two-stage which is composed of an input stage with a cross-coupled active load and a class-AB output stage. By using the pMOS input differential pair, the common-mode level of the OTA gets lower, near to ground level. This allows the use of small nMOS transistors for the switches of the $\Sigma\Delta$ modulator. Moreover, the pMOS input differential pair can minimize the output noise due to its small 1/f noise and optimizes the slew rate and unity-gain frequency [18].

The designed OTA demonstrates 77.6-dB DC gain, 7.07-MHz unity gain bandwidth, 55° phase margin for a 3-pF load, and power consumption is 15 μW. To reduce the offset errors of the OTA in the first integrator, the $\Sigma\Delta$ modulator adopts the correlated double sampling technique. Because the supply voltage level is low, proper biasing of the analog circuit is essential to achieve accurate operation. To solve the biasing problem, the OTA is designed to operate in the condition of

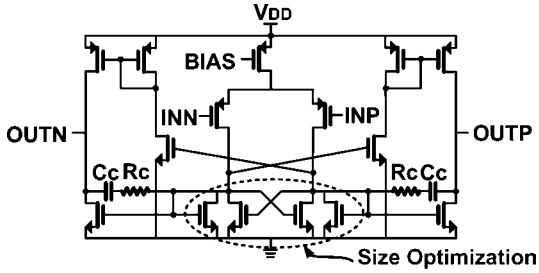

Fig. 6. Two-stage class-AB OTA.

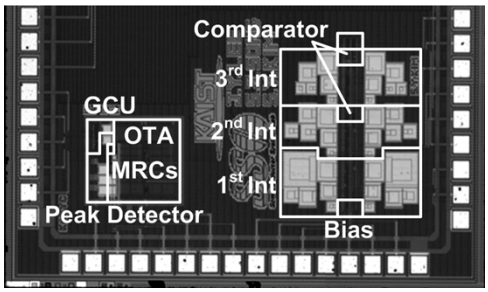

Fig. 7. Chip microphotograph of the proposed analog front-end.

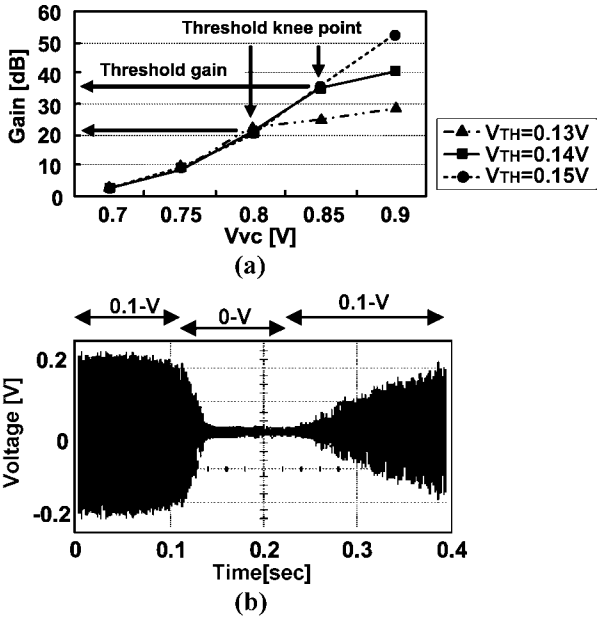

Fig. 8. Measured performance of the CGC preamplifier. (a) Threshold knee voltage and threshold gain variations. (b) Attack and release responses.

$V_{\rm eff} = V_{\rm GS} - V_{\rm TH} \approx 90$ mV. Therefore, the proposed OTA achieves low power consumption with moderate speed and area.

A 1-bit quantizer of $\rm COMP_1$ and $\rm COMP_2$ with a clocked circuit is adopted [19]. By adapting the regenerative quantizer with clocked circuit, low hysteresis and low offset voltage can be obtained [20].

IV. Experimental Results

The chip microphotograph of the proposed analog front-end circuit is shown in Fig. 7. It was fabricated in a 0.25-μm standard CMOS technology with MIM capacitor process and its core size is 0.5 mm^2.

In Fig. 8(a), the measured threshold gain and the threshold knee point variations of the CGC preamplifier are presented as a function of $V_{\rm VC}$ with variation of $V_{\rm TH}$. The threshold knee points are determined by values of $V_{\rm TH}$. By reducing $V_{\rm TH}$, the threshold knee point is decreased. The measured attack and release response is shown in Fig. 8(b). The effect of sudden 25-dB drop in input voltage level to the output signal is measured. It shows a fast gain recovery such as after a 0.1-s delay, its output gain increases gradually according to the input level.

The measured performance of the proposed $\Sigma\Delta$ modulator is presented in Fig. 9(a). It shows the measured output spectrum of the second-order modulator with 2-kHz sinusoidal input signal and 1.024-MHz clock frequency. Under these conditions, the measured peak SNR is measured as 72 dB and peak signal-to-noise-and-distortion ratio (SNDR) is 70 dB in the case of type 1. Fig. 9(b) shows the simulated and measured SNR and SNDR as a function of the input signal which is normalized by reference voltage. The high-level simulation results reveals that the proposed $\Sigma\Delta$ modulator accomplishes different SNR and SNDR values according to the input amplitudes compared with those of the conventional second- and third-order $\Sigma\Delta$ modulator.

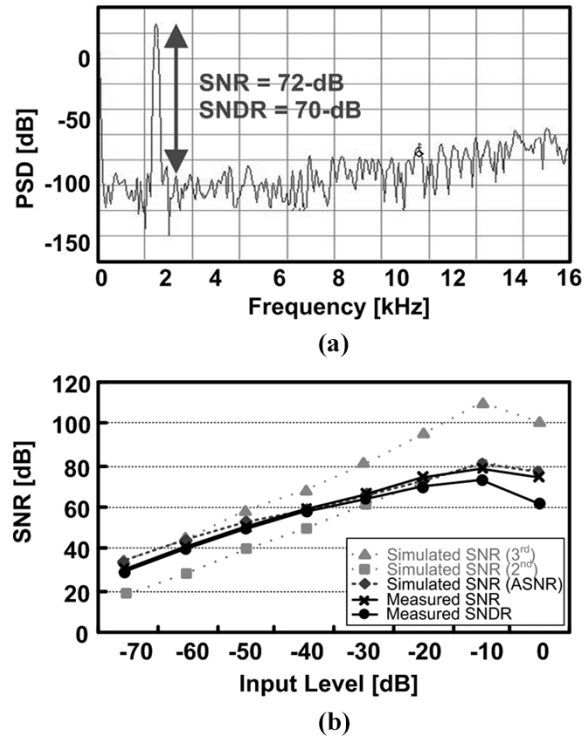

Fig. 9. Measured performance of the ASNR $\Sigma\Delta$ modulator. (a) Spectrum characteristics. (b) Simulated and measured SNR/SNDR versus input amplitude.

Fig. 10 shows a comparison of the power consumption between other analog front-end circuits and the proposed analog front-end according to the input amplitudes. While the power dissipation of the conventional analog front-ends is independent of the input amplitude, i.e., a fixed architecture, the power consumption of the proposed adaptive analog front-end varies according to the input amplitude. By adopting the CGC and the

TABLE II
PERFORMANCE COMPARISON OF THE ANALOG FRONT-END

	JSSC 1997 [4]	JSSC 2002 [5]	This work
Supply Voltage	2.15-V	1.1-V	0.9-V
Power Consumption	323-μW	190-μW	59.4-μW
Peak SNR	77-dB	92-dB	86-dB
Technology	0.8-μm CMOS	0.6-μm CMOS	0.25-μm CMOS

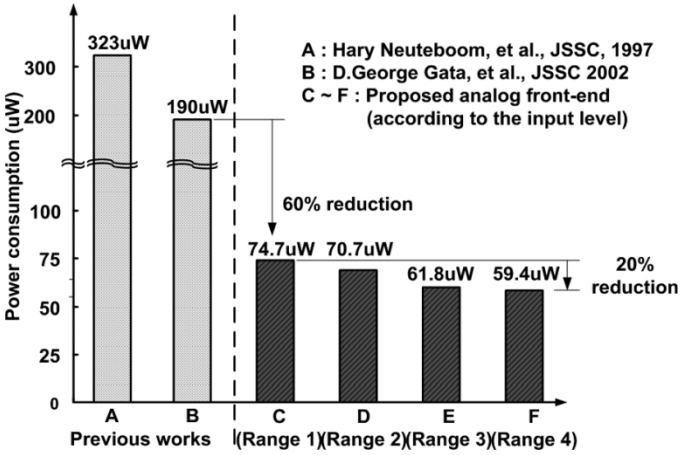

Fig. 10. Power consumption of the conventional versus proposed analog front-end.

ASNR technique, a 20% reduction of power dissipation is obtained from Range 1 to Range 4.

The measured performance of the proposed analog front-end is summarized in Table I. When the input amplitude is higher than 105-dB SPL, the $\Sigma\Delta$ modulator acts as a type 1 modulator to reduce power dissipation effectively. However, if the input amplitude is lower than 90-dB SPL, it operates as a type 4 to offer a high SNR. This allows efficient usage of the limited energy of the zinc–air battery which is typically used in digital hearing aids.

To measure the input-referred noise voltage of the proposed preamplifier, the output noise waveforms are recorded and are divided by the preamplifier gain to generate the specific input-referred noise waveform [21]. The measured typical input-referred noise voltage is 3.8 μVrms.

The second- and third-order $\Sigma\Delta$ modulators enhance the SNR by 9 and 8 dB, respectively, with a shift of clock frequency from 1.024 to 2.048 MHz, respectively. The extra power dissipation due to frequency change is less than 1 μW for each type of modulator.

Table II compares the performance of the proposed analog front-end circuit with that of previous works. The proposed analog front-end circuit dissipates the lowest power: 59.4 μW at power supply voltage of 0.9 V.

V. CONCLUSION

A low-power and energy-efficient analog front-end is proposed and implemented in a 0.25-μm standard CMOS process for possible application to digital hearing aids. By exploiting CGC and adaptive-SNR technique, the proposed analog front-end reduces power consumption and obtains large dynamic range and optimized power consumption with respect to the variation of input signals. CGC combines AGC with EGC to give wide dynamic range. ASNR dynamically changes the order of the $\Sigma\Delta$ modulator and its operating frequency to obtain different SNR values.

The peak SNRs are 72 and 86 dB in the case of second- and third-order $\Sigma\Delta$ modulators, respectively, and the input-referred noise voltage is 3.8 μVrms. The active area of the test preamplifier is 0.1 mm^2 and of the sigma-delta modulator is 0.4 mm^2.

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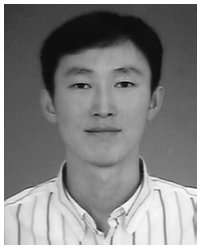

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