An Energy-Efficient Analog Front-End Circuit for a Sub-1V Digital Hearing Aid Chip

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Abstract

A low-power, energy-efficient analog front-end circuit is proposed and implemented for a digital hearing aid chip. It adopts the combined-gain-control (CGC) technique for an accurate preamplification and the adaptive-SNR (ASNR) technique for an improvement of dynamic range with low power consumption. The proposed analog front-end achieves 87-dB peak SNR and dissipates 60-μW from a single 0.9-V supply. The core area is 0.5-mm^2 in a 0.25-μm standard CMOS technology.

Keywords: analog front-end, adaptive SNR technique, combined-gain-control technique, digital hearing aid

Introduction

Recently, the tremendous increase of the biomedical-electronic-system market requires new design techniques for low-power and low-voltage operations [1]. It is necessary to achieve both of the low power dissipation and high performance for a digital hearing aid system. The conventional digital hearing aid system consists of five blocks: a preamplifier, a Σ-Δ analog-to-digital converter, a digital signal processor, a Σ-Δ digital-to-analog converter, and a receiver driver. Among them, an analog front-end composed of a preamplifier and a Σ-Δ modulator takes most of power consumption [2], [3]. Therefore, reducing its power dissipation is an effective method to decrease the system power consumption as well. Adopting extremely low supply voltage may be an attractive solution to reduce power dissipation. However, it mostly brings up a significant degradation of a system performance and makes an analog circuit design difficult.

The accuracy and the dynamic range of the analog front-end circuit greatly depend on the performance of the analog circuit. For the fine operation, high performance analog circuit is essential but it is usually not optimized for low power dissipation. In this paper, we introduce two new design techniques, combined-gain-control (CGC) and adaptive-SNR (ASNR) techniques, to design the low-power and high-performance analog circuit achieving high accuracy and wide dynamic range.

This paper presents the design considerations on the analog front-end and the methodologies of the low power design techniques. Furthermore, detailed design method of the analog front end with the proposed low power techniques will be described. A real chip implementation and its measurement results are explained and finally conclusions will be made.

System Design Consideration

The proposed analog front-end consists of a preamplifier and a Σ-Δ modulator. The preamplifier uses CGC technique for accurate preamplification and Σ-Δ modulator adopts ASNR for wide dynamic range with low power consumption. The architecture of the proposed analog front end is shown in Fig 1. The proposed analog front-end architecture achieves not only the high performance but also the power optimization to the external environment. This analog front-end includes an off-chip DSP for analyzing and modifying parameters. In the conventional preamplifier, an automatic gain control (AGC) and an exponential gain control (EGC) are designed separately because of its design difficulties. In this study, however, CGC integrates AGC and EGC into a single block to reduce power consumption and to expand its dynamic range.

The Fig. 2 shows the relationship between the input of a microphone and the input of the preamplifier. A preceding study reveals that a normal sound level, which is common in human daily life, is from 30 to 90-dB SPL, the Range 1 in Fig. 2 [4]. In this range, the sound amplitude is so small that high performance analog front-end must be used. On the other hand over 90-dB SPL, Region 2~4, high performance analog front-end is not necessary since the sound amplitude is sufficiently large. If we use the high performance analog front-end both in the entire sound regions, the analog front-end produces excessive performance and dissipates power needlessly. In the design of the new Σ-Δ modulator, input sound level is divided into four parts as described in Fig. 2 to control SNR separately at each range to optimize its power and performance.

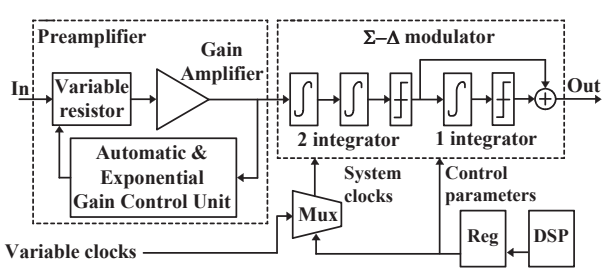


Fig. 1 Proposed analog front-end

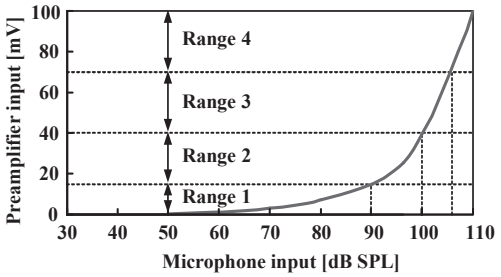


Fig. 2 Characteristics of a microphone for a digital hearing aid

Proposed analog front-end

A. The preamplifier with combined-gain-control technique

The Fig. 3 shows the proposed preamplifier with CGC technique. The V_{TH} is an external control parameter which determines the threshold knee voltage. The gain is given as follows.

$$\text{Gain} = \frac{\text{OUT}}{\text{IN}} = \frac{W_1 L_2 [1 + V_X/(V_{dd} + V_{VC})]}{W_2 L_1 [1 - V_X/(V_{dd} - V_{VC})]}, \quad \begin{matrix} V_1 = V_{VC} - V_X \\ V_2 = V_{VC} + V_X \end{matrix} \qquad (1)$$

where V_1 and V_2 are negative and positive resistance-control-voltage-outputs respectively, generated by the gain control unit (GCU). The V_{VC} is a volume control voltage which determines the common mode level of V_1 and V_2. The V_X, a control voltage decided by the preamplifier output, decides the differential mode level of V_1 and V_2. The W_1, W_2 and L_1, L_2 are the width and the length of the transistor M_1 and M_2, respectively. The V_{dd} is a supply voltage of the analog front-end circuit.

The MOS resistive circuit (MRC), which is composed of four N-type transistors M_1 and M_2, enables to obtain the exponential gain characteristics in accordance with gain amplifier (GA). In addition, the GCU with the peak detector (PD) helps CGC to get the automatic gain characteristics. The PD senses the envelope of the output voltage and controls the GCU.

The gain and the threshold knee point of the preamplifier can be changed by varying V_{VC} and V_{TH}, respectively. When the value of V_{VC} is low, the threshold gain, a gain which the threshold knee point is applied, decreases according to (1) and the power dissipation of the preamplifier is reduced. On the other hand when the value of V_{VC} is high, the threshold gain grows up and the required resolution of the next-stage Σ-Δ modulator is decreased.

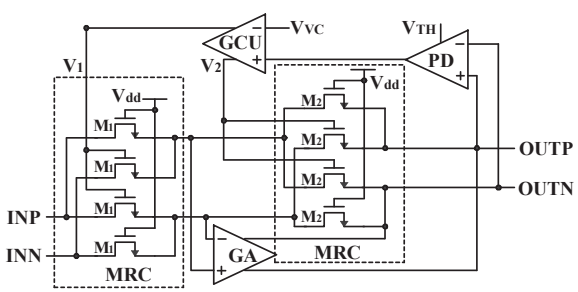


Fig. 3 Proposed preamplifier with CGC technique

B. The Σ-Δ modulator with adaptive SNR technique

To provide wide dynamic range, the Σ-Δ modulator should provide different kinds of SNR values according to the input amplitudes. There have been studies on achieving different SNRs and one method is changing the clock frequency. By changing clock frequency, the Σ-Δ modulator achieves different SNR characteristics. But adopting high clock frequency makes the design of an analog circuit difficult such as operational transconductance amplifier (OTA), since the unity-gain frequency of the OTA should be at least four times higher than the clock frequency of the Σ-Δ modulator [5]. High order Σ-Δ modulator is an alternative approach to modify the SNR. In case of more than 3rd order Σ-Δ modulator, however, its performance seriously suffers from nonidealities due to finite gain and bandwidth of the OTA, and instabilities caused by saturation of the integrator [6]. In this paper, we introduce the ASNR technique to the Σ-Δ modulator to provide stable varying SNRs.

The proposed Σ-Δ modulator is described in Fig. 4. The SW_1 determines the order of the Σ-Δ modulator between 2nd and 3rd while the SW_2 chooses its clock frequency. The combination of these switches allows the Σ-Δ modulator to obtain four different kinds of SNRs. Its control parameters are stored in the control register and a DSP analyzes and modifies them for easy and convenient control. By selecting proper parameters according to the input amplitude, the Σ-Δ modulator obtains optimal SNR from power and performance point of view [7].

Fig. 5 shows the detailed architecture of the Σ-Δ modulator. When the $/SW_1$ is closed, it operates in 2nd order by bypassing the output from the 2nd integrator to the OUTN or OUTP. Because the resistance value of the conventional N-type switch varies according to drain voltage, the 2nd integrator output degrades seriously when it passes through $/SW_1$. A high performance switch, whose resistance value is constant under all range of drain voltage, is necessary to prevent this distortion. However, the high performance switch is difficult to design and consumes additional power. Therefore we adopts the $COMP_1$ which converts the 2nd integrator output into a PWM signal and passes it through the $/SW_1$ without signal distortion. When the $COMP_1$ is activated, the 3rd integrator and $COMP_2$ are totally turned off to eliminate extra power consumption. On the other hand, if the $/SW_1$ is opened, the 3rd integrator accepts the output of the 2nd integrator as an input and performs a 3rd-order modulation. In this case, the $COMP_1$ is turned off to avoid extra power dissipation. By turning the SW_2 on and off, clock frequency is changed between 2.048-MHz and 1.024-MHz, respectively.

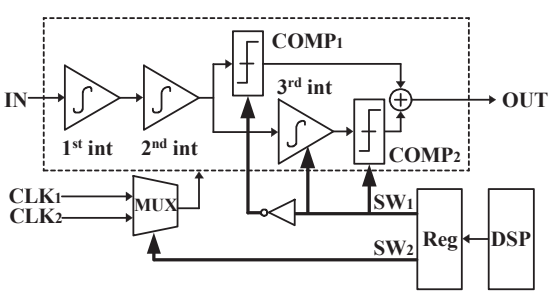
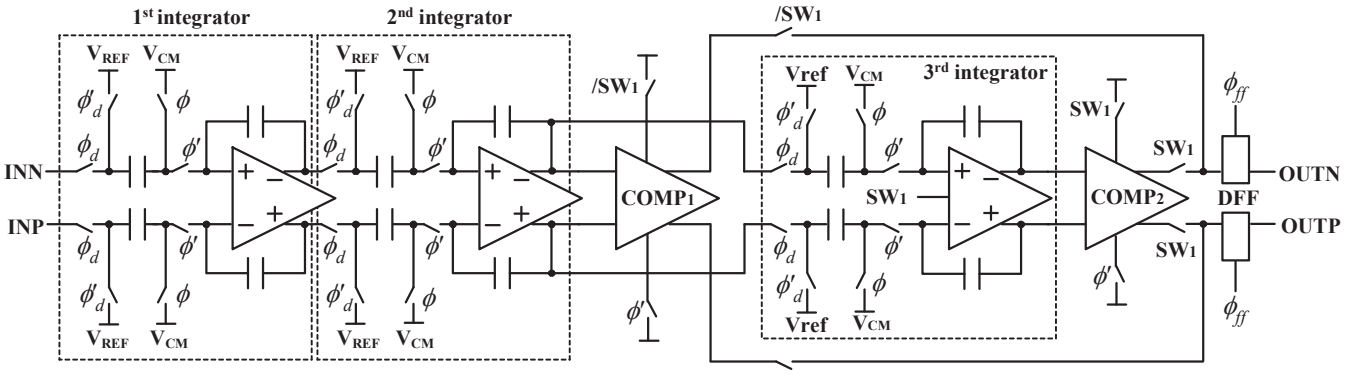


Fig. 4 Proposed Σ-Δ modulator exploiting adaptive SNR technique



	Type1	Type2	Type3	Type4
SW_1	off	off	on	on
SW_2	off	on	off	on

Fig. 5 Detailed Σ-Δ modulator architecture

By changing SW_1 and SW_2 separately, four configurations of Σ-Δ modulator, which have different kinds of SNRs, are obtained as summarized in a box of Fig. 5. With SW_1 opens, type 1 and type 2 of the 2nd order Σ-Δ modulator are achieved by turning the SW_2 off and on, respectively. With the closed SW_1, type 3 and type 4 of the 3rd order Σ-Δ modulators are given by turning the SW_2 off and on, respectively.

The low power OTA is designed to have a compensated two-stage, which has an input stage with cross-coupled active load and a class AB output stage [8]. It shows 77.6-dB DC gain, 7.07-MHz unity gain bandwidth, and 55° phase margin for a 3-pF load. The 1-bit quantizers such as $COMP_1$ and $COMP_2$ with a clocked circuit minimize the hysteresis to offer good reset [9].

The Fig.6 shows MATLAB simulation results of the proposed Σ-Δ modulator. Different kinds of SNR values can be generated according to the input amplitude.

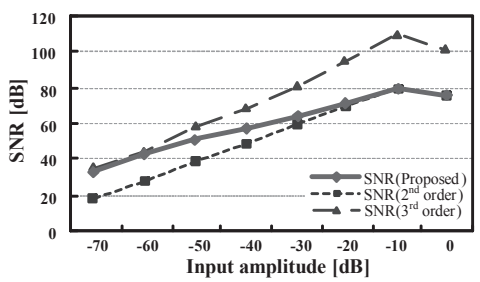


Fig. 6 Simulation results of the conventional vs. proposed Σ-Δ modulator

Experimental Results

The chip microphotograph of the proposed analog front-end circuit is shown in Fig. 7. It was fabricated in a 0.25-μm CMOS technology and its core size is 0.5-mm^2.

In Fig. 8, variations of the measured threshold gains and the threshold knee points of the preamplifier are presented as a function of the V_{VC} with the V_{TH} as a parameter. The threshold knee point is determined by different values of the V_{TH}. By reducing V_{TH}, knee point is decreased simultaneously. Moreover, the threshold gain of the preamplifier is determinded according to the values of the V_{VC} and V_{TH}. By using these parameters, an excessively high gain is prevented and the power dissipation is reduced. Measured attack and release response is shown in Fig. 9. The output signal is shown when the input voltage level suddenly drops by 25-dB. After a 0.1 sec delay, its output gain increases gradually according to the input level.

The Fig. 10 shows the plots of the measured SNR and SNDR versus the input amplitude. A measured output voltage spectrum is presented in Fig. 11. The proposed Σ-Δ modulator is type 1 with 2-KHz sinusoidal input signal and 1.024-MHz clock frequency. The measured peak SNR is 72-dB.

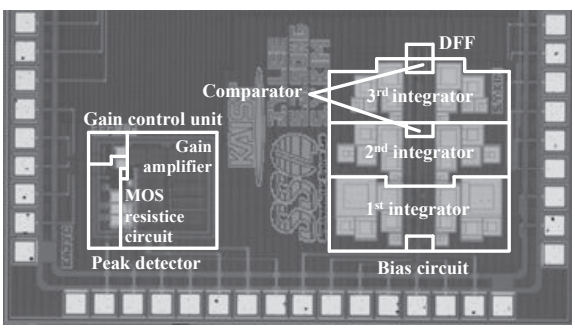


Fig. 7 Microphotograph of the proposed analog front-end

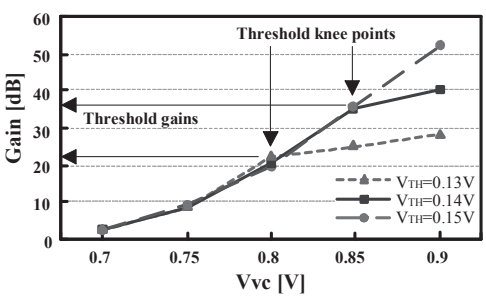


Fig. 8 Measured gain as a function of V_{VC} with V_{TH} as a parameter of the proposed preamplifier

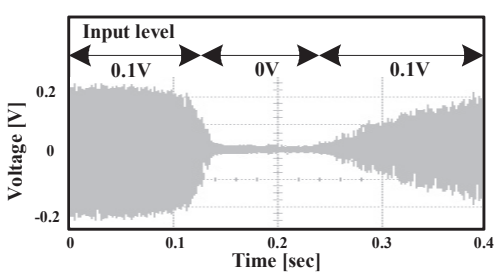


Fig. 9 Measured attack and release response

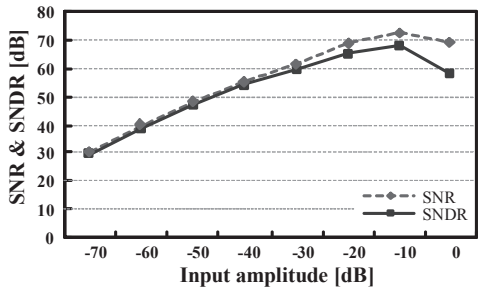


Fig. 10 Measured SNR/SNDR vs. input amplitude

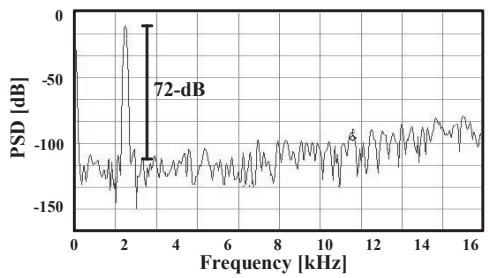


Fig. 11 Measured spectrum of the proposed Σ-Δ modulator

The measured performance of the proposed analog front-end is summarized in TABLE I. When the input amplitude is higher than 105-dB SPL, the Σ-Δ modulator acts as the type 1 and reduces power dissipation effectively. But if the input amplitude is lower than 90-dB SPL, it operates as the type 4 and offers high SNR. It allows an efficient usage of the limited energy of a zinc-air battery usually adopted in digital hearing aid [10]. The typical input referred noise of the complete analog front-end circuit is 3.8-μVrms.

The 2nd and 3rd order Σ-Δ modulator enhances the SNR by 9-dB and an 8-dB, respectively with the shift of clock frequency from 1.024-MHz to 2.048-MHz. The extra power dissipation due to frequency change is less than 1-μW in each type of the modulator.

TABLE I
THE PERFORMANCE SUMMARY

Supply voltage	0.9-V			
Order	2nd order		3rd order	
	Type1	Type2	Type3	Type4
Clock frequency (kHz)	1.024	2.048	1.024	2.048
Peak SNR	72-dB	81-dB	78-dB	86-dB
Power dissipation (Σ-Δ modulator)	26.4-μW	26.8-μW	35.7-μW	36.7-μW
-3dB bandwidth	8-kHz			
Input referred noise	3.8-μVrms			
Power dissipation (Preamplifier)	V_{VC}=0.75	V_{VC} =0.8	V_{VC}=0.85	
	33-μW	35-μW	38-μW	
Total power dissipation (Analog front-end)	59.4-μW ~ 74.7-μW (According to the parameter value)			
Die size	0.5-mm^2			
Technology	0.25-μm CMOS technology			

The TABLE II compares the performance of the proposed analog front-end circuit with those of the previous works. The proposed analog front-end circuit dissipates the lowest power at the 0.9-V power supply voltage.

TABLE II
THE PERFORMANCE COMPARISON OF THE ANALOG FRONT-END CIRCUIT

	JSSC 1997 [2]	JSSC 2002 [3]	This work
Supply Voltage	2.15-V	1.1-V	0.9-V
Peak SNR	77-dB	92-dB	86-dB
Power consumption	323-μW	190-μW	59.4-μW
CMOS Technology	0.8-μm	0.6-μm	0.25-μm

Conclusion

A novel low-power, energy-efficient analog front-end is proposed and implemented in a 0.25-μm CMOS process for a digital hearing aid chip. To reduce power dissipation and expand its dynamic range, the CGC and the ASNR technique are devised and adopted. The peak SNR is 86-dB and the input referred noise is 3.8-μVrms. The proposed analog front-end consumes a minimum power of 59.4-μW at 0.9V supply.

Acknowledgements

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