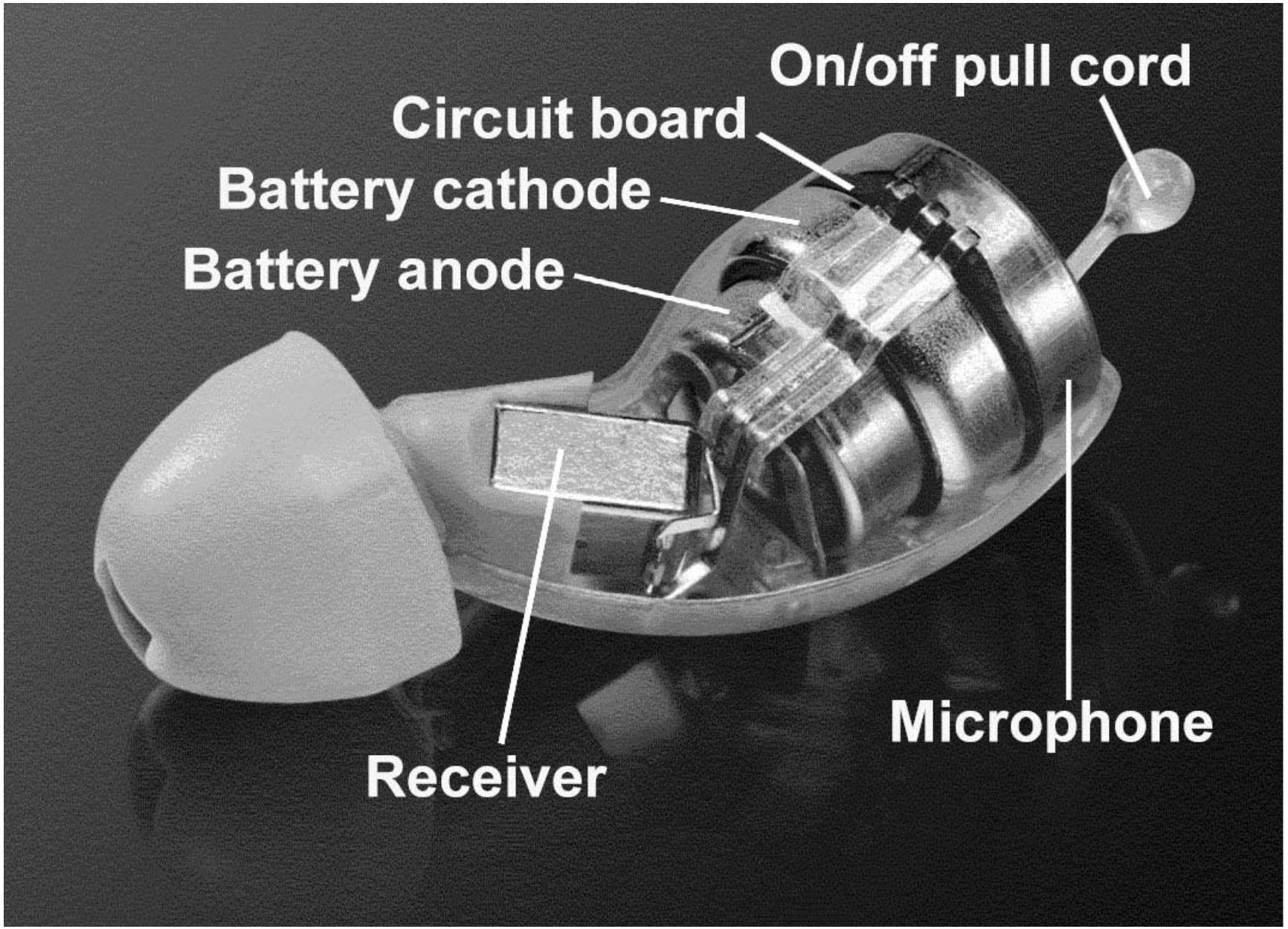
OUTLINE

- Performance specifications
- Analog block design for low power
- Measured performance
- Summary

CUTAWAY VIEW OF HEARING AID SYSTEM

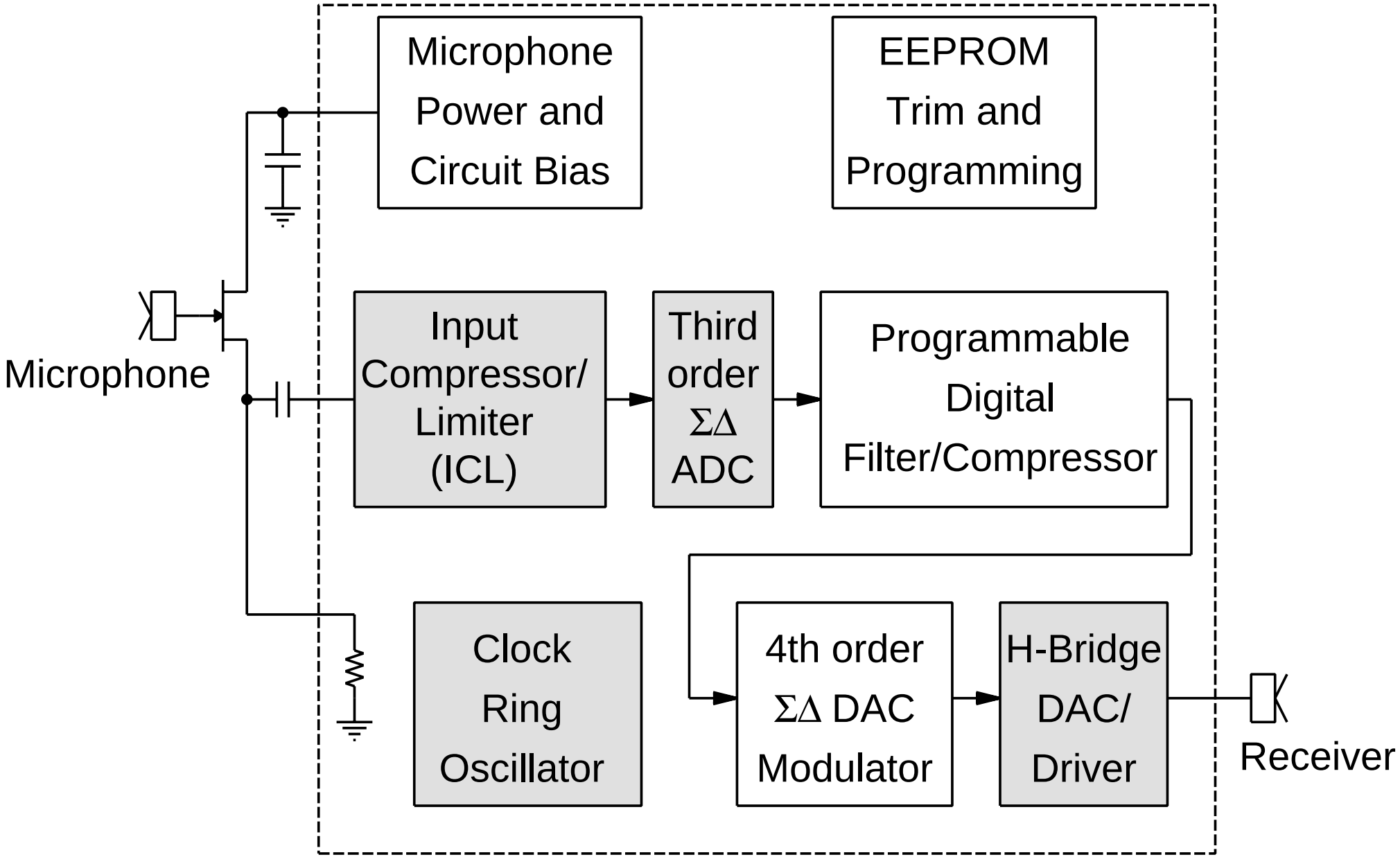


CHIP PERFORMANCE SPECIFICATIONS

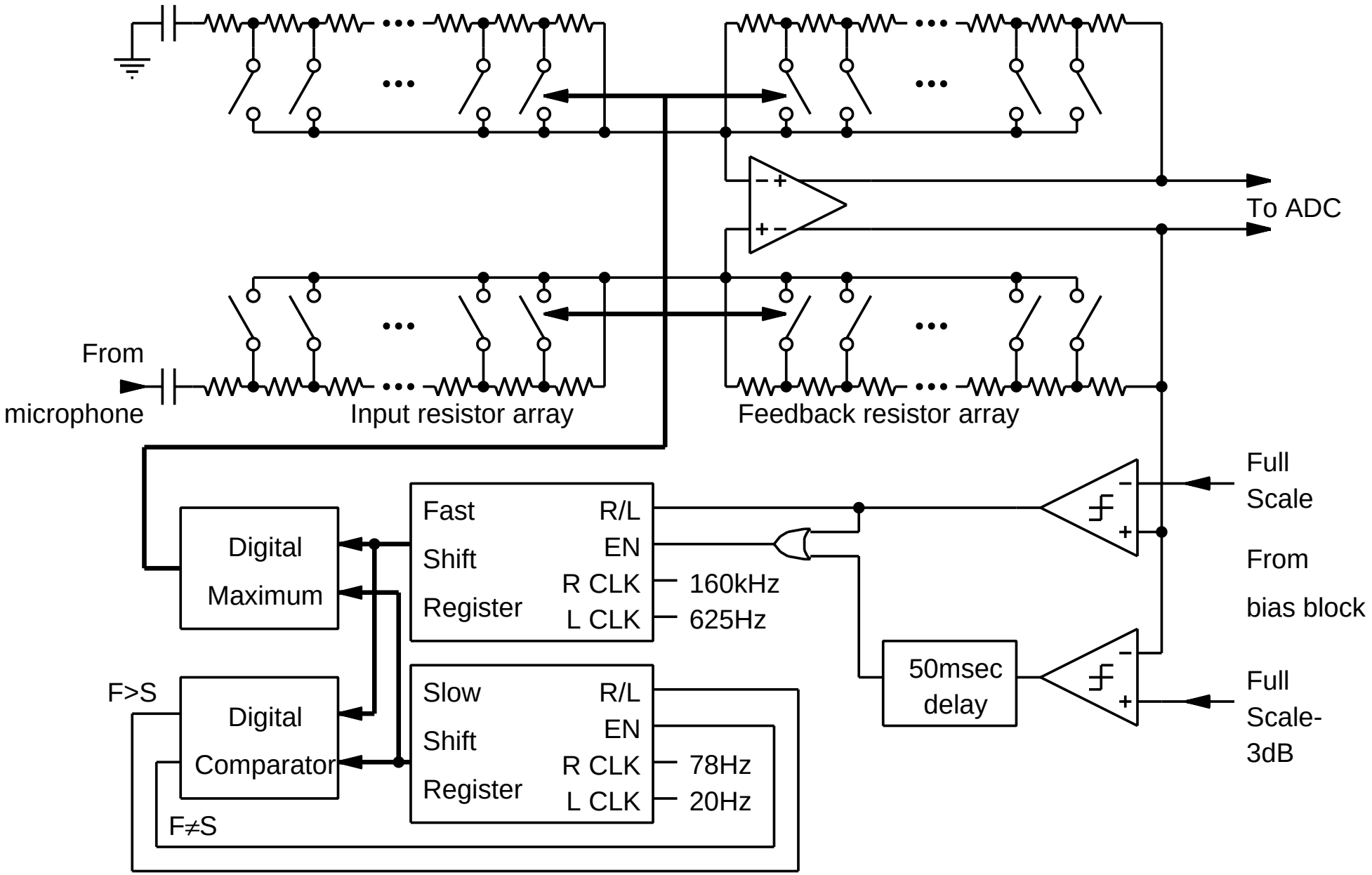
Battery voltage range	1.1V - 1.5V
-3dB bandwidth	100Hz-10kHz
Input referred noise (100Hz-10kHz)	<3.5μV_{rms}
Input compression threshold	85dBSPL =7.942mV_{peak}
Total harmonic distortion	
Below input compression	<0.1%
Above input compression	<1%
Total battery current	<300μA*

* Typical existing low noise, digitally filtered hearing aid chips for replaceable batteries draw 800μA - 1.5mA supply current

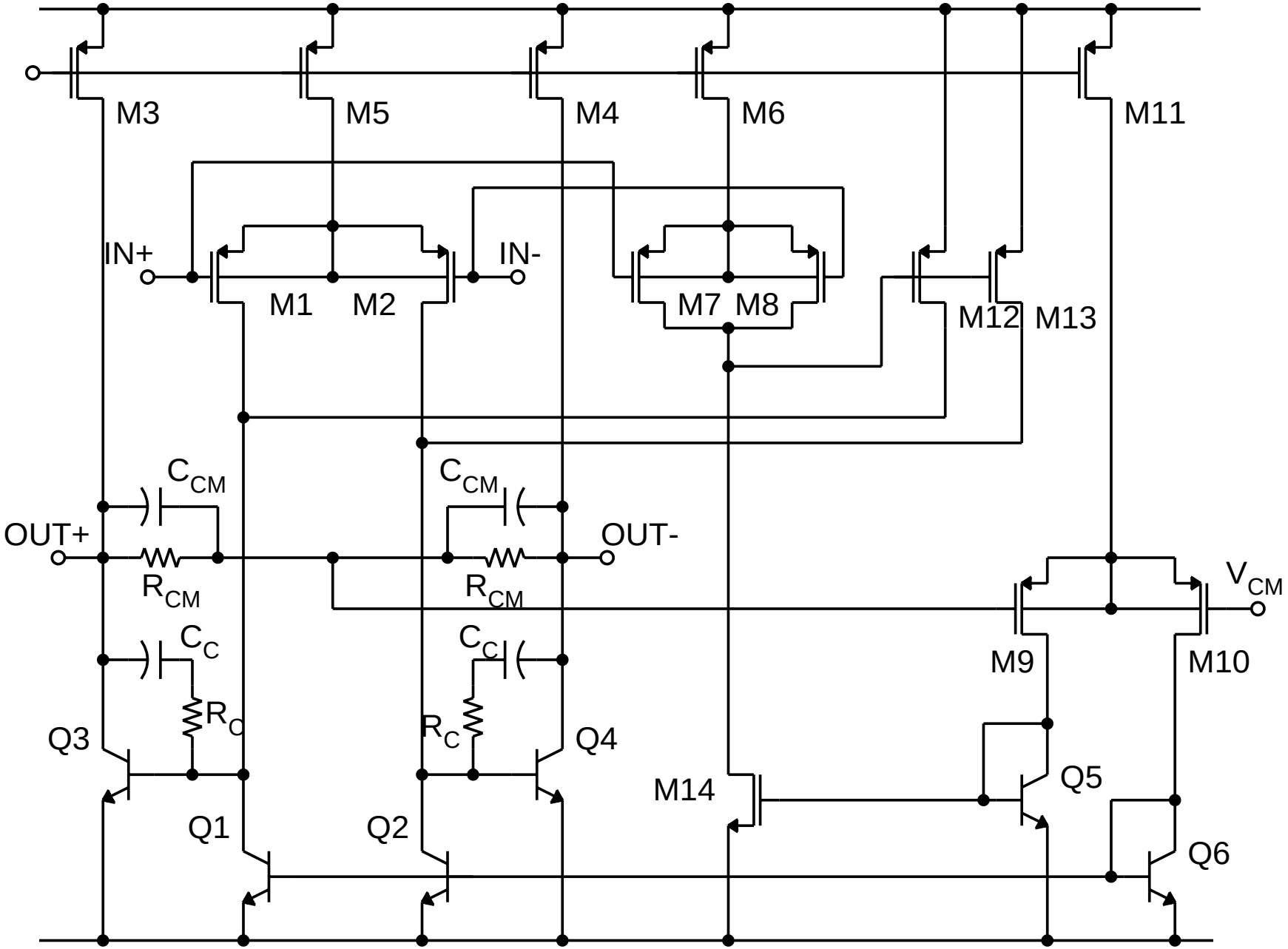
CHIP BLOCK DIAGRAM



INPUT COMPRESSOR/LIMITER (ICL) ARCHITECTURE

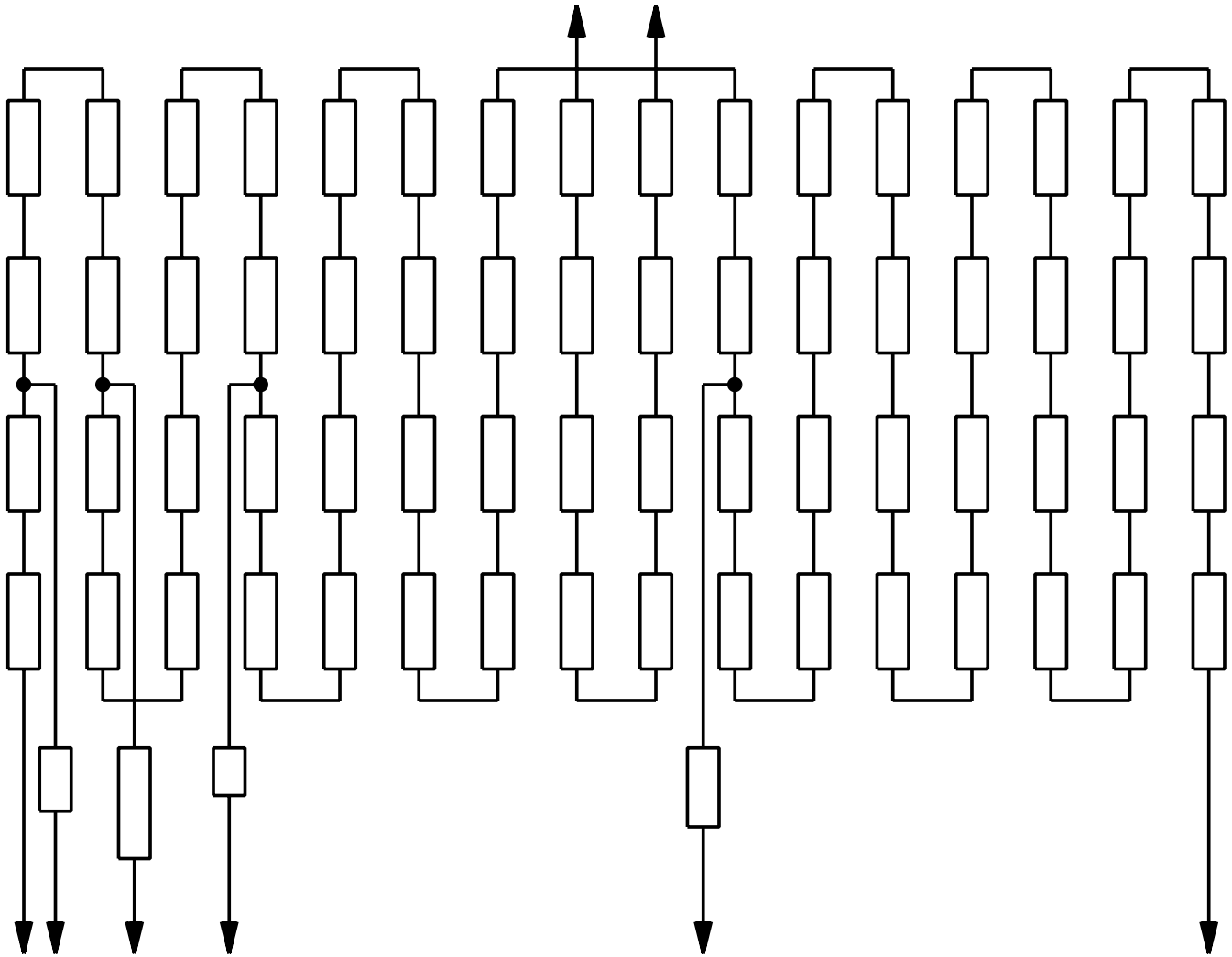


ICL OPAMP SCHEMATIC



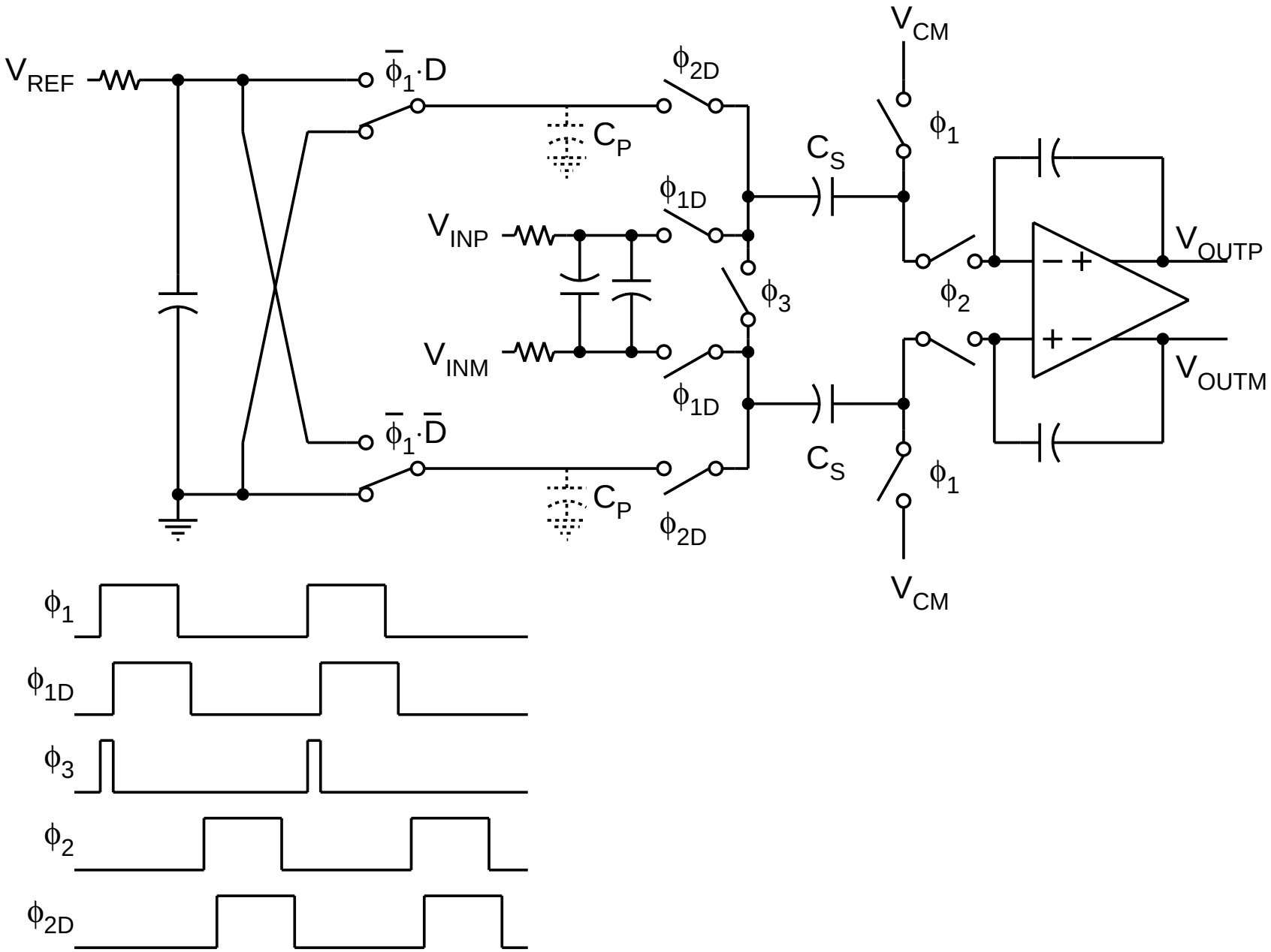
ICL RESISTOR ARRAY LAYOUT

Low-level input resistance

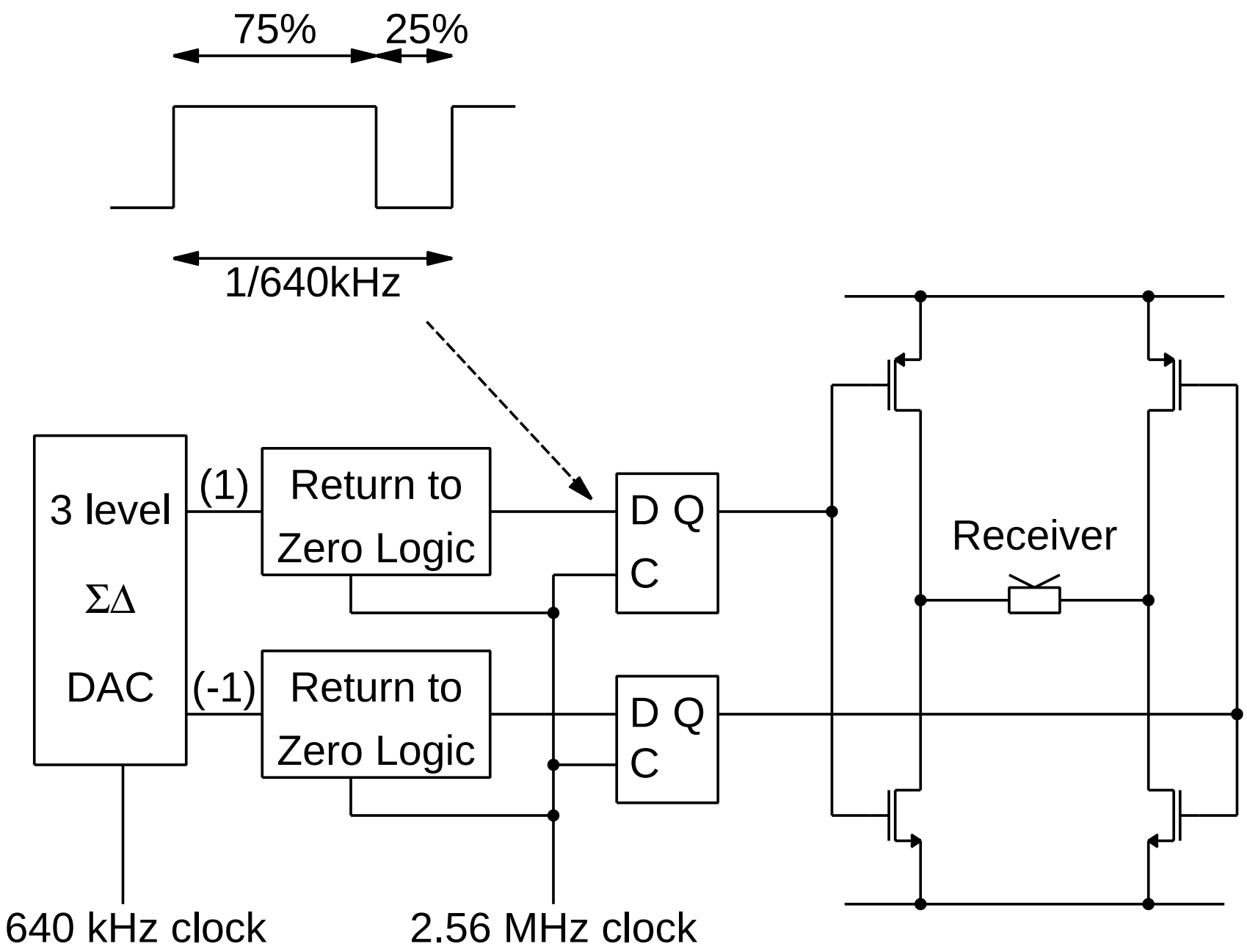


To feedback resistance MOS switch array

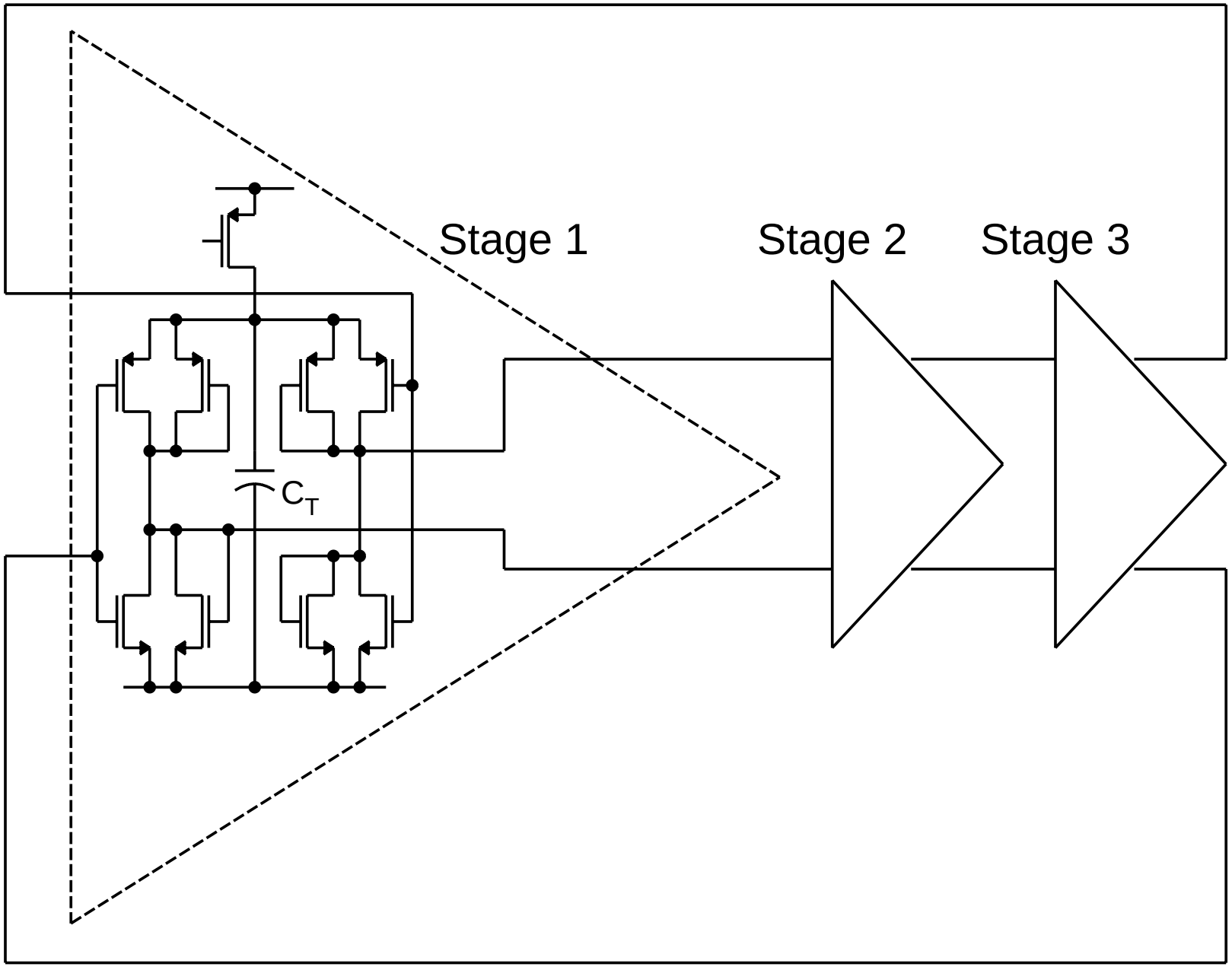
FIRST ΣΔ ADC INTEGRATOR



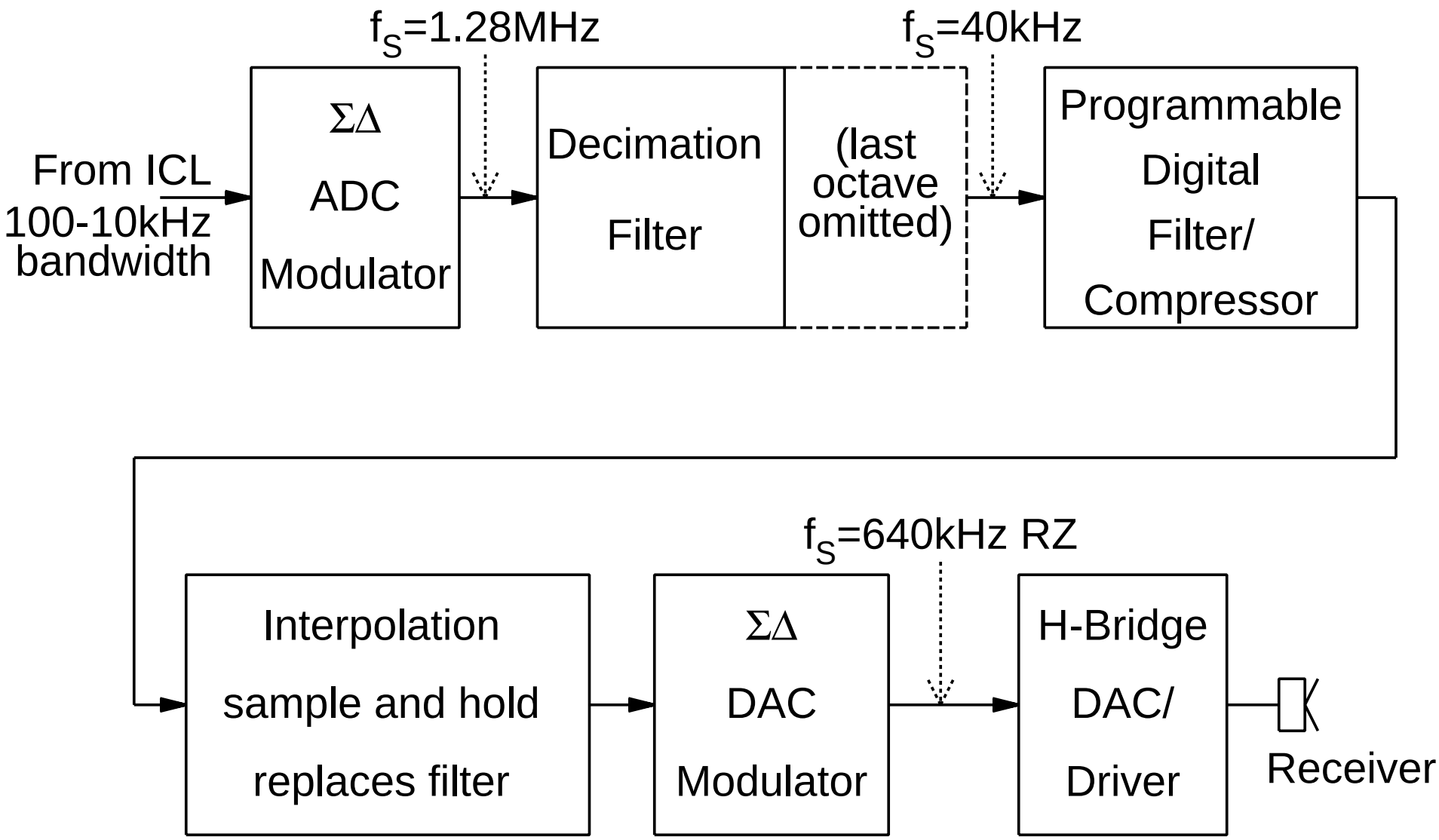
ΣΔ DAC AND H-BRIDGE TIMING



CLOCK OSCILLATOR SCHEMATIC

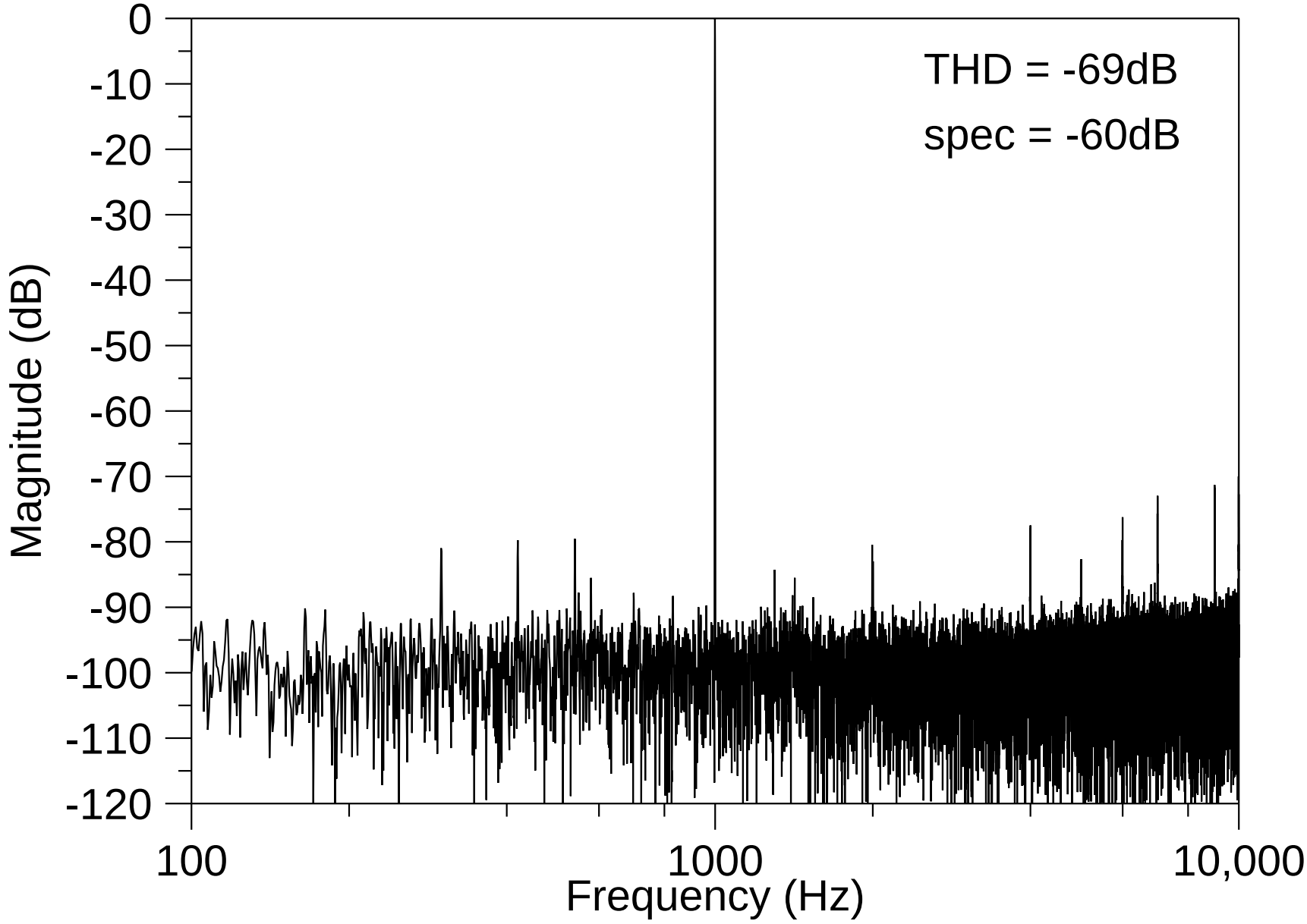


SAMPLING RATES FOR LOW POWER



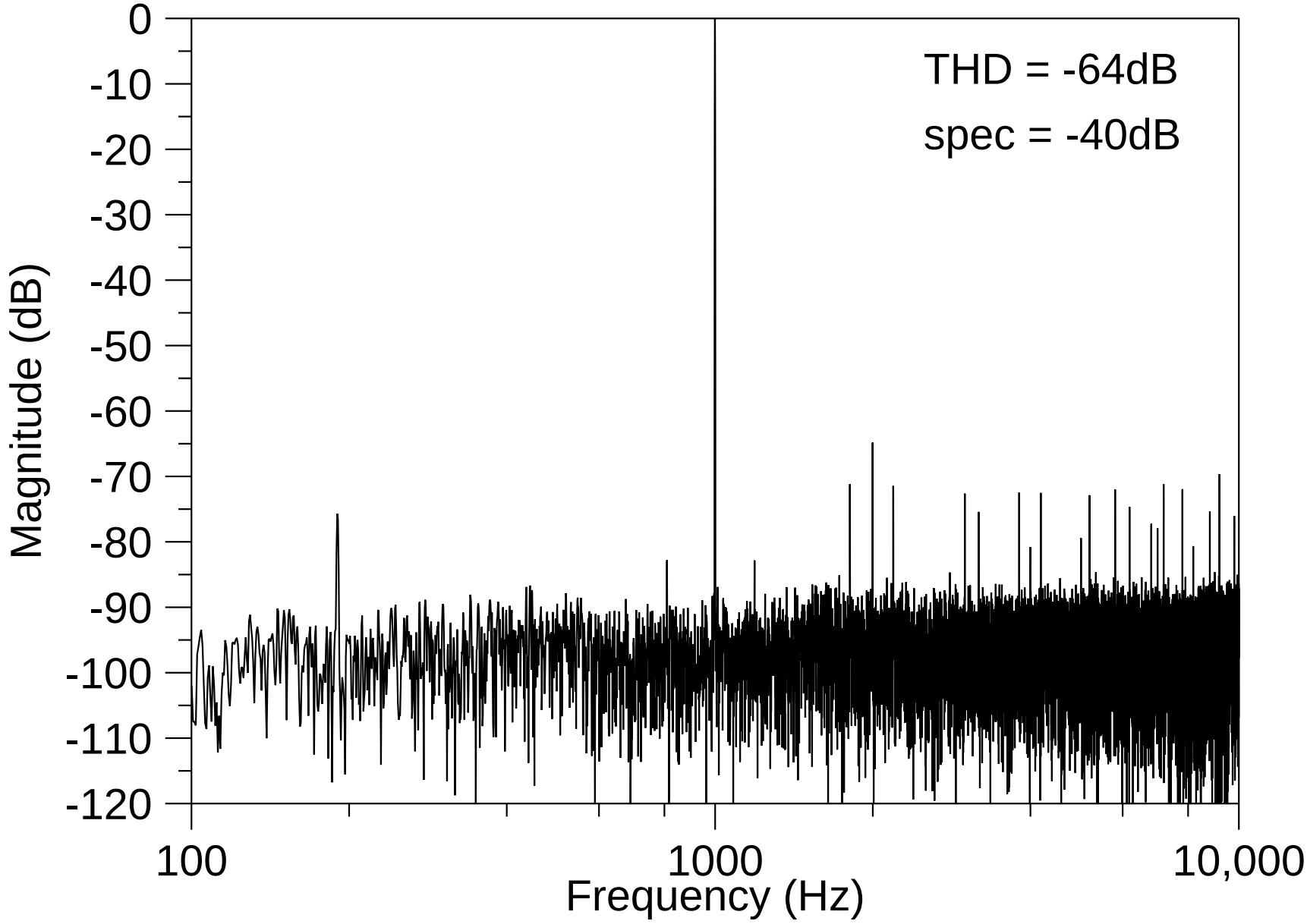
MEASURED FFT RESPONSE

Low level input: v_{IN} = 4mV peak f_{IN} = 1kHz



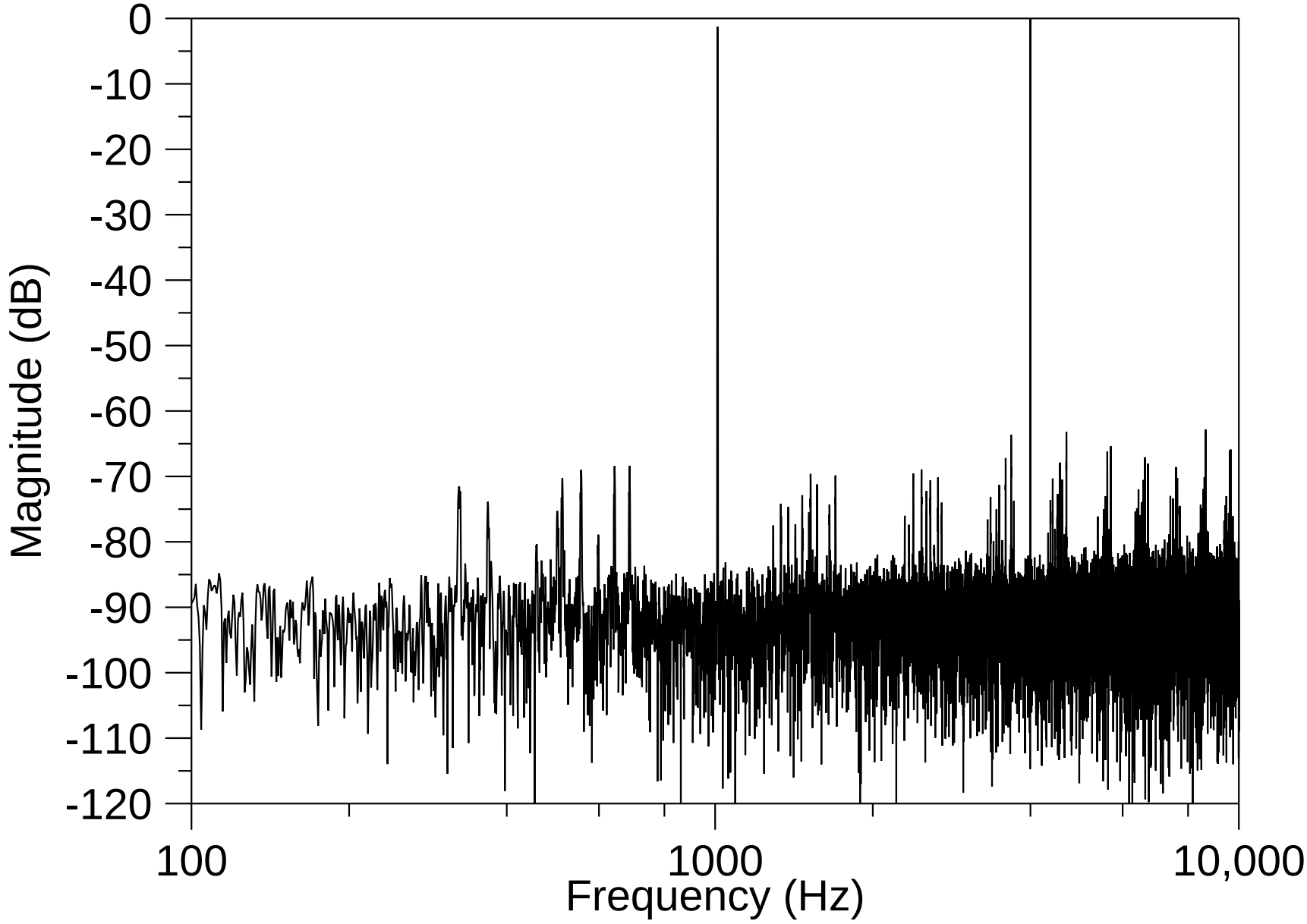
MEASURED FFT RESPONSE

High level input: v_{IN} = 80mV peak f_{IN} = 1kHz



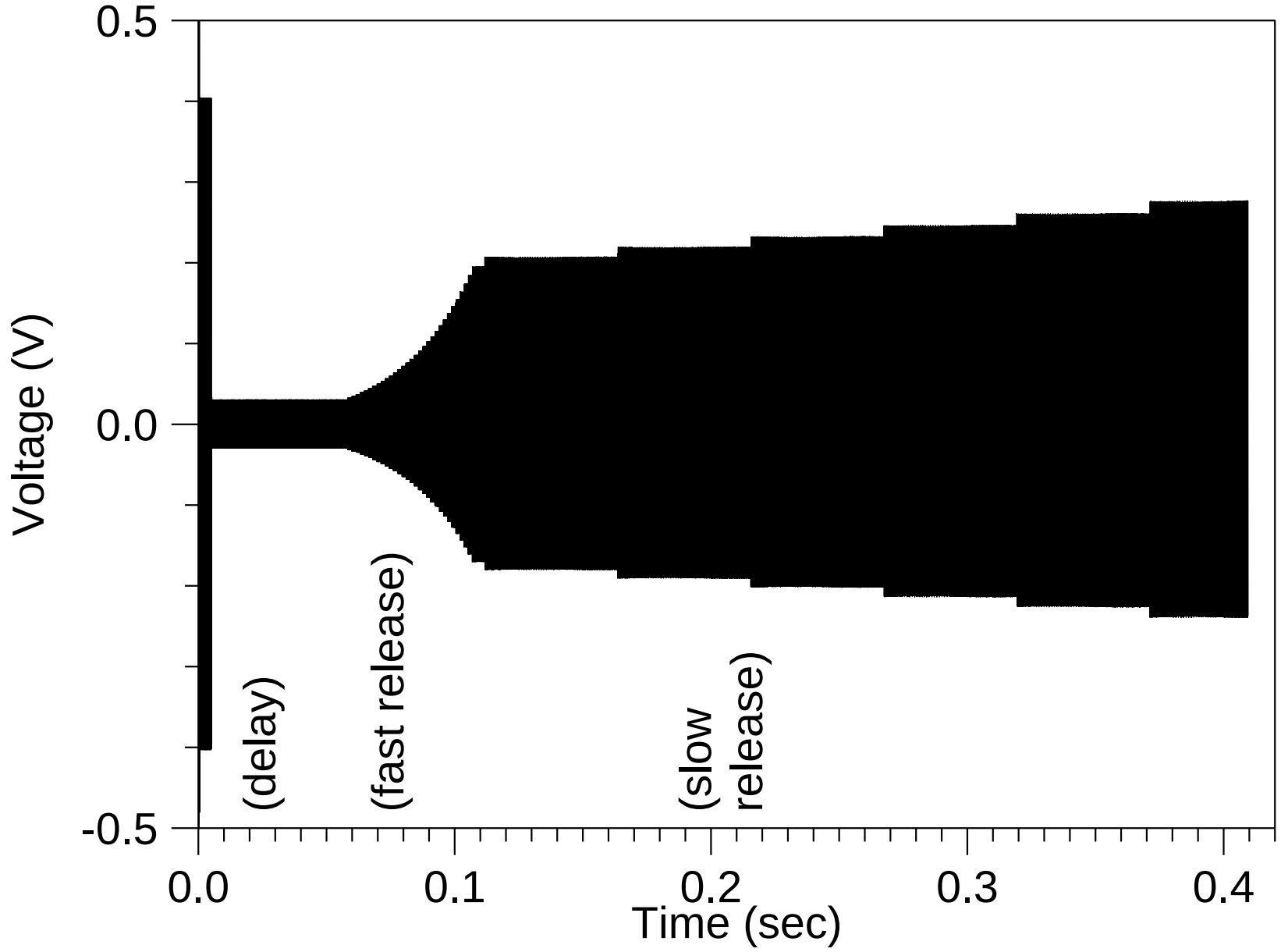
MEASURED FFT RESPONSE

Two tone input: v_{IN} = 4mV peak f_{IN} = 1kHz, 4kHz



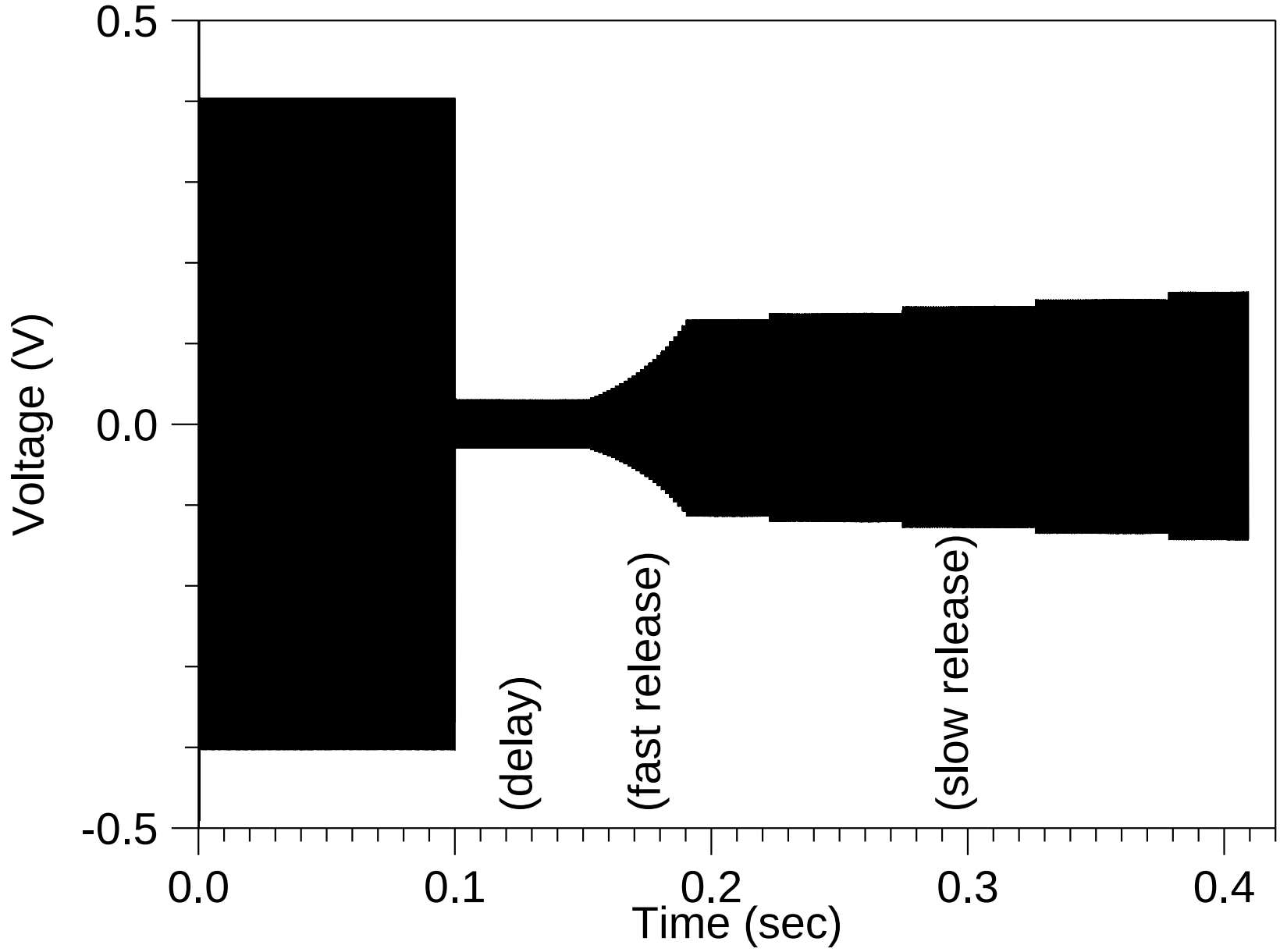
MEASURED ATTACK AND RELEASE RESPONSE

Short compression transient



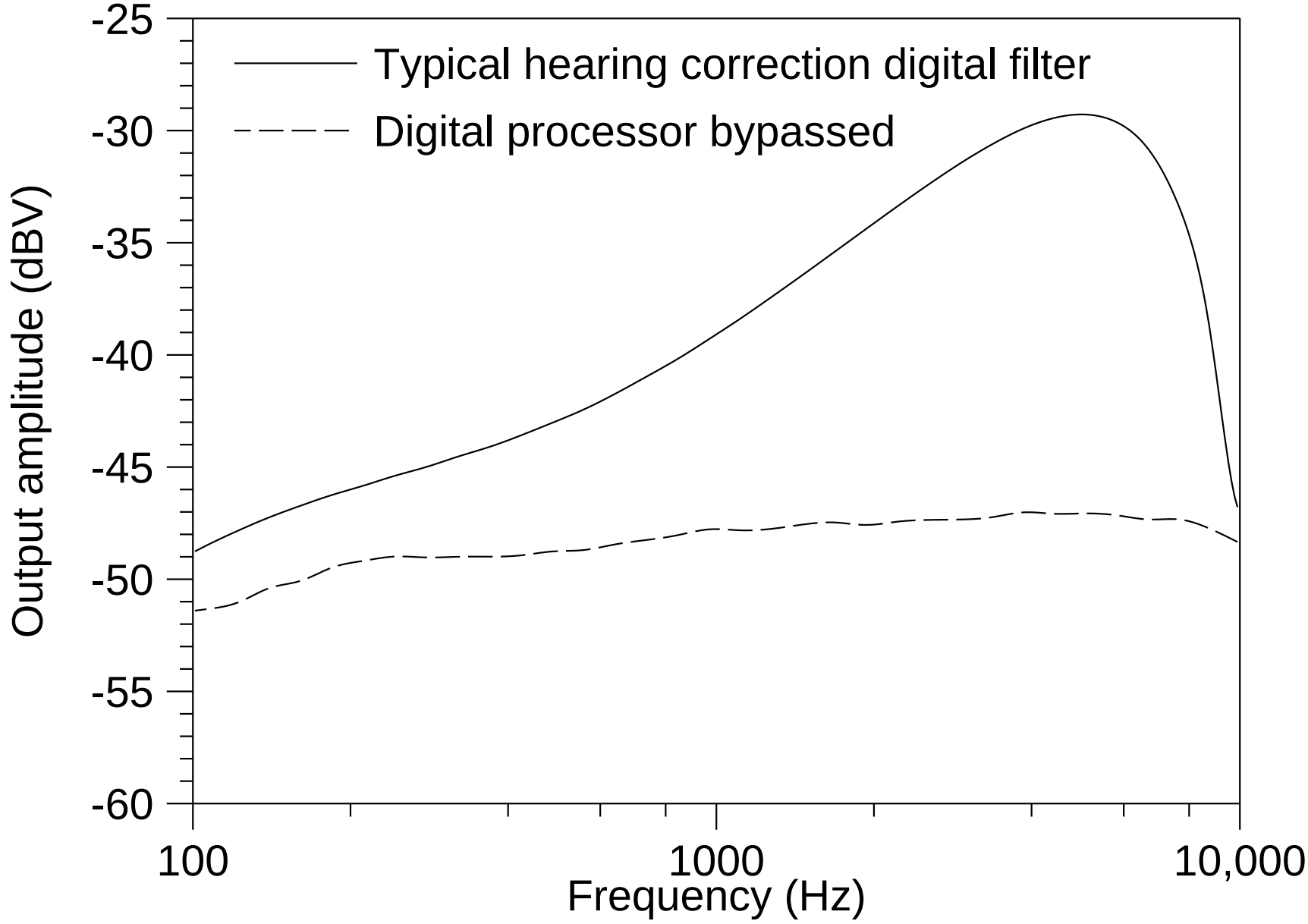
MEASURED ATTACK AND RELEASE RESPONSE

Long compression transient

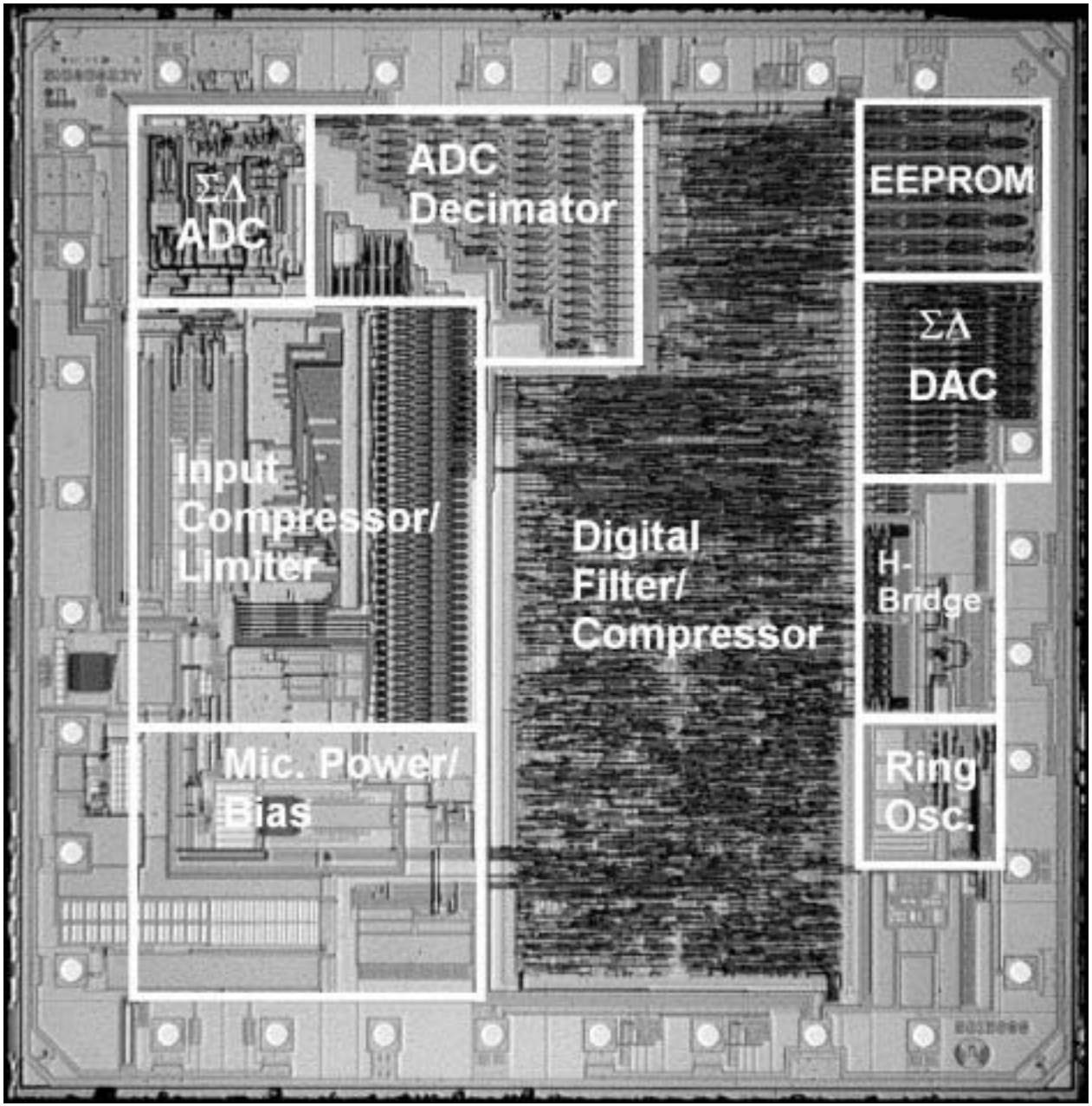


MEASURED FREQUENCY RESPONSES

Low level input: v_{IN} = 4mV



DIE MICROGRAPH



PERFORMANCE SUMMARY

Battery voltage range		1.1-1.5V
Battery current consumption (no signal)		
1.1V supply		
Analog	173μA	
Digital	48μA	
H-Bridge	15μA	
Ring oscillator	34μA	
Total		270μA
1.3V supply		299μA
1.5V supply		323μA

PERFORMANCE SUMMARY (continued)

-3dB bandwidth	100Hz-10kHz
Input referred noise (100Hz-10kHz)	$2.8\mu V_{rms}$
Maximum input signal	$450mV_{peak}$
Total harmonic distortion	
$v_{IN}=7mV_{peak}$	0.02%
$v_{IN}=80mV_{peak}$	0.5%
Input compressor maximum gain step error	0.09dB
Clock jitter	147ps rms
Sub-bandgap reference stability	1%
Temperature range	20-40°C
Die size in 0.6μm, 3.3V CMOS	$12mm^2$