A 1.1-V 270-μA Mixed-Signal Hearing Aid Chip

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***Abstract*—This paper presents a single-chip mixed-signal IC for a hearing aid system. The IC consumes 270 μA of supply current at a 1.1-V battery voltage. The presented circuit and architectural design techniques reduce the total IC power to 297 μW, a level where up to 70 days of lifetime is achieved at 10 h/day for a small zinc–air battery. The measured input referred noise for the entire channel is 2.8 μVrms and the average THD in the nominal operating region is 0.02%. The jitter for the on-board ring oscillator is 147 ps rms. The chip area is 12 mm^2 in a 0.6-μm 3.3-V mixed-signal CMOS process.**

***Index Terms*—Analog-to-digital conversion, digital filters, digital signal processing, digital-to-analog conversion, gain compression, hearing aid circuits, limiting, low power, low voltage, ring oscillator.**

I. Introduction

FIG. 1 SHOWS the signal path of the IC. All signal processing elements, with the exception of the microphone, receiver (earphone), and coupling and bypass capacitors are contained within the single mixed-signal IC. A preamplifier that includes gain compression limiting amplifies the output of the microphone. The limiter function prevents loud sounds from overloading the analog-to-digital converter (ADC), preventing distortion. A sigma–delta ADC outputs a bitstream at a rate of 1.28 MHz. This bit stream passes through a decimation filter and is down-sampled to a rate of 40 kHz. The digital signal processor operates on the 40-kHz rate data to perform the hearing aid signal-processing algorithm. The output of the digital signal processor drives a sigma–delta digital-to-analog converter (DAC) modulator where the signal is converted to a 2-b stream at a rate of 640 kHz. The output of the sigma–delta modulator goes through an H-bridge driver, which then drives the receiver, which converts the 2-b stream into an analog, acoustical signal. The digital signal processor needed to be optimized for low power and small size, yet had to provide a certain amount of flexibility. A general-purpose DSP core would provide the flexibility at the expense of power and size. A dedicated, hardwired digital signal processing circuit would consume minimal power and would be small, but would lack flexibility. The final design selection was a hardwired digital signal processing circuit with programmable parameters that adjust and configure the hearing aid signal-processing functions. The approach provides the needed flexibility without the penalties of a general-purpose DSP core.

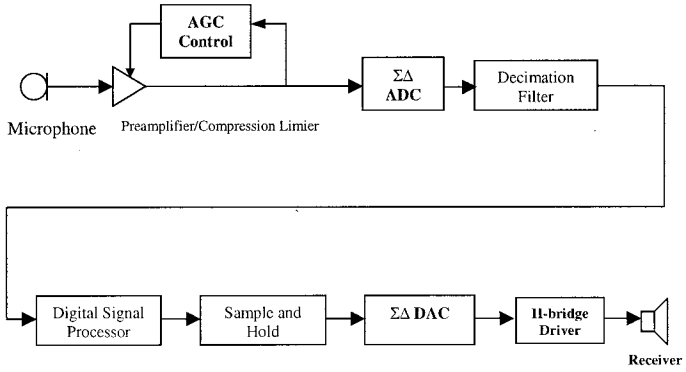

Fig. 1. Signal path block diagram.

The chip operates with a single-cell voltage supply, as low as 1.1 V. The 0.6-μm 3.3-V CMOS IC process used includes a deep n-well layer essential for junction isolation of digital and analog sections. This layer also affords a vertical npn bipolar device in the input stage opamp to reduce $1/f$ noise, as well as in the bandgap reference. Also available are a low-threshold voltage option for the MOS devices and EEPROM cells for prescription selection and analog trim functions. Both the input compression limiter (ICL) and the ADC use a locally boosted supply voltage to drive the nMOS analog switch gates. This work achieves 28 dB lower distortion while using one fifth the current consumption of previous low-power work [1], aided by process enhancements and new design techniques.

II. ICL

A diagram of the ICL is shown in Fig. 2. After conversion from the single-ended microphone input by this stage, fully differential circuitry is employed throughout the analog blocks. A closed-loop architecture satisfies 0.03% input-stage harmonic distortion requirement and keeps static power consumption constant over all gain settings. Resistor taps and nMOS switches are provided for 83 gain steps of 0.5 dB, from -1 to 40 dB. Input signals experience gain compression and release governed by four time constants. Relatively fast gain reduction and recovery occurs for brief and exceptionally high sound levels, whereas

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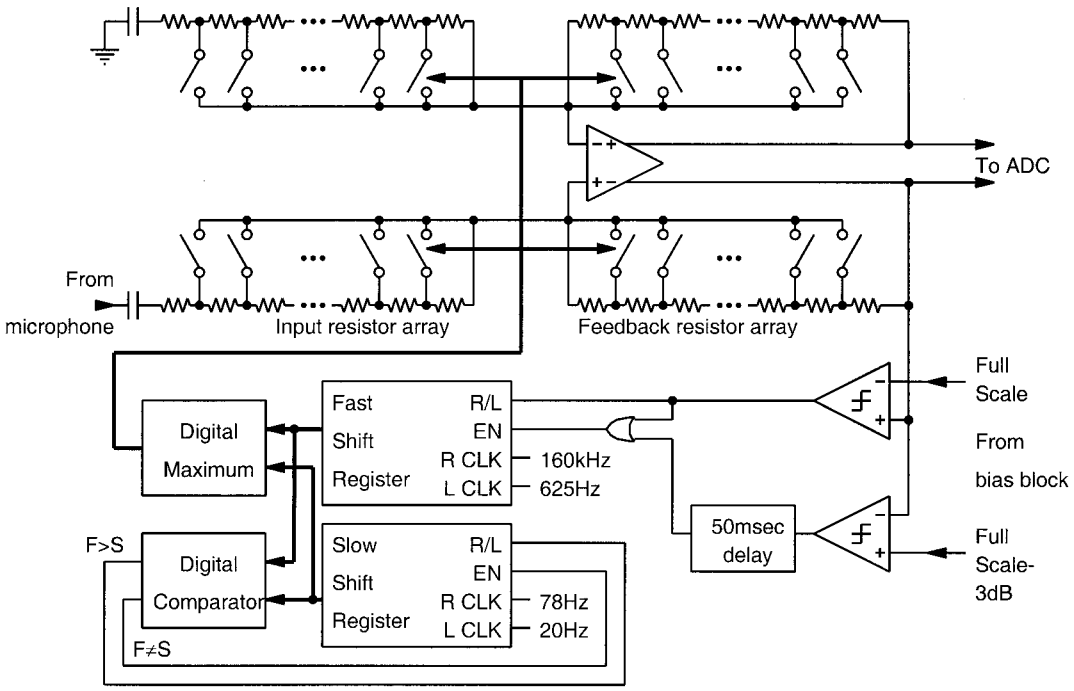

Fig. 2. ICL.

compression and release from sustained sound levels occur at significantly slower rates. A 3-dB hysteresis window inhibits changes in the gain setting for steady-state sound levels, preserving linearity. Even though the incremental resistance for each 0.5-dB gain step is nonuniform, almost all of the resistance required for each tap is realized with a varying number of unit resistors from an array of matched cells.

The bidirectional shift registers in Fig. 2 drive the resistor array switches without intervening decoder. These registers may change the state of only one switch per clock cycle, giving glitch-free gain steps. The Compare and Maximize functions are computed with a chain of simple bitwise gates. Closed-loop gain is reduced as "one" bits are shifted to the right in response to sound levels greater than full scale, and is increased as "zero" bits are shifted to the left during release. The first 57 steps of gain reduction are realized by taps on the feedback resistance, and the final 26 steps, for high sound levels, adjust the input resistance. This arrangement saves considerable bias current in the opamp output stage, since minimum load resistance is kept high, but still gives minimum noise with lower input resistances at high gain settings. The differential input resistors for high gain settings are 10 KΩ each, and the total feedback resistance available is 1 MΩ. Since the bandwidths are limited and the resistance values fairly high, the NMOS switches in the resistor arrays can be made large enough so that their channel resistance does not cause a gain error $>$0.1 dB. Small stub resistors outside the array are then used on each tap to make up the difference between the nearest integer number of unit resistors and the nonuniform resistance required. With this layout, accurate logarithmic gain steps and accurate total gain are achieved. For further layout details, see [2].

Fig. 3 shows the ICL opamp schematic. The active part of the opamp is a fairly standard two-stage design. M1 and M2 are the diff pair for the first stage, and Q1 and Q2 are their active loads. The choice of bipolar devices for the active loads reduces $1/f$ noise. Then Q3 and Q4 are the amplifying devices for the second stage, with M3 and M4 their class-A active loads. C_c and R_c give pole-splitting compensation. $R_{\rm cm}$ and $C_{\rm cm}$ generate a common-mode output voltage level that is compared to the desired common-mode level $V_{\rm cm}$ by the diff pair of M9 and M10. Q6 and Q1–Q2 form a current mirror that completes the common-mode feedback loop. Q5 is in the circuit only to keep the V_{ds} of M9 matching the V_{ds} of M10 and minimize the offset in the M9 and M10 amplifiers. The base voltage of Q5 is fed to the gate of M14 because it was a convenient source of a bias voltage that is several hundred millivolts above the negative supply rail. There is no real signal being transmitted from Q5 to M14. M14 is a very long and thin device that is designed to just give a very small current (a fraction of a microamp) to M7 and M8. The actual drain current of M14 is not critical, and the gate voltage of M14 is not critical. Just enough current from M14 to sense when M5 is somewhere near the triode region is needed. When the opamp input common-mode voltage at the gates of M1, M2, M7, and M8 is in its proper operating range, slightly above mid-supply, then the drain current of M6 would be sufficient to pull the gates of M12 and M13 almost to the positive rail and M12 and M13 are off. However, when the input common-mode voltage is too high, and M5 is going into triode, then the V_{ds} across M6 is also very small. Then, whatever small drain current there is in M14 can pull the gate voltage of M12 and M13 low, turning them on. M12 and M13 then dumps some temporary bias current into the first stage, to substitute for the bias current into Q1 and Q2 that is no longer coming from M5 since it is in triode. This keeps the common-mode feedback loop active. Since there is overall resistive feedback around the opamp when the output common mode level is set by the feed-

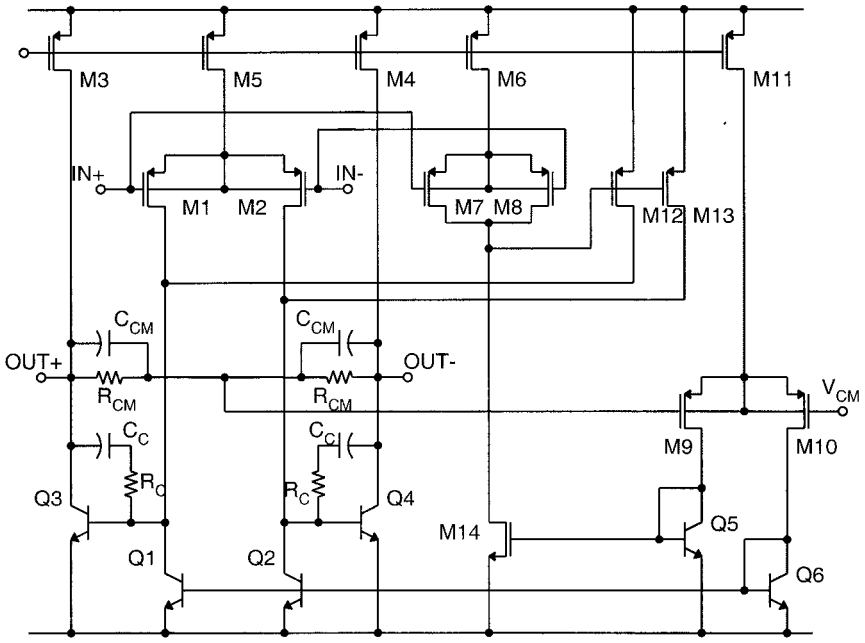

Fig. 3. ICL opamp schematic.

back loop, the input common mode is also quickly restored to its proper range and M12 and M13 are again turned off, leaving the opamp in its normal operating state. Without this circuitry, it is possible that the common-mode loop can settle in a stable operating point that drives both the output terminals to the positive rail caused by either an initial startup condition or a transient condition. M7, M8, and M6 are scaled down from M1, M2, and M3, to save power. M5 is 20 gate fingers, and M6 is a factor of 10 smaller. M1 and M2 have to be huge to reduce the opamp $1/f$ noise to a very low level for the hearing aid, and they are 48 fingers, each 52 μm wide by 8 μm long. M7 and M8 are two fingers of 4 μm by 2 μm. Therefore, M7 and M8 are not exact scaled down replicas of M1 and M2, but for the operation of this circuit exact ratios are not necessary.

III. Sigma–Delta ADC Modulator

The third-order $\Sigma\Delta$ ADC modulator consists of a cascade of two single-bit stages, a second-order stage followed by a first-order stage [3]. The input sampling network for the first integrator is shown in Fig. 4. The use of a single pair of differential sampling capacitors C_S reduces the total input capacitance for a given kT/C noise budget and allows reduction of opamp power. An additional short clock phase ϕ_3 discharges these capacitors before each sample and erases the charge condition from the previous full-scale reference sample. This reduces the dynamic signal input charge required, eliminating an active buffer in preference to a simple passive RC anti-alias filter as shown. Furthermore, the switches that sample the reference voltage with a polarity that conveys the feedback digital bit D are arranged to hold both parasitic capacitances C_P discharged to ground except around time interval ϕ_2. This suppresses a mechanism for data-dependent charge drain from the reference voltage and eliminates an active buffer for the reference. A simple RC filter from the battery supply, as shown, performs well as a reference

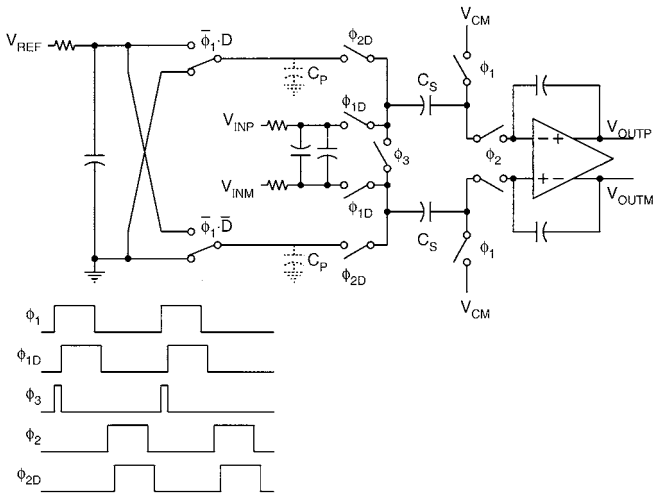

Fig. 4. First $\Sigma\Delta$ ADC integrator.

supply in this system. Fig. 5 shows the measured performance of the ADC modulator operating at 1.28 MHz. It achieves a dynamic range of 87 dB unweighted from 100 Hz to 10 kHz and 92-dB signal to distortion, drawing a 66-μA supply current. Following the ADC modulator, the decimation filter consists of a cascade of five polyphase finite impulse response (FIR) filters, each decimating by two with a transfer function $H(z)$ of

$$H(z) = \left(1 + z^{-1}\right)^4. \tag{1}$$

Droop from this filter is partially corrected by an FIR filter with a transfer function $H_{\mathrm{FIR}}(z)$ of

$$H_{\mathrm{FIR}}(z) = 1 + \left(1 - z^{-2}\right) * 3/16. \tag{2}$$

The combined decimation plus droop correction filter draws an 8-μA supply current.

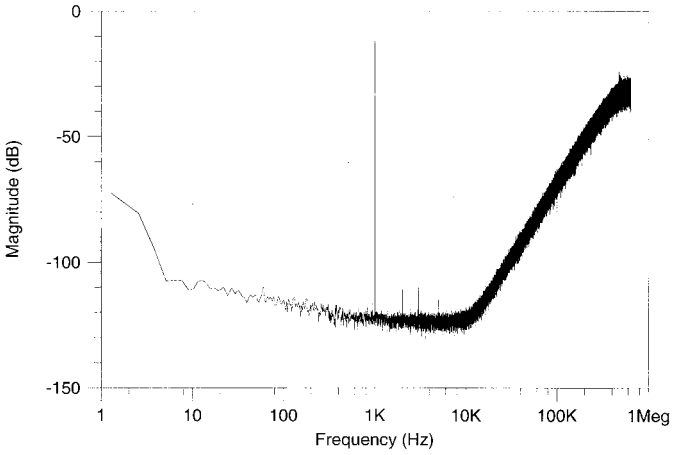

Fig. 5. Measured ADC spectrum.

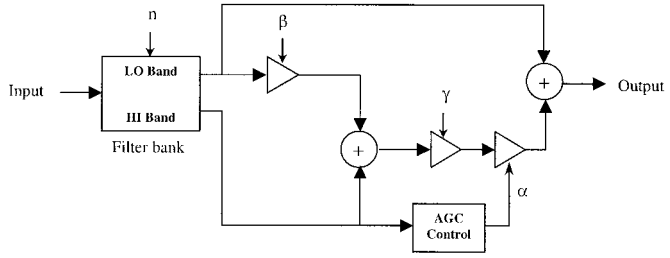

Fig. 6. Two-band AGC algorithm.

IV. Digital Signal Processing Section

Fig. 6 shows a basic block diagram of the signal processing algorithm. The input signal is split into two frequency bands. Each subband is processed and then summed to provide a full bandwidth output. While the algorithm seems simple, the programmable parameters n, β, and γ provide quite a bit of flexibility. Parameter n selects the transition characteristics between the low- and high-frequency bands. Parameter β enhances the low-frequency response by adding a fraction of the low-frequency signals through the high-frequency AGC channel. Parameter γ primarily controls the amount of high-frequency gain. The high-frequency channel has AGC. The AGC function is controlled by the signal from the high-band output of the filter bank and generates parameter α controlling the AGC multiplier.

The filter is implemented as an FIR filter. This eliminates the finite word-length problems of infinite impulse response (IIR) filters such as overflow and limit cycles. With the FIR filter, the required word length at each part of the filter is deterministic. Unlike IIR filters where the word length is often made wider to minimize limit cycles, for example, the approach with FIR filters allows the word lengths to be optimized, resulting in less hardware, lower power, and smaller size. To further optimize the design, the FIR filter uses coefficients that are 2^n values, and, in fact, all filter coefficients are 0.5. Multiplying by 0.5 is implemented by hardwired shifting of the signal bits and hence uses no power, or gates and is minimal size. The values of β and γ are also selected from 2^n values and hence the β- and γ-multipliers are nothing more than a multiplexer implementing a selectable shifting function. With these optimizations, only one full multiplier is needed and is used only once per sample period. This is in contrast to a general-purpose DSP core and common DSP algorithms, where a single multiplier is used to perform many multiplications during each sample period.

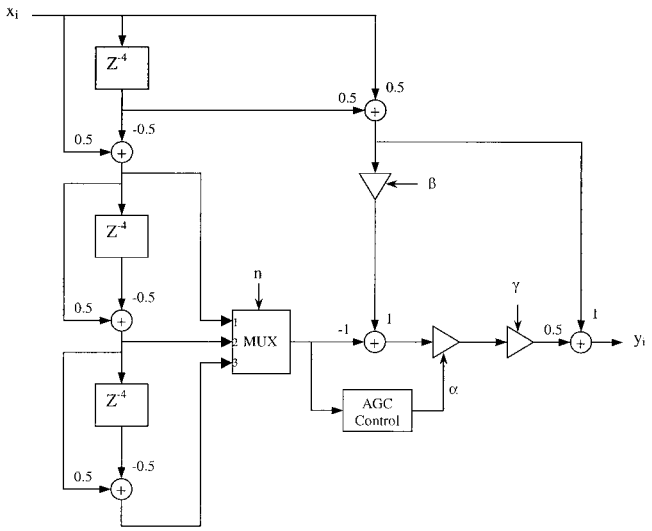

Fig. 7. Digital signal processor.

The band splitting filter has been optimized for minimal circuitry, size, and power. Instead of using a more traditional low-pass and high-pass band splitting structure, a band-pass and notch-filter structure [4] was chosen. By selecting the appropriate sampling rate, the band-pass/notch structure provides psychoacoustically similar results to low-pass/high-pass structures. The advantage of the band-pass/notch structure is again a reduction in the power dissipation and physical size of the filter.

Originally, the digital filter was designed for a sample rate of 20 kHz. During the design of the IC, it was determined that, if the bitstream from the $\Sigma\Delta$ ADC is downsampled to only 40 kHz, and each Z^{-1} delay in the filter was replaced with a Z^{-2} delay (i.e., a double delay), the power savings of the smaller decimation filter and the elimination of an interpolation filter in favor of a simple sample-and-hold circuit more than offset the added power of the additional delay elements. Therefore, the 40-kHz sample rate was used. Fig. 7 shows the final digital signal filter structure. The overall transfer function $H_T(z)$ is given by

$$H_T(z) = \Big[(1+0.5\alpha\beta\gamma)\left(0.5+0.5z^{-4}\right) -(0.5\alpha\gamma)\left(0.5-0.5z^{-4}\right)^n\Big]. \quad (3)$$

Parameters n, β, and γ are programmable. Parameter α is determined by the AGC control circuit based on the level of the signal at the output of the multiplexer. Figs. 8–10 show the effect of each of the programmable parameters on the frequency response of the filter.

V. Sigma–Delta DAC

The sigma–delta DAC has a 20-b signed input at a sample rate of 40 kHz, ideally giving it a dynamic range of 120 dB. The dynamic range as designed was approximately 103 dB and the SNDR was approximately 80 db. The three-level fourth-order sigma–delta DAC minimizes power consumed in the output H-bridge driver, since most samples will be zero for the typical audio levels well below full scale. Increasing the quantization

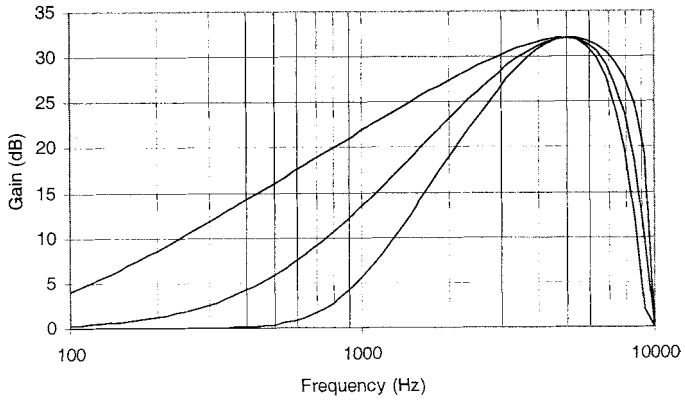

Fig. 8. Effect of varying n on a typical frequency response.

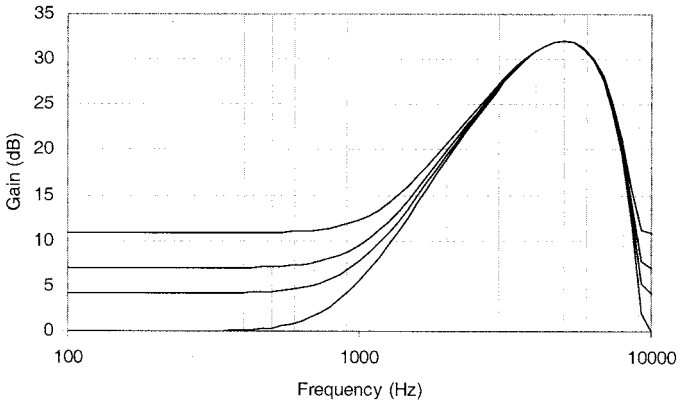

Fig. 9. Effect of varying β on a typical frequency response.

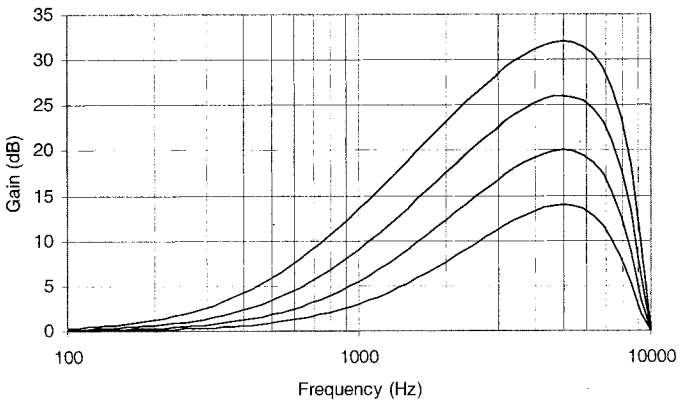

Fig. 10. Effect of varying γ on a typical frequency response.

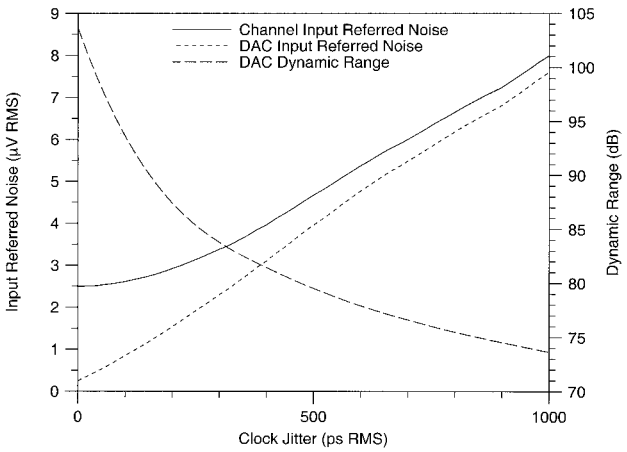

Fig. 11. Simulated DAC performance versus clock jitter.

levels in the output of sigma–delta modulators improves the noise performance and stability of the loop. Typically, a two-level output is used since it is ideally linear and the accuracy of the quantization steps limits the sigma–delta performance. Since the speaker was to be driven differentially, we were able to sum the two ideally linear outputs in the load. This technique creates a three-level (-1, 0 $+1$) or 1.5-b highly linear output. In addition, since the required output power is usually very low, the output waveform is typically driven to zero with occasional single pulses of either -1 or $+1$. For a small signal, this consumes far less power than a traditional two-level sigma–delta that must constantly switch between -1 and $+1$ such that the output average is nearly zero.

For the chosen process and the given load, the switch-mode output-stage power efficiency peaks at about 600 kHz. Given the clocks available, it was convenient to generate a 640-kHz clock. The response of the speaker being used rolls off quickly over 8 kHz and acts as the reconstruction filter for the sigma–delta DAC that gives us an effective over sampling ratio of 32.

Clock jitter modulates the pulse width of the DAC output stream, which causes high-frequency sigma–delta quantization noise to mix down into the baseband. Fig. 11 shows the simulated effects of clock jitter on dynamic range and input referred noise using nominal channel parameters,[1] which illustrates the importance of reducing clock jitter in the oscillator. With a fourth-order modulator, the overall noise performance of the DAC is limited by clock jitter and would not be improved by increasing the modulator order.

Return-to-zero (RTZ) coding is used to preserve linearity by improving the uniformity of the shape of the output pulses, which prevents high-frequency quantization noise from mixing down into the baseband. The RTZ pulse edges are resynchronized to the lowest jitter clock in the system just before feeding the output buffers, as shown in Fig. 12. This reduces sensitivity to jitter in the DAC circuitry and saves system power by requiring the supply current be spent only to suppress jitter in the clock oscillator core.

The three-stage ring oscillator shown in Fig. 13 provides a low-jitter clock. The bias current for all stages is trimmed at test to set the clock frequency to 2.56 MHz. The delay in each stage is implemented by symmetrical p and n transconductances and load resistances driving the gate capacitance of the next stage. Symmetry is essential to match clock waveform rise and fall times and reduce up-conversion of $1/f$ noise [5]–[9]. In addition, extra capacitance added at the tail nodes C_T significantly reduces jitter from kickback and from current source noise. The bias current is digitally trimmed to set the oscillation frequency and is designed to vary linearly with temperature to reduce frequency variation over temperature.

[1]The nominal channel parameters are: ICL gain fixed at 34 dB, $\alpha = 10$, $\beta = 1/16$, $\gamma = 1$, and $n = 1$, giving a nominal channel gain of 31.5 dB at 5 kHz.

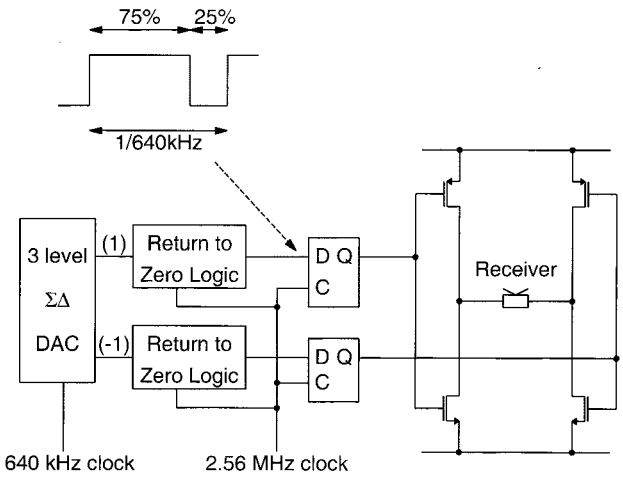

Fig. 12. $\Sigma\Delta$ DAC and H-bridge timing.

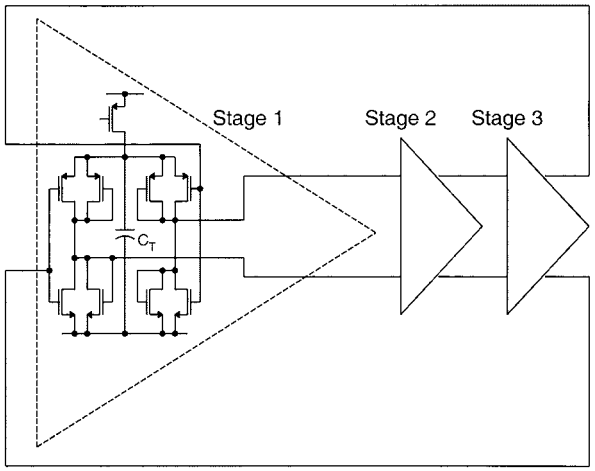

Fig. 13. Clock oscillator schematic.

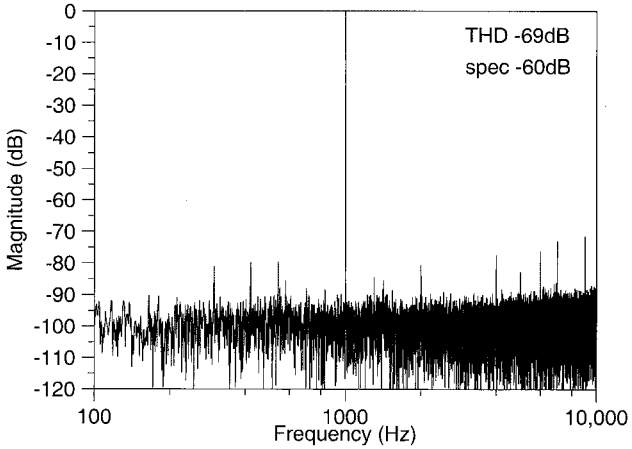

Fig. 14. Measured FFT response $v_{\text{in}} = 4$ mV peak.

VI. Measured Results

A measured output voltage spectrum is plotted in Fig. 14. The input is a 1-kHz sinusoid at a 4-mV peak amplitude. The ICL has a gain of 50, making the 0-dB level 200 mV. This level corresponds to loud conversational speech at about 79 dB SPL and is 6 dB below the level where gain compression is initiated by the input stage. The output is loaded with a test circuit equivalent to the complex impedance of a receiver. Harmonic distortion at -69 dB is well below the 0.1% specification for low-level inputs. Fig. 15 is the measured fast Fourier transform (FFT) response with an 80-mV peak amplitude at 1 kHz and input amplitude well into the compression region of the ICL circuit. With

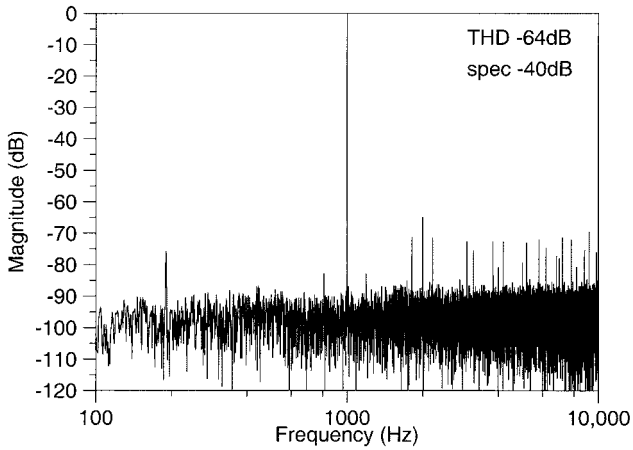

Fig. 15. Measured FFT response $v_{\text{in}} = 80$ mV peak.

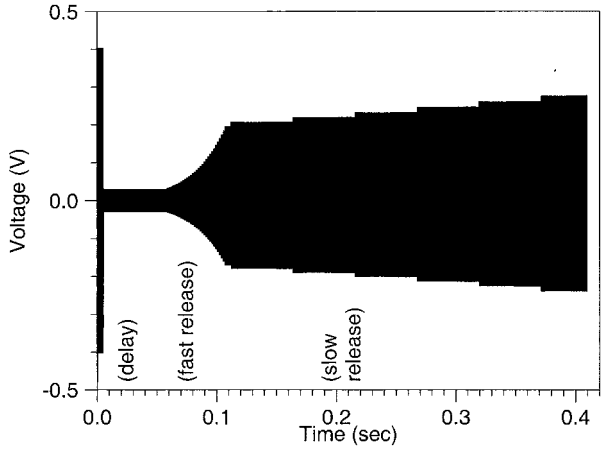

Fig. 16. Measured attack and release response for a short compression transient.

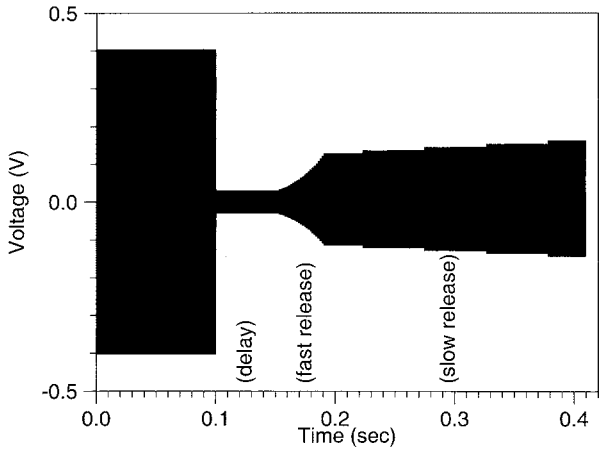

Fig. 17. Measured attack and release response for a long compression transient.

TABLE I
PERFORMANCE SUMMARY

Battery voltage range		1.1-1.5V
Battery current consumption (no signal)		
1.1V supply		
Analog	173μA	
Digital	48μA	
H-Bridge	15μA	
Ring oscillator	34μA	
Total		270μA
1.3V supply		299μA
1.5V supply		323μA
-3dB bandwidth		100Hz-10kHz
Input referred noise (100Hz-10kHz)		2.8μVRMS
Total harmonic distortion		
v_{IN}=7mVpk		0.02%
v_{IN}=80mVpk		0.5%
Input compressor maximum gain step error		0.09dB
Maximum input signal		450mV peak
Clock jitter		147ps RMS
Sub-bandgap reference stability		1%
Temperature range		20-40°C
Die size in 0.6μm, 3.3V CMOS		12mm^2

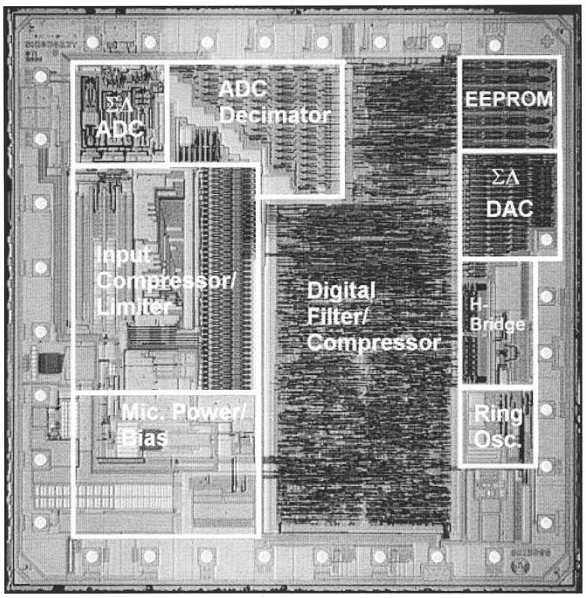

Fig. 18. Die micrograph.

an ICL gain of 50, this makes the 0-dB level equal to 800 mV in Fig. 15. The measured THD at −64 dB is well below the specification limit for the compression region. Figs. 16 and 17 show the release characteristics of the ICL. The output signal is shown when the input signal is suddenly decreased by 20 dB. The output initially drops 20 dB. After a short delay, the fast release shift register controls the compression and begins to increase the gain. Finally, the slow release shift register takes over and continues to increase the gain at a slower rate. The figures show that, for a longer time initially spent in compression, the fast release time is shorter and the slow release period starts at a lower gain and will take longer to get back to full gain. Table I summarizes the chip performance. Fig. 18 shows a microphotograph of the die.

VII. CONCLUSION

A single-chip mixed-signal chip for a hearing aid instrument has been successfully implemented in a 0.6-μm 3.3-V CMOS process. The typical input referred noise of the complete channel is 2.8 μVrms. The typical total harmonic distortion of the complete signal channel is less than 0.02%. The IC consumes a total current of 270 μA at 1.1 V and 299 μA at 1.3 V. The complete chip, including bond pads, measures 12 mm^2.

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While in graduate school, his research was on the effects of a laser on the properties of semiconductor devices. He joined Texas Instruments, Inc. (TI), Houston, in 1979 and began working as a design engineer on telecommunications integrated circuits for TI terminal products. While in Houston, he was project leader for four CMOS IC modem designs and was promoted to manager of a design team in 1983. In 1986, he moved to TI in Dallas with his design team and joined the Mixed Signal Department of TI's Semiconductor Division as design section manager for telecommunications and analog interface circuits. He was made a Senior Member of the Technical Staff in 1987. He was promoted to design branch manager for telecommunications, wireless, and audio IC design in 1991 and was instrumental in developing TI's wireless baseband business. From 1997 to 2001, he was director of the design department for the Mixed Signal DSP Solutions Organization. In that role, he managed design teams that work on a variety of devices ranging from audio and video applications, modems, optoelectronics, speech and high-speed digital bus interfaces. Since 2001, he has been a key technical advisor on broadband solutions for high-speed data modems. He has also been active in university recruiting and relations teams, and is on the advisory board for the Electrical Engineering Department at Texas A&M University and is TI's representative to SRC Integrated Circuits and Systems Science Area. He holds five patents and has authored several articles on CMOS circuit design.