INTEGRATED OPTICAL 1×8 POWER SPLITTER IN SOI PLATFORM

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THESIS CERTIFICATE

This is to certify that the thesis entitled **"INTEGRATED OPTICAL 1×8 POWER SPLITTER IN SOI PLATFORM"**, submitted by **Solomon Krubhakar. I**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Science (by Research)**, is a bonafide record of the research work carried out by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Dedicated to my Wife,
Daughter and Parents

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ABSTRACT

KEYWORDS: Integrated Optics; Power splitter; Multimode Interference Coupler; Silicon On Insulator; Silicon Photonics.

Integrated optical power splitter is an important component in passive/active optical network systems. Currently, such power splitters are being fabricated mostly in silica-on-silicon platform using planar light-wave circuit technologies. Because of the recent advancements of CMOS technology, there is a huge possibility of demonstrating compact power splitters in silicon-on-insulator (SOI) platform. In this work, we have demonstrated multimode interference (MMI) based integrated optical 1x8 power splitter in SOI substrate with large cross-section single-mode input/output waveguides.

The design parameters were optimized in accordance with our fabrication limitations ($\sim$ 2 μm smallest feature size). The device basically consists of one single mode input waveguide, eight single mode output waveguides and a multimode waveguide (MMI region) in between. The device parameters have been optimized by BPM simulation results and fine-tuned based on preliminary experimental investigations. While optimizing the design parameters, care was taken to minimize the wavelength / polarization dependencies, insertion loss, excess loss and throughput power non uniformity among the output waveguides. The device has a footprint of $\sim$ 18 mm $\times$ 1.8 mm and is designed such that it could be pigtailed with standard single mode fibers. Typical spot-size of the guided fundamental mode in these waveguides is estimated to be $\sim$ 7.2 μm x 4.6 μm - comparable to that of standard single-mode fiber operating at $\sim$ 1550 nm.

With a set of optimized design parameters, 1$\times$8 optical power splitters were fabricated on a commercially procured optical grade SOI substrate (Device layer (Si): $\sim$ 5 μm, BOX layer: $\sim$ 1 μm, Substrate layer: $\sim$ 500 μm). The power splitter structures have been defined photolithographically followed by reactive ion etching process.

All the fabricated devices have been characterized in terms of excess loss, insertion loss, non-uniformity in throughput powers and polarization / wavelength dependencies (1530 nm < λ < 1580 nm). The devices were found to be nearly wavelength / polarization insensitive. By analyzing the experimental results, we have observed typical insertion loss of 16 dB with power non-uniformity of 0.7 dB among output ports and excess loss of 7.6 dB. A prototype 1×8 power splitter have also been pigtailed with standard single-mode fiber and packaged. The characterization results suggest that such power splitters can be potentially useful in passive/active optical networks operating in the communication window of $\sim$ 1550 nm and it can be scalable for the realization of 1×16, 1×32, 1×64, etc., power splitters for the use in fiber to the home/office (FTTH/FTTX) networks. The design of such power splitters can also be modified further for the development of arrayed waveguide grating (AWG) devices for multiplexing / de-multiplexing operations in DWDM systems.

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ABBREVIATIONS

Acronyms

AWG	Arrayed Waveguide Grating
Band C	Conventional wavelength band ($\lambda \sim 1527$ to 1567 nm)
Band L	Long wavelength band ($\lambda \sim 1567$ to 1607 nm)
BOX	Buried Oxide
BPM	Beam Propagation Method
CMOS	Complementary Metal Oxide Semiconductor
DI	De-ionized (water)
DWDM	Dense Wavelength Division Multiplexing
FEM	Finite Element Method
FOCT	Fiber Optic Communication Technology
FPR	Free Propagation Region
FSR	Free Spectral Range
FTTH	Fiber To The Home
FTTX	Fiber To The Office
ICP	Inductively Coupled Plasma
ITU	International Telecommunication Union
LCRW	Large Cross-section Rib Waveguide
MMI	Multimode Interference
OLT	Optical Line terminal
ONU	Optical Network Unit
OPS	Optical Power Splitter
PhWW	Photonic Wire Waveguide
PIC	Photonic Integrated Circuit
PLC	Planar Lightwave Circuit
PON	Passive Optical Network
PPR	Positive Photo Resist

RIE	Reactive Ion Etching
SEM	Scanning Electron Microscope
SMF	Single Mode Fiber
SOI	Silicon-On-Insulator
TE	Transverse Electric (polarization)
TM	Transverse Magnetic (polarization)
UV	Ultra-Violet

Chemical Names

Al	Aluminum
Ar	Argon
Au	Aurum (Gold)
CHF_3	Tri-fluoro Methane
Cr	Chromium
HF	Hydro Fluoric Acid
HNO_3	Nitric Acid
H_2O	Water
H_2O_2	Hydrogen Peroxide
KOH	Potassium Hydroxide
$LiNbO_3$	Lithium Niobate
NaOH	Sodium Hydroxide
SF_6	Sulfur Hexafluoride
Si	Silicon
SiO_2	Silicon dioxide
TCE	Tri-chloro Ethylene

Units

dB	Decibel
dBm	Decibel milli-Watts
mW	milli Watts
GHz	Giga Hertz

Gbps	Giga-bits per second
μm	Micrometer
ps	Pico Second
g	gram
s	Second
min	Minutes
sccm	standard cubic centimeter per minute
mTorr	milli-Torr (of pressure)
mbar	milli-Bar (of pressure)
ml	milli-liter (of fluid)

NOTATION

W	Rib waveguide width [μm]
H	Rib waveguide height [μm]
h	Slab height [μm]
$\boldsymbol{r}$	$\frac{h}{H}$ ratio
n	Refractive index
$\mathbf{n}_{eff}$	Effective refractive index
$\boldsymbol{M}$	Number of input waveguides
$\boldsymbol{N}$	Number of output waveguides
$\boldsymbol{\lambda}$	Wavelength [nm]
$\boldsymbol{\beta}$	Propagation constant [rad/m]
$\boldsymbol{\phi}$	$\boldsymbol{\nu^{th}}$ mode field distributions
$\boldsymbol{\psi}$	Input guided mode field
$\boldsymbol{R}$	Arc radius of bend waveguides [μm]
$\boldsymbol{L_{MMI}}$	Length of multimode interference region [μm]
$\boldsymbol{W_{MMI}}$	Width of multimode interference region [μm]
$\boldsymbol{L}$	Length of multimode interference region for $\boldsymbol{N}$ images [$\boldsymbol{\mu}$m]
$\boldsymbol{\omega_x}$	1/e width of guided mode in horizontal direction (along x-axis) [μm]
$\boldsymbol{\omega_y}$	1/e width of guided mode in vertical direction (along y-axis) [μm]

CHAPTER 1

INTRODUCTION

The advent of fiber optic communication technology (FOCT) revolutionized the telecommunication field in transferring the information from one place to other. Immunity to electromagnetic interference, exceptionally low loss, high data-carrying capacity, very low crosstalk, lighter weight, lesser cost, etc., are some of the major advantages of FOCT [1], [2]. Thus, optical fiber could replace the conventional copper transmission lines and gives a way to manage the rapidly increasing communication network traffic. However, the communication throughput has been affected due to the nodal components of the optical networks [3]. When an optical network is comprised of passive components, it is referred as passive optical network (PON). Schematic of a simple PON is shown in Fig. 1.1. A PON is mainly comprised of optical distribution networks (which consists optical fibers and power splitters), an optical line terminator (OLT - located at service provider's central office) and number of associated optical network units (ONUs - located at end customer's premises).

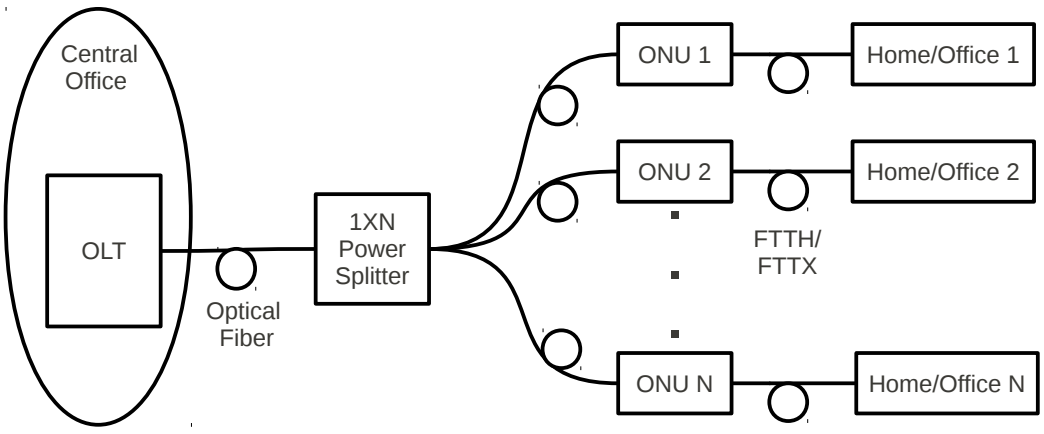


Figure 1.1: Scheme of a simple passive optical network (OLT - Optical Line Terminal; ONU - Optical Network Unit).

In the PONs, optical fibers have been already deployed until ONUs, after which copper cables are still being used to reach the end customer in most of the places. This

is in fact affecting the required bandwidth and the performance of the optical network. In order to provide the consumer's demands like *triple play services* (voice, data, and video) via internet/intranet, optical fiber network requires higher bandwidth. The above mentioned advantages of FOCT provided a way for the implementation of fiber to the home/office (FTTH/FTTX) applications, where the optical fiber is extended until the destination of the consumer locations with the help of optical devices like power splitters, switches, (de-)multiplexers, etc. In this way the required bandwidth is currently being obtained more efficiently. Optical power splitters play a major role to achieve this. Even though fiber based power splitters have been employed in some PONs, the control over output power uniformity, thermal stability, etc., degrade the performance. These difficulties can be avoided if we use integrated optical power splitters. Moreover, other important devices of optical networks like AWGs, switches, sources and modulators can also be integrated along with the power splitter in a single chip - photonic integrated circuits (PICs). By understanding the significance of integrated optical power splitter in optical networks, it has been considered as subject for my MS research work.

1.1 Motivation: Why SOI based MMI Power Splitter?

In general, integrated optical M$\times$N power splitters (M input and N output ports) can be designed based on different principles like cascaded Y junction [4], cascaded directional coupler [5], free propagation region [3] and multimode interference [6]. The working principle and merits/demerits of all these devices are very briefly discussed here.

(1) Cascaded Y Junction

Y-junction waveguide structures are usually used for the integrated optical 1$\times$2 power splitters. By cascading required number of 1$\times$2 power splitters, one can realize 1$\times$N power splitter (see Fig.1.2). Such power splitters have widespread applications in integrated optics such as Mach-Zehnder interferometer (modulator), sensors, etc [4]. Limitations of this kind are: (a) when realizing 1$\times$N structures by cascading 1$\times$2 structure, (see Fig.1.2), the excess/insertion losses and polarization dependent loss also get added

up; (b) the device package density in PICs will be less as the cascaded device structure is larger; (c) batch fabrication will get affected due to the larger device footprint.

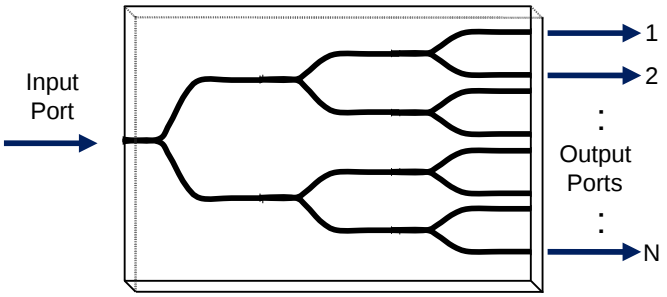


Figure 1.2: Schematic top view of cascaded Y junction based 1×8 optical power splitter

(2) Cascaded Directional Coupler

A directional coupler mainly consists of two closely spaced coupled waveguides, where the transmitted light in one waveguide is coupled to other waveguide by evanescent field coupling [5], [7]. Other sections of directional coupler consist of S-bend waveguides to launch and collect light at input and output ends respectively. By cascading directional couplers, one can design a power splitter with desired number of input and output ports (see Fig.1.3). However, because of many number of bend waveguides and larger device dimension, the excess loss of the cascaded device increases. The dependency on polarization and wavelength are other major disadvantages.

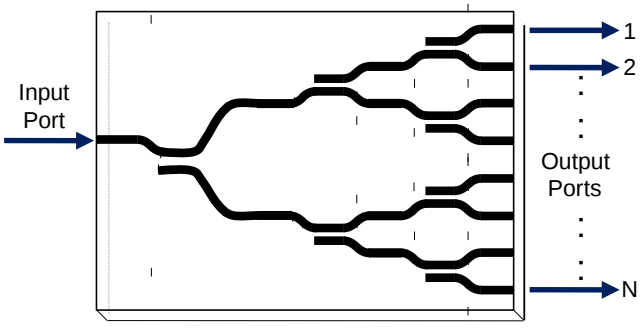


Figure 1.3: Schematic top view of cascaded directional coupler based 1×8 optical power splitter

(3) Free Propagation Region

The structure contains single mode input and output waveguides connected by wide planar waveguide which acts as free propagation region (FPR) (see Fig.1.4). When the light from the input waveguide emerges into the planar waveguide, it is freely expanded in FPR and is distributed into the output waveguides (where the output waveguides are kept with separation in between them, in accordance with the fabrication limitation). The device is compact in size and thus suitable for batch process. This device is also useful to design AWGs. However, the leakage of light at FPR-output waveguide junction increases the insertion/excess loss and also the non uniformity in output power distribution [3].

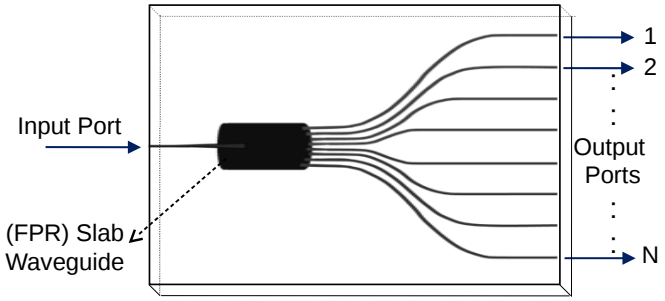


Figure 1.4: Schematic top view of free propagation region based 1×8 optical power splitter

(4) Multimode Interference (MMI)

MMI power splitter consists of single mode input and output waveguides connected with a multimode waveguide (see Fig.1.5). When the input light enters from the single mode waveguide into the multimode waveguide region, higher order modes are excited. Because of the superposition of the excited modes, single or multiple images are formed as they propagate inside the multimode waveguide region. This principle is called as self imaging [6], [3]. Output waveguides can be kept at the specific locations at the other end of MMI region to collect the light from the images. In this way the input light power can be distributed into many output ports. MMI power splitter is more efficient than other kind of power splitters in terms of size, fabrication yield, excess/insertion losses.

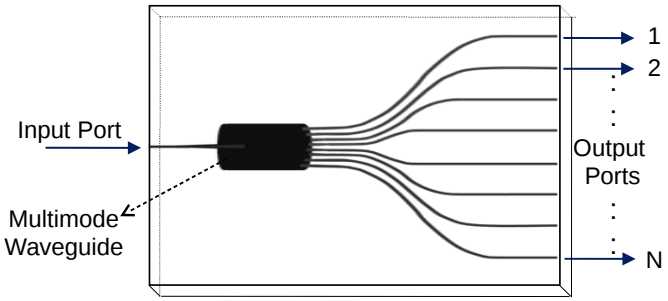
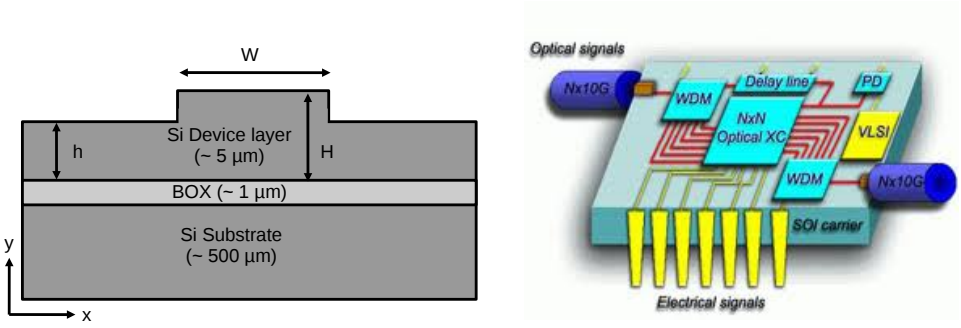


Figure 1.5: Schematic top view of multimode interference based 1×8 optical power splitter

Integrated optical power splitters (OPS) with various specifications are already commercially available. The commercially available power splitters are mostly fabricated on silica on silicon platform, using the planar lightwave circuit (PLC) technology. Silica on silicon based OPS exhibits low loss and shows the possibility of mass production using the PLC technology, which is a relatively simpler fabrication process [3]. But as the device layer is silica, OPS can be used only for passive applications and the packing density of PICs will be less when comparing to silicon based technology. Moreover, monolithic integration of electronically tunable and reconfigurable photonic devices like sources, modulators and other devices, along with the power splitter is not possible in these devices, as the device layer is silica. Eventhough, III-V semiconductors and $LiNbO_3$ platforms give the way to fabricate active devices, the processing technologies of these devices are relatively complex and expensive [8], [4], [9], [10]. On the other hand, Silicon on insulator (SOI) is an excellent material platform for various functional photonic devices [11]. As the silicon is device layer here, we can utilize the advantages of silicon as listed below:

1. Wide transparency to communication wavelengths (absorption loss is 0.004 dB/cm at λ = 1.55 μm)
2. Free carrier absorption loss can be very well reduced by using undoped silicon wafers
3. Commercial availability of optical grade SOI wafers
4. Substrate radiation loss is very small, because buried oxide (BOX) layer is used as a bottom cladding
5. Higher refractive index contrast allowing tighter light confinement
6. Electro-optic / Thermo-optic control of light



(a) (b)

Figure 1.6: (a) Schematic cross sectional view of input/output rib waveguide structures in SOI platform (b) scheme of a PIC, where different components like lasers, WDM devices, power splitters, modulators, cross connectors, etc,. are integrated together in a single chip, alongwith the electronic components.

7. Well established CMOS technology can be used for integrating optics and electronics [12].

Cross sectional view of the rib waveguide structure with the commercially available SOI wafer is schematically shown in Fig. 2.3(a). The SOI based integrated optical/photonic devices are especially attractive due to their compatibilities with CMOS technology. Various photonic devices [13] like directional couplers [14], star couplers [15], [16], arrayed waveguide gratings (AWGs) [17], modulators [18], [19], light sources [20], etc. have already been demonstrated using photonic wire waveguide structures in SOI platform. These individual achievements show a possibility to realize a SOI based photonic integrated circuits (PICs) along with electronic components. Scheme of one such possible PIC is shown in 2.3(b).

Though the performance of the photonic wire waveguide devices are reasonably good and very compact in nature, they could not be commercialized yet because of less fabrication reproducibility, relatively more polarization dependent and exhibits higher optical losses (waveguide scattering losses and fiber to waveguide coupling losses). However, the devices with large cross-section rib waveguide (LCRW) structures in SOI platform could be an immediate alternative to overcome the above mentioned drawbacks, and the typical mode size in LCRWs is comparable with the fiber mode size [4]. Understanding the advantages of LCRW structure based devices in SOI platform,

people from our laboratory have already demonstrated various photonic devices like, single mode straight and S-bend waveguide [21], [22], directional couplers [7], [23], 1×4 power splitter [24] and dispersion free interleaver [25], [26], [27]. In this series, it has been considered to realize the basic element of optical communication network - the power splitter - also in SOI platform using LCRW structures. Therefore, it is proposed to demonstrate an integrated optical 1×8 power splitter in SOI platform using LCRW structures for my MS research.

1.2 Objective of the Work

The objective of my MS research work on demonstrating the integrated optical power splitter in SOI platform includes:

1. Theoretical understanding of MMI based power splitter,
2. Design of 1×8 power splitter based on BPM simulation,
3. Optimization of fabrication process,
4. On-chip characterization of the fabricated devices,
5. Fiber pig-tailing, packaging and testing of the prototype device.

1.3 Organization of the Thesis

This thesis starts with an introduction to optical power splitters and their applications in optical communications. In Chapter 1, the advantages of MMI based power splitters are discussed followed by the significance of the choice of SOI material platform to fabricate the device. Chapter 2 begins with a short discussion on the working principle of MMI power splitter. The complete design aspects for each part of the device based on BPM simulation results are discussed in detail and optimized design parameters of the device are also reported in this Chapter 2.

Fabrication process flow along with optimization of fabrication process parameters are discussed in Chapter 3. Optical characterization setup used and experimental results of all the fabricated devices in terms of output power obtained, excess/insertion losses

are also discussed in Chapter 3. Some of the best devices were fiber pigtailed/packaged and tested for the device performance. The performance of the devices before and after packaging and the corresponding issues are discussed in Chapter 4. Finally, the thesis conclusions contains summary of the research work that has been carried out and outlook for the further development of the research based on this device.

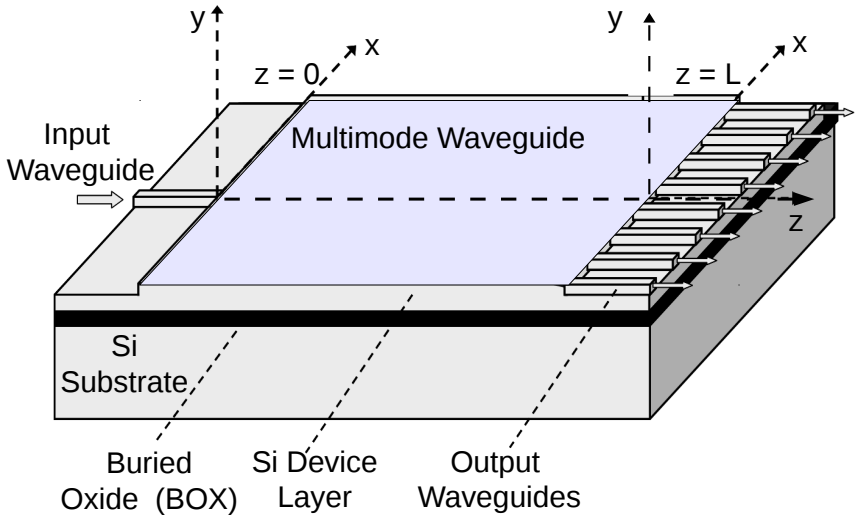
CHAPTER 2

DESIGN OF INTEGRATED OPTICAL 1×8 POWER SPLITTER

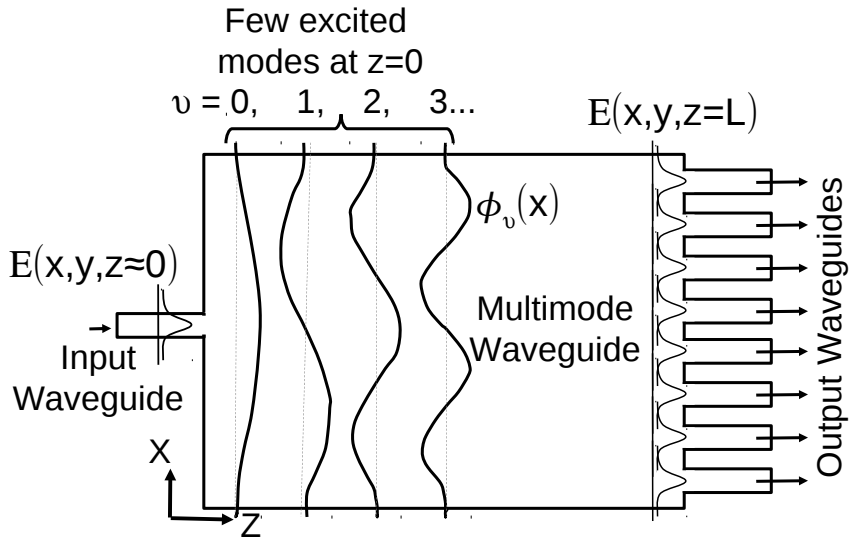
In this Chapter, the theory of MMI based integrated optical power splitter is briefly discussed. Afterwards, critical design parameters and their optimized values using BPM simulation for a 1×8 optical power splitter, to be fabricated later on SOI platform is reported.

2.1 Background Theory : MMI based Power Splitters

In an optical waveguide, light is propagated from one end to other end in the form of confined eigen modes [4]. These modes are conventionally known as guided modes. A waveguide which can support more than one eigen mode is called as multimode waveguide. When light from single mode waveguide is allowed to enter into the multimode waveguide, higher order modes are excited alongwith fundamental mode. The number of excited modes depends on the dimensions of the multimode waveguide. By properly choosing the dimensions of multimode waveguide region, the phase relationship of all the excited guided modes can be made in such a way that, superposition of all the excited guided modes can appear as single or multiple images of the input guided mode, at a finite length of MMI waveguide. This is known as self-imaging principle. These image(s) can be the source(s) for outward single-mode waveguide(s). Thus, one can design 1×N, 2×N,.....M×N power splitters based on self imaging principle. Detailed theory of MMI power splitter has been explained using guided mode approximation method by Soldano et al [6]. As the present work is focused on 1×8 power splitter in SOI platform, the scheme as shown in Fig.2.1(a), has been chosen conveniently for theoretical analysis.



(a)



(b)

Figure 2.1: (a) 3D scheme of a SOI based integrated optical 1x8 power splitter, (b) schematic top view of the power splitter showing few excited higher order guided modes and their superposition in the multimode (MMI) region, which forms multiple images of the input mode-field distribution.

The thickness of the device layer is chosen such that only the $\psi(x,y)_{00}$ and $\psi(x,y)_{\nu_0}$ modes are supported by the single-mode and multi-mode waveguide, respectively. Here, ν is the eigen mode number along X-axis. The dispersion relation of ν^{th} mode can be expressed as:

$$\beta_\nu^2 + k_{x\nu}^2 = \left(\frac{2\pi n_{MMI}}{\lambda_0}\right)^2, \tag{2.1}$$

where β_ν is the propagation constant and $k_{x\nu}$ is the lateral component of the wavevector corresponds to ν^{th} mode; n_{MMI} is the effective index of the multimode region for vertical confinement of light and λ_0 is the free space wavelength. From modal analysis of guided light in MMI region, $k_{x\nu}$ can be expressed as:

$$k_{x\nu} = \frac{(\nu+1)\pi}{W_\nu^e} \tag{2.2}$$

where W_ν^e (slightly greater than W_{MMI}, the physical width of the MMI region) is the effective width of the ν^{th} mode in MMI region. Assuming $W_\nu^e \approx W_{MMI}$, the propagation constant of ν^{th} mode can be approximated as:

$$\beta_\nu \approx \beta_0 - \frac{\nu(\nu+2)\pi}{3L_\pi}, \tag{2.3}$$

where $L_\pi = \pi/(\beta_0 - \beta_1)$, is the beat length between two lowest order modes. The input field $\psi(x, z \simeq 0)$ can be expressed as a weighted summation of all the guided modes supported by the multimode region:

$$\psi(x, z \simeq 0) = \sum_{\nu=0}^{m} c_\nu \phi_\nu(x), \tag{2.4}$$

where (m+1) number of guided modes are supported in MMI region, and c_ν is the excitation coefficient of ν^{th} mode field - which can be calculated as the overlap integrals of the normalized ν^{th} mode profile $\phi_\nu(x)$ and the normalized field profile from input waveguide $\psi(x, z \simeq 0)$. The field distribution is evolved as a function of propagation length of MMI region and it can be written as:

$$\psi(x, L) = \exp(-j\beta_0 L) \sum_{\nu=0}^{m} c_\nu \phi_\nu(x) \exp\left[-j(\beta_\nu - \beta_0)L\right]. \tag{2.5}$$

By substituting the expression of β_ν from Eq.(2.3) into Eq.(2.5), one can rewrite Eq.(2.5)

as:

$$\psi(x,L) = \sum_{\nu=0}^{m} c_\nu \phi_\nu(x) \exp\left[j\frac{\nu(\nu+2)\pi}{3L_\pi}L\right]. \tag{2.6}$$

Depending on the phase relationship among all the excited guided modes along propagation direction, the superposition of all the excited guided modes forms single or multiple images of the input guided mode, if the phase factor satisfies the following condition,

$$\exp\left[j\frac{\nu(\nu+2)\pi}{3L_\pi}L\right] = 1(or)(-1)^\nu. \tag{2.7}$$

If symmetric input field is launched (here, fundamental mode is launched at the center of the multimode region), only the even symmetric modes will be excited due to the reason that the overlap integral of input fundamental mode and the excited higher order odd modes will become zero, (i.e.$c_\nu = 0$ for $\nu = odd$). Moreover, for ν = even, we have $\nu(\nu+2)$ is exactly divisible by 4. So if we choose the length of MMI, $L_{MMI} = 3L_\pi/4$, then we can get single self imaging of input field. By controlling the length of MMI region one can have desired number of images at the output. It has been shown by Bachmann et al [28] that, in order to get N images of the input field, the required length of MMI region is,

$$L_{MMI} = 3L_\pi/(4N). \tag{2.8}$$

Each of these images can be considered as the source point for output waveguides of the power splitter. In this way the input light power can be distributed into many number of output waveguides.

The design parameters have been optimized for the given device dimensions by considering low excess loss and low non-uniformity in output power distribution. The optimization of the device design parameters are detailed in the following Section.

2.2 Design Principles

The beam propagation method (BPM) is a most widely used computational technique for simulating the propagation of light in optical waveguides. BPM is a fast and simpler

method to solve for guided modes as well as radiation field with intensity distribution in integrated optical waveguide devices. Finite difference - beam propagation method (FD-BPM) based simulation tool [29] has been used to design the optimum device parameters.

Design details of the integrated optical 1×8 power splitter based on commercially available SOI wafer has been discussed in this section. The scheme of the proposed device is shown in Fig. 2.2. The critical design parameters includes:

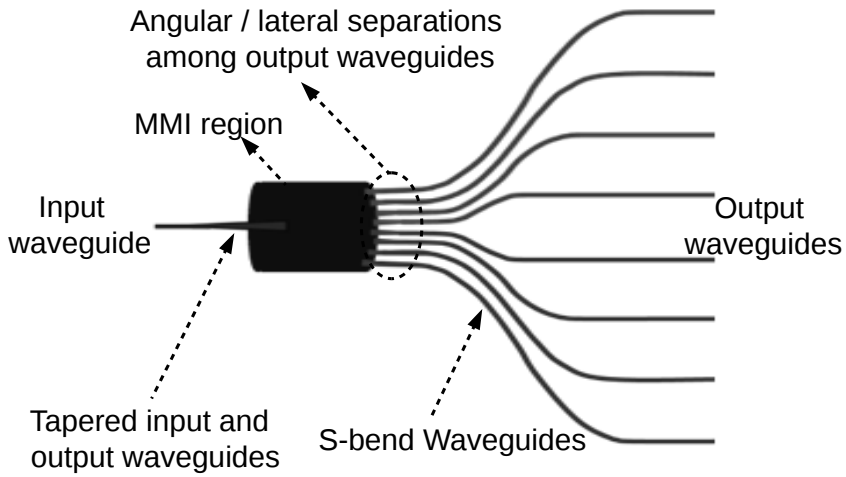


Figure 2.2: Proposed scheme of the 1×8 power splitter

1. single-mode conditions of input/output waveguides,
2. dimensions of MMI region,
3. adiabatic tapering of input/output waveguides,
4. angular/lateral separations among output waveguides and
5. S-bend design parameters.

While optimizing the parameters, care has been taken to achieve compact, lower excess loss, uniform power splitting, wavelength/polarization independencies and compatibility to pigtail with standard single-mode fiber.

Input and Output Waveguides

Input/output waveguides are designed by considering single mode guidance at $\lambda \sim 1550$ nm and optimum size of the guided mode in the waveguide. SOI based large

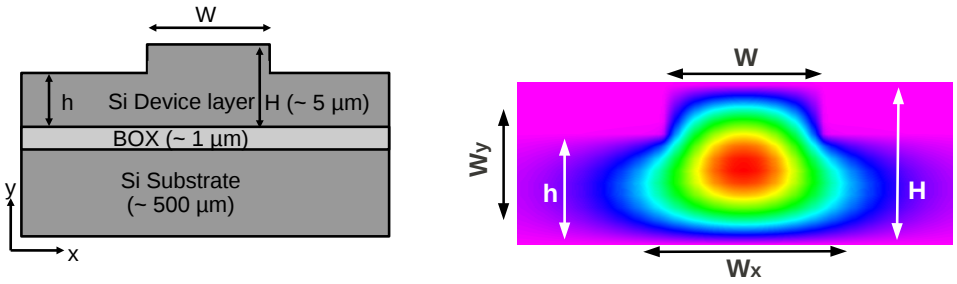


Figure 2.3: (a) Scheme of the cross sectional view of input/output rib waveguide structures in SOI platform, (b) fundamental mode profile (at 1550 nm) of a typical LCRW structure from BPM simulation (Figure aspect ratio is not to scale).

cross-sectional rib waveguide (LCRW) structures (see Fig. 2.3(a)) are considered for the proposed device, as they exibit relatively lower polarization dependent losses (due to less birefringence) and lower dispersive losses (due to less wavelength dependent group index variation). Besides, the fundamental mode sizes of LCRW structures ($\approx$ 7 $\mu m \times$ 4 μm) are comparable to the mode field diameter of the standard single mode fiber ($\approx$ 9.5 μm), and thus the fiber - waveguide coupling loss (due to the mismatch of mode sizes) can be reduced. Single mode guidance at larger cross section can be obtained, if the waveguide parameters like rib width (W), rib height (H) and slab height (h) satisfy the Soref's single mode condition [30].

$$\begin{aligned} \frac{W}{H} &\leq 0.3 + \frac{r}{\sqrt{1-r^2}} \\ r = \frac{h}{H} &\geq 0.5. \end{aligned} \tag{2.9}$$

The single mode waveguide dimensions are carefully chosen from [22], wherein detailed experimental study on various parameters of single mode straight and bend waveguides were carried out. The results of [22] shows that, vertical mode size is almost constant with respect to r for $2.5\mu m \leq W \leq 6\ \mu m$, and lateral mode size is larger for smaller waveguide width W and/or for higher values of r, due to less confinement

of the guided mode. It has also been reported that, coupling loss of $\leq$ 2 dB can be obtained for $r \geq$ 0.7 and 4 $\mu m \leq W \leq$ 6 μm and waveguide scattering loss of $\leq 1dB$ can be obtained for $r \geq$ 0.6 and 5 $\mu m \leq W \leq$ 6 μm. Moreover, for $W =$ 5.5 μm and $r =$ 0.7, lateral size of the fundamental mode is $\approx$ 7 μm, which is nearly comparable to fiber mode size and thus we can expect lower coupling loss at these parameters [22]. Based on these results, for the input/output single mode waveguides, width $W =$ 5.5 μm and $r =$ 0.7 (slab height h = 3.2 μm), have been considered for the present work.

MMI Region

Multimode interference region has been designed in such that we get distinct eight images of the input field. The following controlling parameters are considered critically in designing the device:

1) input waveguide width
2) photolithographic limitation
3) image resolution
4) uniform power distribution among eight output ports.

LCRW based single mode input/output waveguide of width W = 5.5 μm and slab height h = 3.2 μm has been considered. Minimum feature size we can obtain from photolithography system of our Laboratory is $\sim$ 2 μm. If we incorporate this limitation while designing the width of MMI region W_{MMI}, we need atleast 58 μm (= 8 $\times$ W + 7 $\times$ G; input waveguide width W = 5.5 μm; minimum separation among output waveguides when emerging out of MMI region G = 2 μm) to construct eight single mode waveguides at the end of MMI region. In order to reduce the overlap of tails corresponding to the modal fields of the self images and by considering the practical issues in fabrication (especially while developing PPR in photolithography), seperation G has been conveniently chosen as 3 μm. The width of MMI region have been further extended on both sides (W_{tol}) by 0.5 μm in order to account the fabrication tolerance. At this point, W_{MMI} = 66 μm (= 8 $\times$ 5.5 μm + 7 $\times$ 3 μm + 2 $\times$ 0.5 μm) has been considered. Initially, the length of the MMI region (L_{MMI}) has been considered according to equation

(2.8). With the device design parameters mentioned above, BPM simulations had been carried out, to obtain eight images.

It has been observed that the images formed at output side of MMI region were, not distinct enough and overlap of images were still exists. Intensity distribution in MMI region at this stage is as shown in Fig. 2.6. This will increase the excess loss and nonuniformity in power distribution among output waveguides. The unfavourable image formation can be avoided if we could control the number of modes excited in the MMI region, and upon further reducing the overlap of images by increasing the separation among images formed. So, the input waveguide has been added with an waveguide with tapered width (W_{it}) at the input side of MMI region as shown in Fig. 2.4.

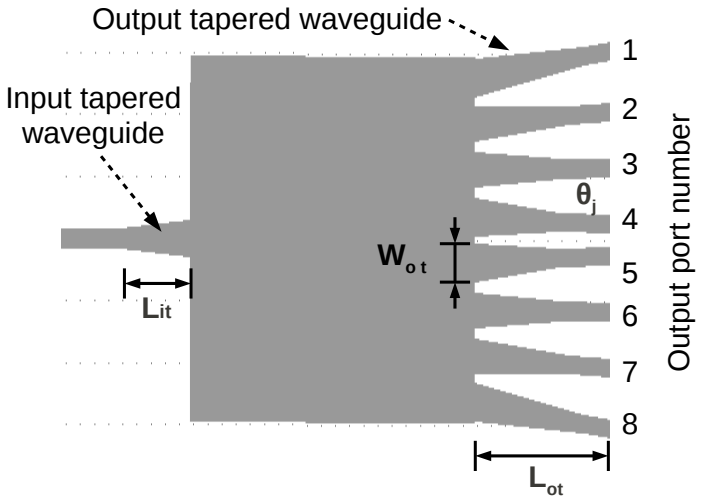


Figure 2.4: Scheme of the tapered waveguides along with the controllable design parameters.

Image resolution has been observed by varying W_{it} from 5.5 μm to 14 μm, and at the same time W_{MMI} has been chosen such that it can accommodate eight output images at the end of MMI region with image $(1/e)$ width W_{it}. In order to achieve this, W_{MMI} has been chosen according to the equation,

$$W_{MMI} = N \times W_{it} + (N-1) \times G + W_{tol}, \tag{2.10}$$

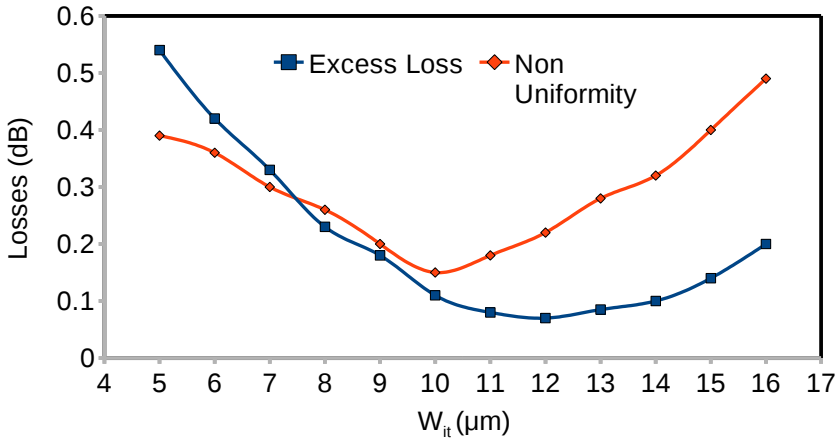


Figure 2.5: BPM simulation results of the excess loss and non-uniformity variation w.r.t. the input tapered waveguide width W_{it}

where number of output ports N = 8, separation among the output waveguides emerging outof MMI region G = 3 μm and fabrication tolerance width $W_{tol} = 1$ μm has been considered to get eight images of the excited input field of width W_{it}. Eight number of tapered waveguides with acceptance width $W_{ot} = W_{it} + 1$ were also connected at the output side of the MMI region and end up with a waveguide of width 5.5 μm. In order to collect the light from the images efficiently and to further decouple the tails of the modal fields of the images, W_{ot} has been considered as 12 μm. Throughout the design so far, L_{MMI} has been considered according to the equation (2.8). L_{it} has been considered 1000 μm to allow adiabatic mode expansion from input tapered waveguide to MMI region. BPM simulations have been then carried out to study excess loss and non-uniformity of output power distribution from the device. The simulation results show that the excess loss and non-uniformity were not as expected for all the possible variations of MMI region.

But, when L_{MMI} has been increased slightly (δl) in BPM simulation the excess loss got reduced and relatively better image resolution were obtained. In this way, while W_{it} has been optimized as 11 μm, W_{MMI} and L_{MMI} also have been optimized as 118 μm and 4006 μm respectively by BPM simulation. At this point even though excess loss has been reduced, the non-uniformity were still not as expected. This problem is due to the evanescent coupling of fields among output waveguides.

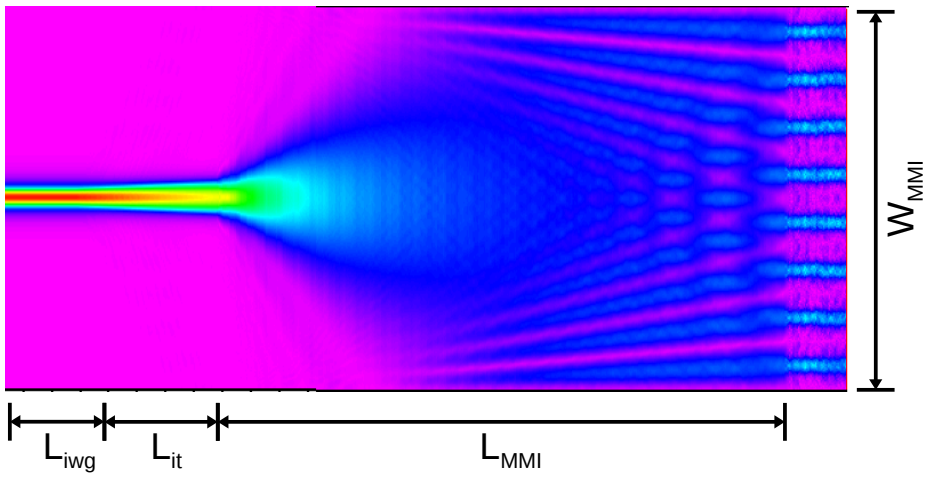


Figure 2.6: Intensity distribution in MMI region of 1 x 8 power splitter (before optimization of output tapered waveguides), shows the formation of eight clear images obtained at $W_{MMI} = 118\mu m$; $L_{MMI} = 4006\mu m$.

Output Tapered Waveguides

Coupled mode theory analysis for the interaction among eight output waveguides can be developed and one can find out the output waveguide parameters to control the non-uniformity. But as it is very tedious process to form atleast eight coupled mode equations and solve them numerically. Instead, BPM simulation results have been directly utilized to optimize the output waveguide parameters, so that we get minimum non-uniformity and excess loss. The output waveguides were tapered in width, stating from $W_{ot} = W_{it}$ at the end of MMI region to waveguide width of 5.5 μm, for a length of tapered waveguide $L_{ot} = 1000\mu m$. By varying the angle between each output waveguides, the evanescent field coupling among output waveguides can be controlled and thus output power uniformity can be improved. So, the angle between output waveguides were tailored until we get better uniformity and lower excess loss.

S-Bend Waveguides

S-bend waveguide structures are required to keep the output waveguides at 250 μm apart. This is due to the reason that, the standard single mode fiber has a diameter of 125 μm. So either side of the fiber it is a standard custom to keep the output waveguide separation at 250 μm. Scheme of final structure of the device with S-bend structures are

shown in Fig. 2.2. S-bend structures can be constructed with two arcs with corresponding radius of curvatures and then can be connected with straight waveguides, as shown in Fig. 2.7. Transition loss occurs at the junction of straight and S-bend waveguides, as

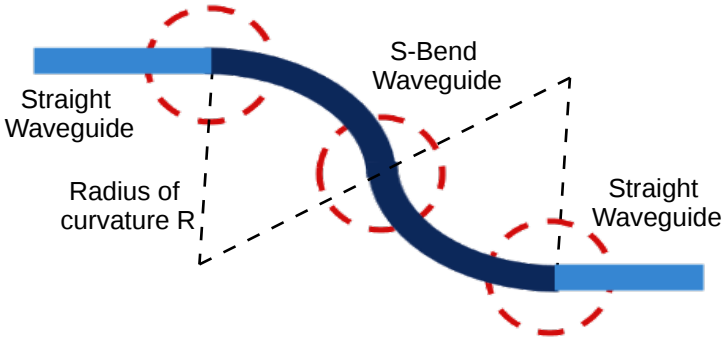


Figure 2.7: S-Bend waveguide has been constructed with two arc structure as shown. Encircled regions shows the connecting regions of these waveguides.

there is mode mismatch between them. Shifting of modes towards the outer curvature of the bend gives radiation loss. In order to achieve 250 μm separation among eight output waveguides, S-bends of different arc radius has been constructed and the excess loss and non uniformity of the devices have been studied, and the corresponding plots are shown in Fig. 2.8. From this analysis, radius of curvature R has been comfortably considered as 45 mm for both the arcs. With this optimized S-bend parameters, calculated transition losses at straight to S-bend regions and from S-bend to straight waveguide regions are shown in Fig. 2.9

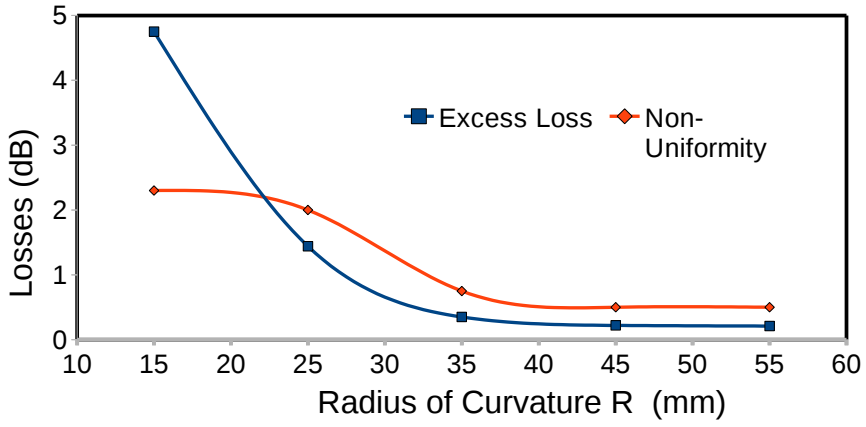


Figure 2.8: BPM simulation results of excess loss and output power non uniformity w.r.t the radius of curvature of S-Bend waveguides at 1550 nm

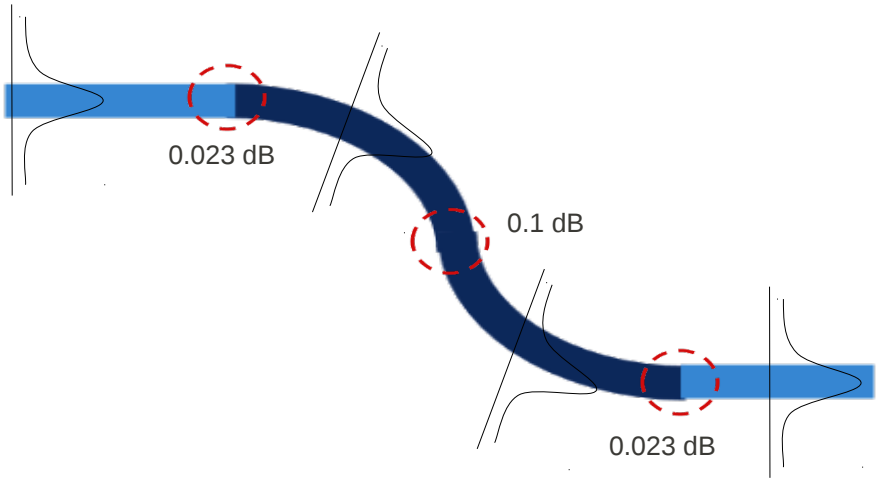


Figure 2.9: S-Bend waveguide along with computed mode mismatch loss at various transision points.

2.3 Simulation Results

With the optimized parameters as discussed above, BPM simulation has been carried out to investigate the transmission characteristics in terms of nonuniformity, insertion and excess loss. For the excitation at input waveguide with TE and TM mode, the transmission characteristics obtained from simulation are as shown in Fig. 2.10. The excess

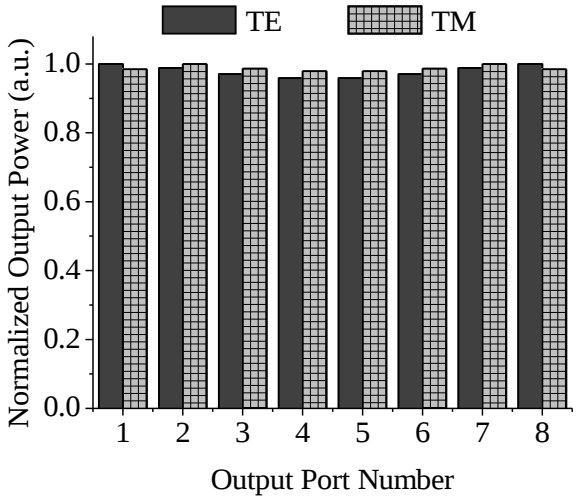


Figure 2.10: Transmission characteristics for TE and TM polarization at operating wavelength λ = 1550 nm

loss (ignoring scattering losses) of a 1 $\times$ 8 power splitter designed (at λ= 1550 nm) with above mentioned optimized parameters is estimated to be 0.2 dB. The normal-

ized transmitted powers at eight output ports have been shown in Fig. 2.10 for both TE and TM polarizations. The BPM simulation results clearly show that the power distribution is almost uniform (non uniformity 0.12 dB) due to the excited multimode interference effect at the end of the FPR region. Power distribution among the output waveguides are slightly polarization dependent (0.16 dB). With the optimized design parameters (Table 2.1) the device has been fabricated in SOI platform as discussed in Chapter 3.

Table 2.1: Optimized device parameters

Parameter	Values
L_{MMI}	4006 μm
W_{MMI}	118 μm
W_{it}	11-12 μm
W_{ot}	12 μm
L_{it}	1000 μm
L_{ot}	1 1200 - 1500 μm
R	45 mm

SUMMARY

In this chapter, power splitter design parameters have been optimized considering different losses. To prove the simulation results, 1 $\times$ 8 power splitter with these optimized parameters have been fabricated and characterized. The details of fabrication procedures are discussed in next chapter.

CHAPTER 3

FABRICATION AND CHARACTERIZATION

The optical 1 $\times$ 8 power splitters were fabricated on SOI substrate (Si device layer: 5 μm, BOX: 1 μm, substrate: 500 μm) using the optimized design parameters as discussed in Chapter 2. Fabrication process parameters were optimized step by step with the feedback results obtained from many fabrication attempts and optical characterization results. Details of the fabrication process flow, which includes the mask layout design, fabrication of the photo mask, pattern transfer by photolithography, reactive ion etching of Si and polishing of the waveguide end facets of the fabricated devices are described in this chapter. Methods and results of optical characterization of the fabricated devices in terms of excess loss, output power uniformity, polarization and wavelength dependency are then discussed.

3.1 Mask Design and Fabrication

A photo-mask layout has been designed and subsequently the pattern was transferred on a Cr-coated quartz plate. We have used RSoft CAD tool to design the photomask layout. The mask layout consists of five sets of guiding structures, with each set comprised of a power splitter, a straight waveguide, and a S-bend waveguide structures (see Fig.3.1). These additional waveguide structures (straight and S-bend) were incorporated for the experimental investigation of various loss parameters. The layout is then directly replicated with a PPR (AZP1350, thickness - 50 nm) pattern on the surface of a Cr-coated ($\sim$500 nm) quartz mask plate (4"X4") using a laser writing system (DWL-66, Heidelberg Instruments). During mask writing, a direct laser beam ($\lambda \sim 442$ nm) was used for exposing the photoresist layer according to the designed mask layout. Mask plate was then developed using developer solution prepared in our laboratory (1 g of NaOH pellets in 250 ml of De-Ionized (DI) water for 2.5 minutes). After this step, the exposed Cr regions were etched-out with a Cr-etchant solution (mixture of 16 g of ceric

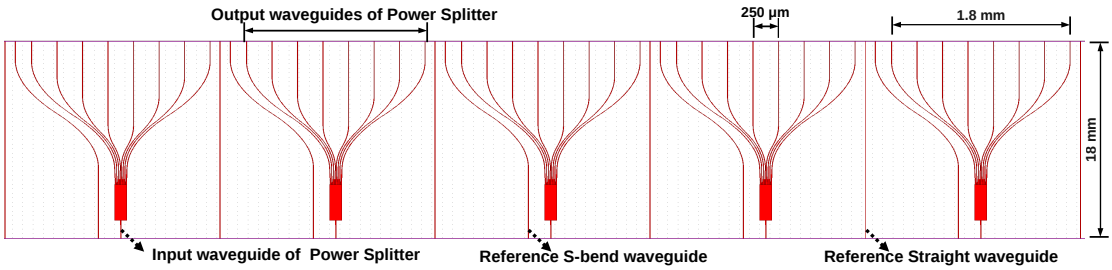


Figure 3.1: Photomask layout used for the fabrication of power splitters and reference straight and S-bend waveguide structures. (see text for details).

ammonium nitrate in 57 ml of DI water and 6 ml of CH_3COOH in 69 ml of DI water). In order to get the final photomask plate, photoresist on top of the remaining Cr region of the device pattern was then stripped off using acetone.

3.2 Device Fabrication

Each step of device fabrication process, corresponding issues and optimization of fabrication parameters are detailed here (see Fig.3.2).

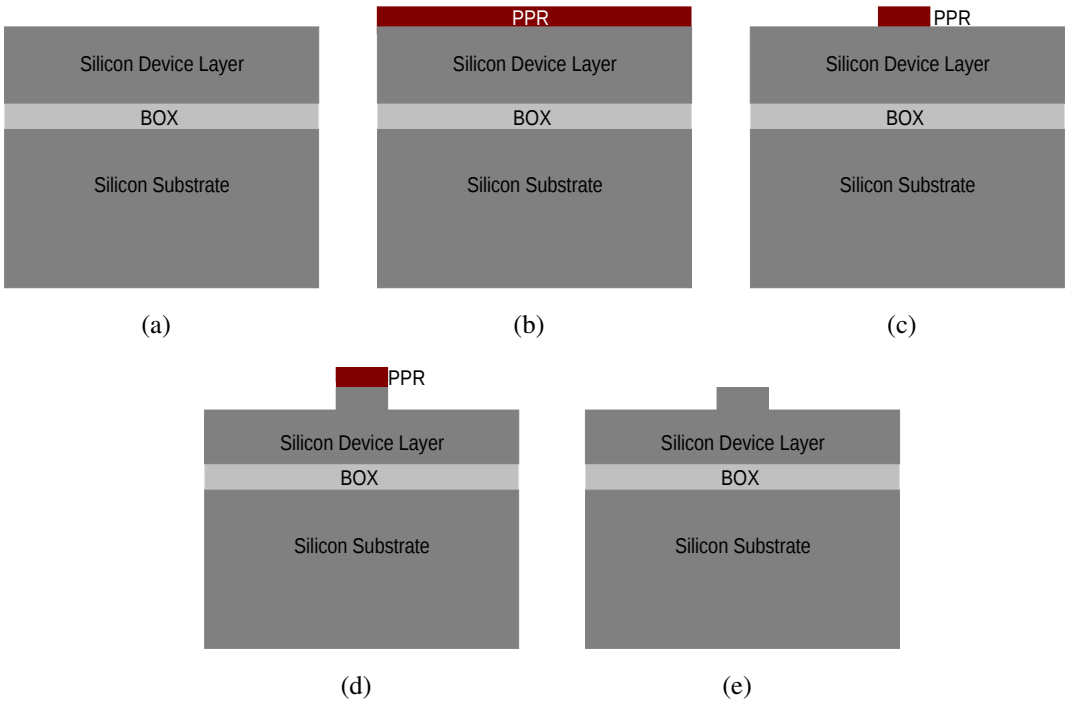


Figure 3.2: Scheme of fabrication process flow while pattern transfer and RIE: (a) cross sectional view of SOI wafer (b) after spin coating of PPR (c) after pattern transfer by photolithography process (d) after RIE process and before strip off the PPR (e) after RIE process and after striped off the PPR.

SOI Wafer Specifications

Optical and electronic grade SOI wafer (of Si device layer: 5 μm; buried oxide layer (BOX): 1 μm; Si substrate: 500 μm) procured from Ultrasil Inc. USA, has been used to fabricate the devices. The cross sectional view of a SOI wafer is shown in Fig.3.2(a). Specifications of the SOI wafers used for this device fabrication are listed in Table 3.1.

Table 3.1: SOI Wafer Specifications

Manufacturer	Ultrasil Inc., USA
Resistivity of device layer	> 5000 $\Omega - cm$
Free carrier concentration	< $10^{12} cm^{-3}$
Wafer Diameter	4"
Wafer Thickness	500 μm
Buried oxide layer	1 μm $\pm$ 0.05 μm
Top device layer	5 μm $\pm$ 0.5 μm
Lattice orientation	<100> $\pm$ 0.5 deg

Wafer Cleaning

First and important step of fabrication is cleaning the substrate to remove the organic and inorganic impurities residing on the substrate. At first, ultrasonic agitation of substrate with TCE was carried out for 2 minutes followed by heating (at 70 ^{o}C) the same for 3 minutes. Afterwards, the substrate was similarly treated with acetone to dissolve the residue of TCE and remaining organic impurities, followed by rinsing in DI water and then dried using nitrogen air. Then the substrate were heated in concentrated nitric acid for about 4 minutes (or until fumes come out) to form a native oxide layer. This oxide layer was then removed by dipping the sample in diluted HF solution (5:1::H_2O:HF) followed by rinse in DI water and then dried using nitrogen air. This leads to the fresh in-situ cleaned Si surface.

3.2.1 Pattern Transfer by Lithography

In order to transfer the pattern from the mask to the SOI sample, photolithography technique was used and it is the most important stage in fabrication of this device. The

following sequence of steps have been carried out on the substrate during the photolithography process:

(1) Spin coating of positive photoresist (PPR)

(2) Pre-baking

(3) UV exposure through photomask

(4) Developing the device pattern

(5) Post-baking.

A thin ($\sim$ 1 μm) and uniform layer of PPR (S-1813 G2) was obtained by spin-coating the PPR on the substrate for 45 s at 5000 rpm with an acceleration of 600 rpm/s. For above mentioned PPR spin coating parameters, the pre-baking time of 23 minutes (at 80 ^{o}C) was practically observed as optimum value. The pre-baked substrate was then exposed to UV light (λ $\sim$ 365 nm, intensity = 300 mW/cm^2) for 125 s, through the photomask using contact photolithography technique (MA/BA 6, Karl Suss Mask Aligner). The exposed region of photoresist become soften and was developed by using NaOH developer solution ($\sim$1 g of NaOH in 200 ml of DI water) followed by DI water rinse. The sample was then post-baked for 35 minutes at 120 ^{o}C, to harden the photoresist pattern. This hardend PPR pattern was used as mask for RIE process. The PPR patterns and the corrsponding dimensions were cross checked by using optical microscope. The above mentioned lithographic process steps are shown schematically in Fig.3.2(a)-(c).

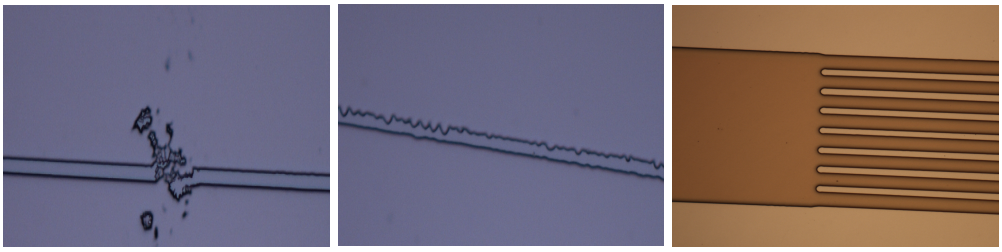
Optimization of Various Process Parameters

It has to be noted that the above mentioned optimized process parameters were obtained over repeated and modified attempts on different substrates at different times. When the PPR was spin-coated on the substrate at 6000 rpm (with 45 s and an acceleration of 600 rpm/s), followed by UV exposure (for 80 s), upon developing, the PPR pattern on the substrate was obtained with damages at certain regions (see Fig.3.3(a)). This is due to the nonuniform and very thin layer of PPR pattern, which in turn causes lower rigidity of the PPR pattern on Si surface. Moreover, very thin layer of PPR leads to

faster developing and hence less controllability over the pattern dimensions. In order to overcome these issues, thicker PPR layer need to be used.

To get thick layer of PPR on the substrate, we spin-coated at 4000 rpm (with 45 s and an acceleration of 600 rpm/s). After UV exposure (for 120 s) and developing, the PPR patterns obtained on the substrate were not smooth along the boundaries (see Fig.3.3(b)). This type of issue is technically known as reflective notches, which occurs due to the highly reflective surface of Si substrate and heavy dose of UV exposure. Since the PPR layer was thicker, heavy dose of UV exposure was unavoidable.

When the PPR was spin coated at 5000 rpm (with 45 s and an acceleration of 600 rpm/s), the PPR thickness was highly uniform over the substrate and found to be optimum (1 μm). After UV exposure (for 120 s) and developing ($\sim$ 30-40 s), the PPR patterns obtained on the substrate were smooth along the boundaries and could control over the pattern dimensions (see Fig.3.3(c)).



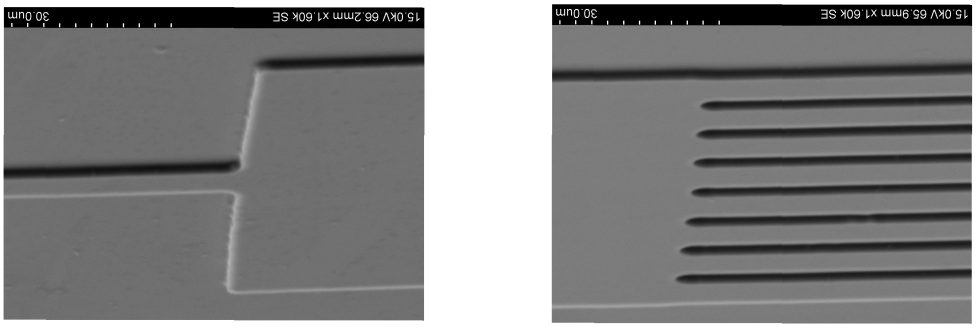
(a) (b) (c)

Figure 3.3: Microscopic images of the PPR patterns obtained for various PPR spin coating rpm (a) at 6000 rpm, defect occured due to less rigidity of PPR on substrate, (b) at 4000 rpm, smoothness of boundaries got affected due to heavy UV dosage and reflecting surface of Si substrate, (c) MMI - output waveguide region of one of the best fabricated devices just after the PPR was developed and subsequently post baked at 5000 rpm shows PPR patterns with good control over pattern dimension could be obtained.

3.2.2 Reactive Ion Etching

After the photolithography process, PPR pattern was used as a mask for reactive ion etching (RIE) process - this is to realize Si rib structures. The RIE process was optimized with a conventional RIE system (RF source frequency = 13.56 MHz), using

fluorine (SF_6+Ar) chemistry (Plasmalab 80 Plus, Oxford Plasma Technologies). The etching chemistry and ambiance were carefully chosen so that the fabricated rib waveguide structures have uniform widths, vertical sidewalls and smooth surface/sidewalls. The optimized RIE parameters are: gas composition of SF_6 : Ar :: 20 : 20 sccm, RF power = 150 W, chamber pressure = 200 mTorr, substrate temperature = 20 ^oC. With these parameters, the Si etch rate was controlled to the value as low as $\sim$320 nm/minute and corresponding rms value of surface roughness was found to be $\sim$ 25 nm. Silicon etching has been carried out for 308 s to achieve the optimized etch depth of 1.6 μm as discussed in Chapter 2. After RIE process, PPR was stripped off by heating the sample



(a) (b)

Figure 3.4: SEM picture of a portion of the fabricated 1$\times$ 8 power splitter device: (a) junction of input waveguide - MMI region, (b) region where output waveguides emerging out of MMI region.

with acetone. A scheme of cross sectional view of a sample before and after RIE process are shown in Fig.3.2(e)-(f). The surface profiler measurement shows the average etch depth is around $\approx$ 1.6 μm. The SEM images of portions of a fabricated 1$\times$ 8 power splitter are shown in Fig.3.4.

3.2.3 Dicing and Polishing

Following the RIE process, the input and output sides of the samples were diced along the direction perpendicular to waveguide axis. Since the optical characterizations of the devices require optically flat end facets for both input and output waveguides, the end facets were polished (mechanically) with the help of polimer sheets coated with diamond grains of different sizes. The polishing was done step-by-step with different

polimer sheets having grain sizes of 30 μm, 15 μm, 9 μm, 6 μm, 3 μm, 1 μm, 0.5 μm and 0.1 μm, to gradually reduce the roughness of the waveguide end facets. Microscopic and SEM images of end-facets of the waveguides after polishing are shown in Fig.3.5.

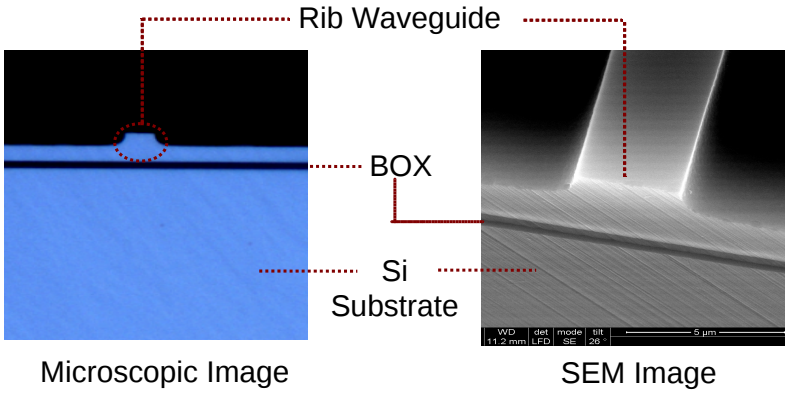


Figure 3.5: Microscopic and SEM images: cross sectional view of the optically polished end facet of one of the input waveguide of the fabricated 1$\times$ 8 power splitter.

Challenges

In order to reduce the Fresnel loss, we require input and output waveguides with perpendicular end facets with respect to the waveguide axis. Moreover, while polishing, mechanically removed Si particles and/or any damage in the polishing sheet affects the quality of the end facet polishing. It was a time consuming job with the existing polishing machine in order to polish the sample perpendicular to the waveguide axis and with less damages. Polishing couldn't be achieved efficiently in the sample S4 and S6, due to tilted and imperfect end facet polishing respectively (the available length of the sample was short for polishing further).

Fabricated Samples and their Nomenclature

In total, 6 samples (S1 to S6), each containing 3 or 4 power splitter devices along with straight and S-bend waveguides were fabricated on different samples at different times. The fabricated devices are identified as SiDj, representing jth device of the ith sample. The process parameters for all these devices at various fabrication stages are given in

Table 3.2: Qualitative description of six fabricated samples which were systematically characterized.

Sample Number	Etch Depth [μm]	Comments
S1	~ 1.58	PPR patterns were not smooth after lithography, which propagated until RIE. Quality of polishing at end facets was not as expected.
S2	~ 1.61	PPR patterns were not smooth after lithography, which propagated until RIE. Quality of polishing at end facets was not as expected.
S3	~ 1.6	PPR patterns were smooth. All end facets after polishing was much better with good waveguide cross sections.
S4	~ 1.61	Device S4D3 was mechanically damaged (by mistake). The sample was slightly tilted at the edges with respect to the waveguide axis and couldn't polish further due to short of sample length.
S5	~ 1.6	PPR patterns were smooth. All end facets after polishing was much better with good waveguide cross sections.
S6	~ 1.6	Polished end facets were damaged and couldn't polish further due to short of sample length.

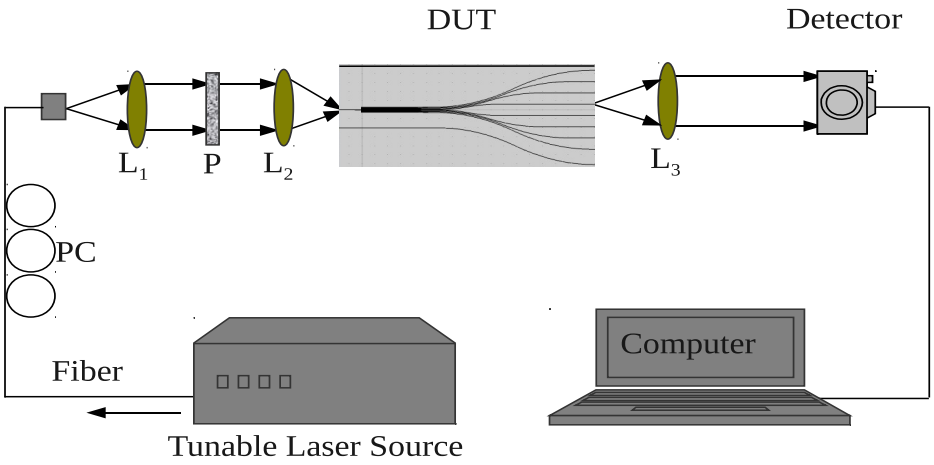
Table.3.2 with the appropriate comments. While fabricating the samples S1 and S2, the control over the lithography process to obtain smooth PPR pattern were difficult to achieve and this propagated until the RIE process. End facet polishing were also not so good in initial attempts. Reasons for the poor performance of the fabricated devices (S1 and S2) has been analyzed and the above mentioned problems has been reduced for the rest of the samples with hands on experience in the fabrication process.

3.3 Optical Characterization

All the fabricated 1×8 power splitters was optically characterized using end-fire characterization setup. Details of the experimental setup, results of optical characterization in terms of output power distribution, wavelength/polarization dependency and corresponding issues of fabricated power splitters are discussed in this section. Some of the best devices have been fiber pigtailed and subsequently packaged.

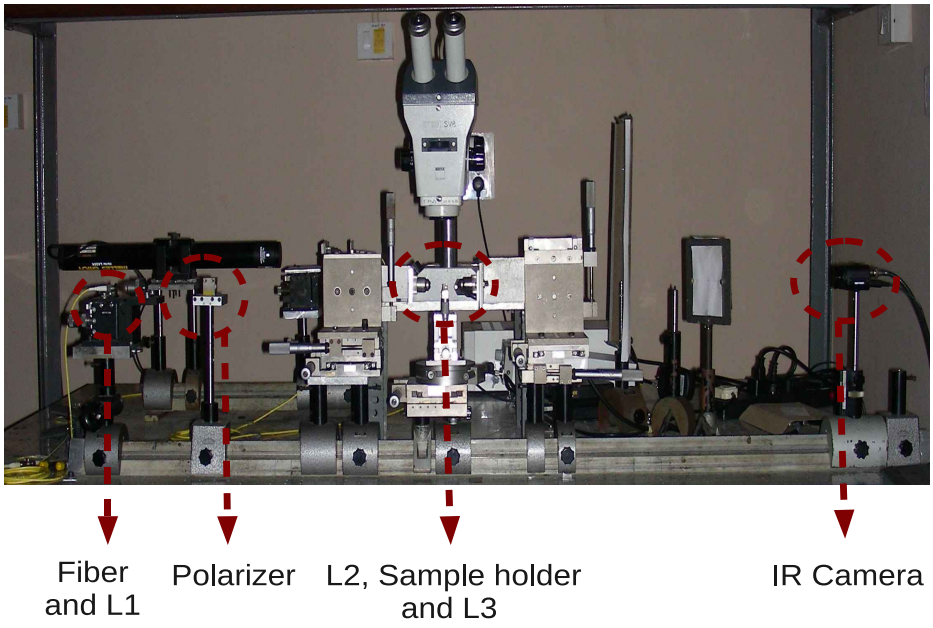
3.3.1 Experimental Setup

End-fire coupling setup (see Fig.3.6) developed in our lab, was used for optical characterization of the fabricated devices. Single mode fiber-coupled external cavity tunable (1510 nm < λ < 1600 nm) semiconductor laser (Santec: TSL-210V) with a maximum output power of 10 mW was used as light source for optical characterizations. Light from the LASER source is collimated using a 10x - objective lens (L_1), and then passed through a polarizer (TE/TM). This polarized light was focused to the input waveguide of the device using another 10x - objective lens. Output light from the device is then collected using 60x/40x objective lens (L_3). The light output from each of the output port can be obtained by changing the position of the output lens (L_3). The output power from each port was measured by the optical power meter system, placed after lens L_3, as shown in Fig.3.6. The photo detector (THORLABS: S132A) interconnected with the optical power meter used for the characterization is capable to detect the minimum power level of 1 nW. Guided mode profiles of the fabricated devices was obtained by imaging the near-field pattern of transmitted light onto the IR camera (SPIRICON:LBA300). To study the polarization dependencies, a combination of fiber-optic polarization controller (PC) and a Glan-Thompson TE / TM pass polarizer (P) was used.



DUT – Device Under Test, PC – Polarization controller,
L –Lens, P – Polarizer

(a)



(b)

Figure 3.6: (a) Scheme of the characterization setup (b) experimental setup for characterization of optical devices

3.3.2 Characterization Results

Characterization of Reference Straight and Bend Waveguides

The reference straight and bend waveguides (see Fig.3.1) were first characterized in terms of waveguide losses, bend induced losses, mode profiles and their polarization dependency. Fabry-Perot measurement technique was used for the estimation of waveguide propagation losses. At λ = 1550 nm, typical waveguide propagation losses for straight waveguide were found to be 1.5 dB/cm for TE polarization and 1.3 dB/cm for TM polarization (for waveguide width W = 5.5 μm and r = 0.7). Nearly polarization independent bend induced loss (average) of S-bend structures was estimated to be 0.5 dB for a bend radius of 45 mm. The guided mode profiles of the fabricated waveguides have been obtained by imaging the near-field pattern of transmitted light onto the IR camera. Mode-profiles for TE-polarization and TM polarization at $\lambda \sim$ 1550 nm are shown in Fig.3.7.

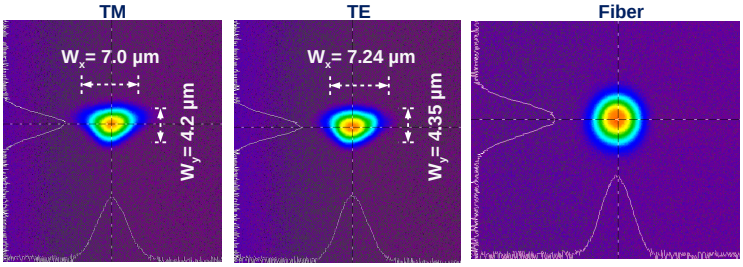


Figure 3.7: Mode profile measurement for TM, TE polarization of a reference straight waveguide fabricated in adjacent to the OPS 1/e width and 1/e height; and mode profile of standard single mode fiber

Typical mode-size was estimated to be $\simeq$ 7.24 μm $\times$ 4.35 μm for TE-pol and $\simeq$ 7.0 μm $\times$ 4.2 μm for TM-pol (at λ = 1550 nm) respectively. From the mode profile imaging (see Fig.3.7(a) and 3.7(b)) the single mode guidance is confirmed. It is evident from the Fig.3.7(c) that fiber and rib waveguides have different mode shapes and sizes which results in mode mismatch loss. However, the lateral size of the guided mode of the waveguides (width W = 5.5 μm and r = 0.7) is comparable to that of mode field diameter of the single-mode fiber ($\approx$ 9 μm). As a result, we can expect relatively lower coupling loss for large cross sectional rib waveguide structures compared to photonic

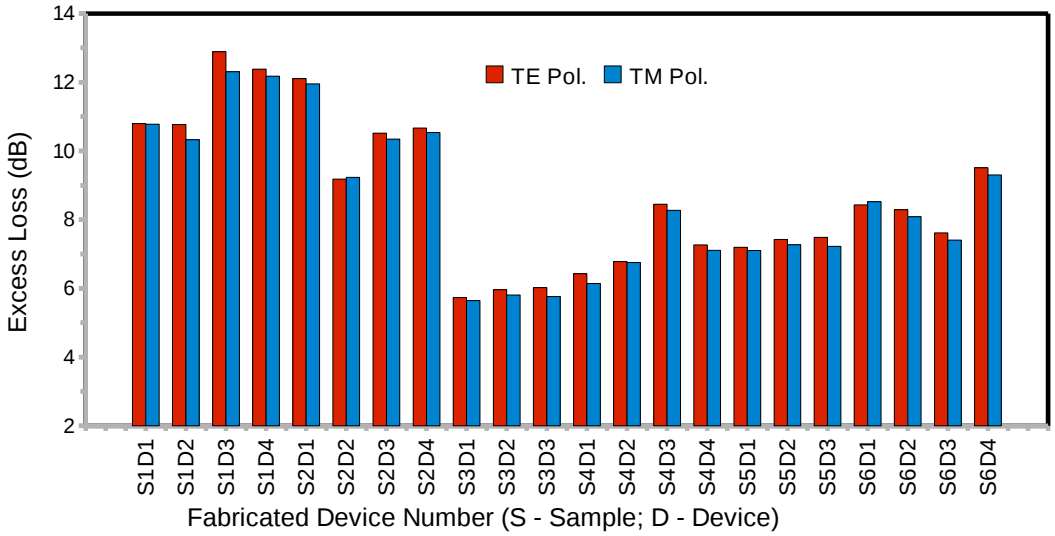


Figure 3.8: Excess loss for all the fabricated devices (at λ = 1550 nm).

wire waveguides.

Characterization of Power Splitter

For an input power of 6 mW (at λ = 1550 nm), the throughput powers from all eight output waveguides of all the devices were measured for both TE and TM polarizations. The corresponding excess loss and output power non-uniformity measurements are reported in Fig.3.8 and Fig.3.9 respectively. Based on the experimental results obtained from samples S1 and S2, fabrication process parameters were optimized for rest of the samples. The excess loss and output power non-uniformity are relatively low from the sample S3 onwards are evident from Fig.3.8 and 3.9 respectively. Lack of hands on experience in fabrication and imperfect polishing of the end facets are the causes for high non uniformity and excess loss in samples S1 and S2. Sample S3, S4 and S5 are relatively good samples in terms of low excess loss (see Fig.3.8) and uniformity in out-out power distribution (see Fig. 3.9). Excess loss of the device S4D3 is deviated from rest of the devices of sample S4 due to a mechanical damage. Output power distribution of sample S6 were affected by the end facet roughness and mechanical damages by the polishing. Due to the non availability of sufficient length, the sample S6 couldn't be polished further. From Fig.3.8, one can see that the polarization (TE/TM) dependency of excess loss and output power non-unifromity are very minimum.

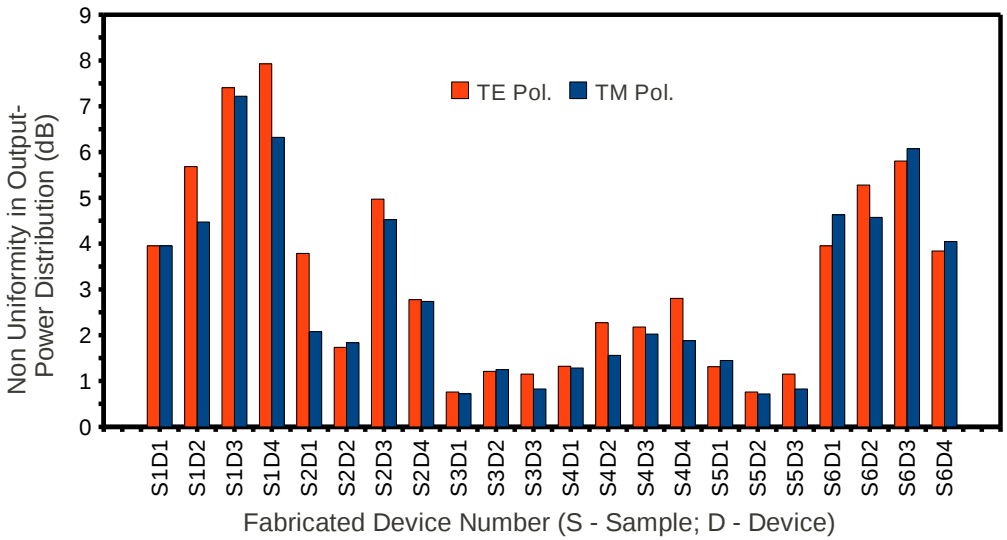


Figure 3.9: Output power non-uniformity among of all the fabricated devices (at λ = 1550 nm).

The throughput power from four best devices of two different samples (S3D1, S3D3, S5D2 and S5D3) are reported in Fig.3.10 for TE polarization and in Fig.3.11 for TM polarization respectively. By comparing the experimentally measured output power for TM-polarized light, we have noted the lowest (highest) excess loss of 6.5 dB (7.6 dB) and the minimum (maximum) insertion loss of 15.3 dB (17.3 dB). The throughput non-uniformity in the best device has been estimated to be 0.6 dB for TM polarization. Typical polarization dependent loss, which has been calculated by the difference of excess loss in TM and TE polarization (in dB scale) is $\sim$ 0.23 dB. We have also observed

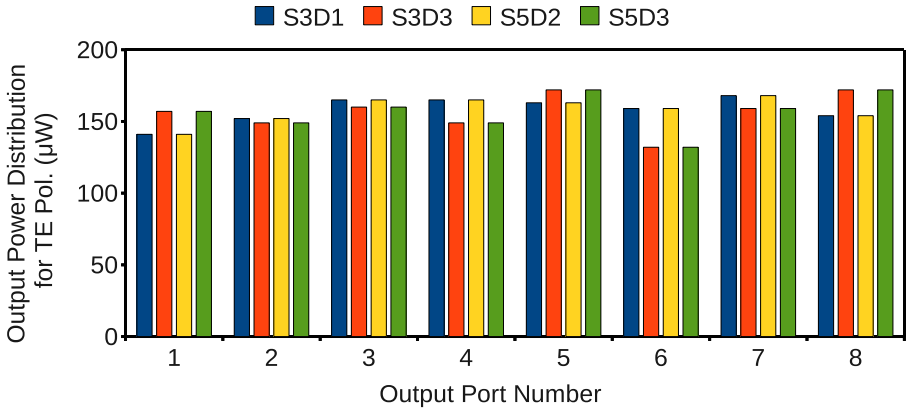


Figure 3.10: Output power distribution for four best devices of different samples for TE polarization (at λ = 1550 nm)

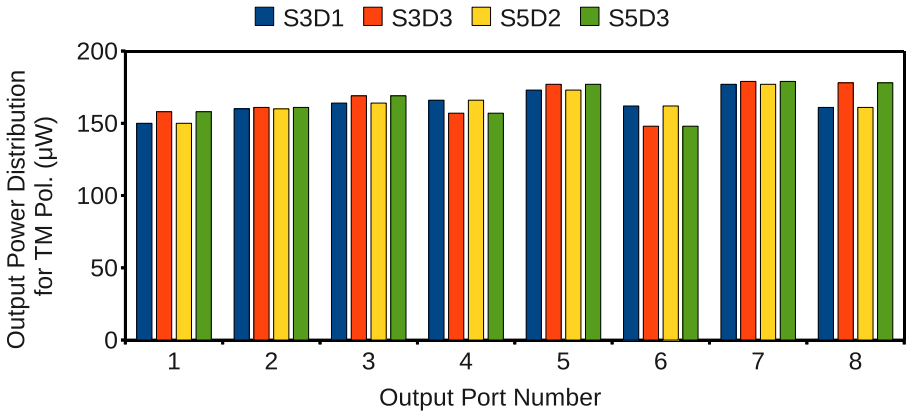


Figure 3.11: Output power distribution for four best devices of different samples for TM polarization (at λ = 1550 nm)

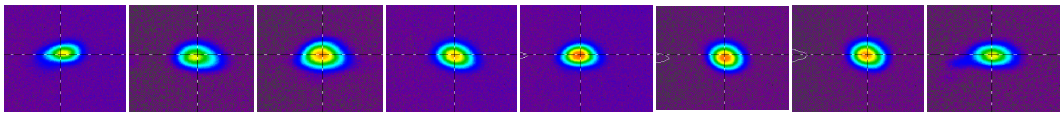


Figure 3.12: Mode profile from all the output ports of the device S3D1 (at λ = 1550 nm)

that the throughput power in any of the output port is nearly independent of wavelength of the input light from 1520 nm to 1600 nm. Wavelength dependancy of output power response of one of the best devices(S3D1) is shown in Fig.3.13. It has also been observed that almost similar results were obtained for both TM and TE polarization. From these plots we can observe that the experimental behavior is closely matching with the simulated one but difference in values may be attributed to variations in actual waveguide dimensions generated during various process steps and errors in characterization measurements.

Average excess loss and non uniformity of the devices has been calculated per sample to study the fabrication yield (see Fig.3.14). With the optimization of fabrication process based on the results obtained through many fabrication and characterization, the excess loss and non uniformity per sample has been gradually reduced in samples S3, S4 and S5. Considering these three samples as effective samples, the average excess loss and non uniformity has been obtained as 6.5 dB and 1.3 dB respectively. When the 1×8 power splitter is fabricated with the above mentioned design and fabrication parameters in industry environment, the losses can be significantly reduced.

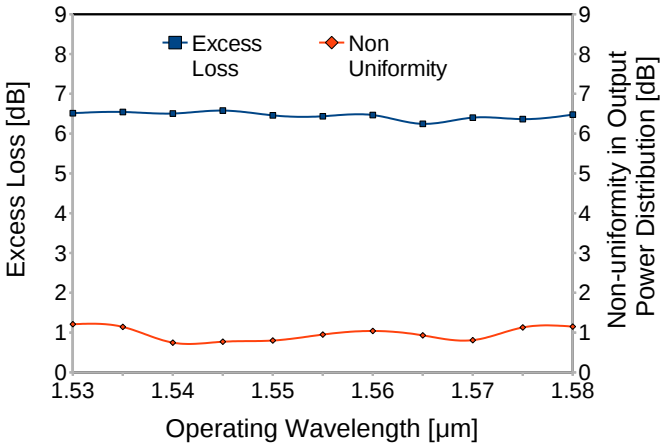


Figure 3.13: Wavelength dependency of output power distribution of the device S5D2.

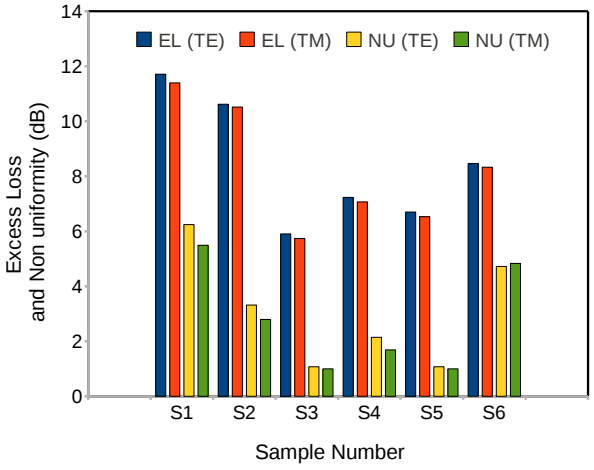


Figure 3.14: Average excess loss and output power non-uniformity of the fabricated samples (at λ = 1550 nm).

Conclusions

A set of 1 $\times$ 8 optical power splitter devices were fabricated in SOI platform. Fabrication parameters were optimized based on repeated fabrication results and some optical characterization results. Optical characterization of all the fabricated devices have been carried out and reported in terms of excess loss, insertion loss, non uniformity in output power distribution and wavelength/polarization dependency. The consistency of characterization results with relatively minimal loss were observed from the experimental power measurements of samples S3, S4 and S5. For TM-polarized light, we obtained the typical excess loss of 7.6 dB, insertion loss of 16 dB and non-uniformity in output power distribution of 0.7 dB. In all the devices, the polarization/wavelength dependency is almost negligible.

CHAPTER 4

Packaging and Testing

As discussed earlier, the power splitters have major applications in fiber based passive/active optical networks. Therefore, they need to be fiber pigtailed and packaged suitably. This Chapter describes the details of fiber-pigtailing, packaging and the performance testing of our SOI based integrated optical 1×8 power splitters.

4.1 Fiber Pigtailing and Packaging

We have chosen two of our best devices (S3D1 and S5D2) for fiber pigtailing, packaging and testing. It is worth mentioning here that the fiber pigtailing and packaging was carried out in SAMEER, Mumbai, with the help of Dr. Anuj Bhatnagar and his team. An 8-channel fiber-array ribbon and a 1-channel fiber assembled in V-groove(s) platforms were used for pigtailing the output and input waveguides, respectively (with center-to-center channel separation of 250 μm) and the other end(s) of the fibers were pre-attached with FC/PC connectors at each of the ports. A typical cross section of one such fiber V-grove assembly is shown schematically in Fig.4.1. The assembly is tightly held by gluing it with a pyrex lid from top. The end-facets of fiber-V-grove assembly are polished for efficient light (butt-) coupling from fiber to polished waveguide end-facets. Since, the thickness of the V-groove assembly is $\approx$1 mm, it is recommended to have an equivalent handle wafer thickness of integrated optical chip, in order to achieve better mechanical support during adhesion. As mentioned in Chapter 3, the power splitters were fabricated in commercially acquired optical grade SOI wafers having a handle wafer thickness of 500 μm. Hence, these wafers were at first glued to another dummy substrate (silicon wafer thickness 500 μm) using an epoxy adhesive (Araldite), to get $\approx$1 mm of handle wafer thickness (see Fig.4.2). Typically, such epoxy have a tendency to harden as soon as their polymer-resin and hardner were mixed together. In order to achieve a thin layer of this epoxy for sticking wafers, initially a small quantity ($\approx$ 1 ml)

of hardner was dissolved in acetone. Later, equal (or lesser) quantity of polymer-resin is mixed with the prepared solution and immediately applied using a paint-brush on top of the dummy substrate. The fabricated device sample are then carefully placed over this dummy substrate and left to dry for 12-14 hours. For proper sticking, the light metal weight should be placed evenly on top of the glued wafers. Care was taken to avoid the scratching of top device surface while putting under a metal weight. The end facets of the glued wafers were again polished with 3 μm, 1 μm, 0.5 μm and 0.1 μm diamond coated polishing sheets.

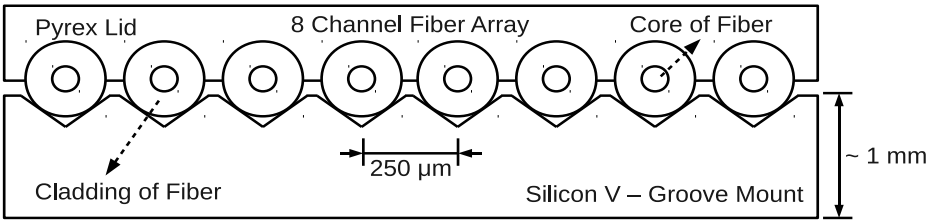


Figure 4.1: (a) Scheme of the cross-sectional view of fibers assembled in v-grooves (showing eight adjacent fibers separated by a distance of 250 μm.)

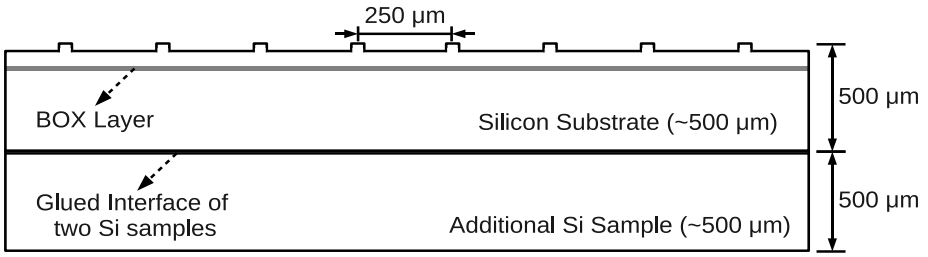


Figure 4.2: Scheme of the cross-section of fabricated chip showing the output waveguides separated by a distance of 250 μm. (Figure not to scale)

For initial alignment purpose, visible light was launched into the input waveguide through a butt-coupled 1-channel V-grooved fiber, and the output of the device was observed with a 5 - 10 $\times$ microscope objective and a photo detector. Once the alignment is done with the visible light, the splitter was tested by observing eight output images (at 1550 nm), with the help of a Agilent 81640A tunable laser. Fig.4.3 shows the eight output images captured by a CCD camera, when the splitter was tested at this wavelength.

Then, V-grooved 8-channel fiber-array ribbon (pre-attached with a FC/PC connector

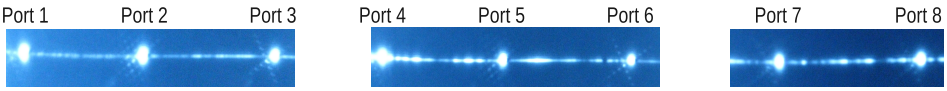


Figure 4.3: Photograph of images obtained from output ports of the fabricated 1x8 optical power splitter just before pigtailing with single mode fiber. (At this point of time the device was mounted in the pigtailing setup and light was launched into the input port of the device through the 1 - channel fiber).

on another end) were butt-coupled to the output ports of the device and the alignment was done such that to get maximum power output from the ports. When this alignment is done, the 1-channel (8-channel) fiber array ribbon was attached to the input (output) ports of the device with a UV-curable NOA-61 epoxy. Upon the completion of UV curing of the epoxy, even though the fiber is attached to the input/output ports of the device, for mechanical stability and isolation of the pigtailed device, it was kept in a packaging case and glued. Fig.4.4, displays a photograph of the pig-tailed 1×8 optical power splitter after fixing it within a proper packaging case (without the top cover). A top cover is kept on the packaging case and then it is also glued firmly on the wall of the packaging case. Completely packaged 1×8 optical splitter is shown in Fig.4.5, wherein FC/PC connectorized fiber channels can be used for input/output ports of the device.

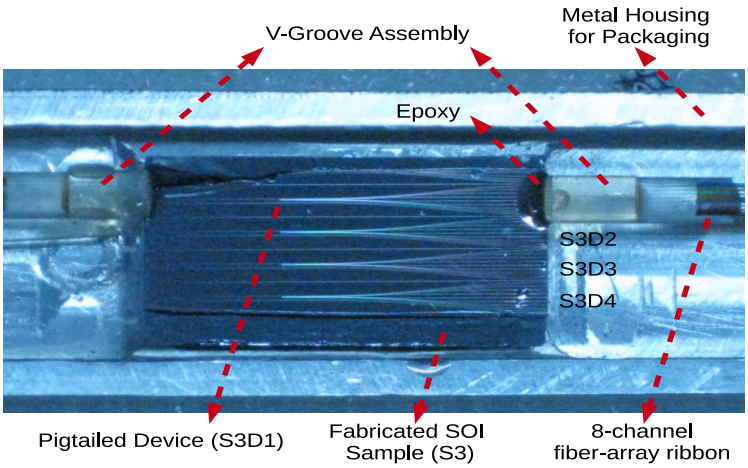


Figure 4.4: Photograph of the fiber pigtailed 1×8 power splitter (device S3D1).

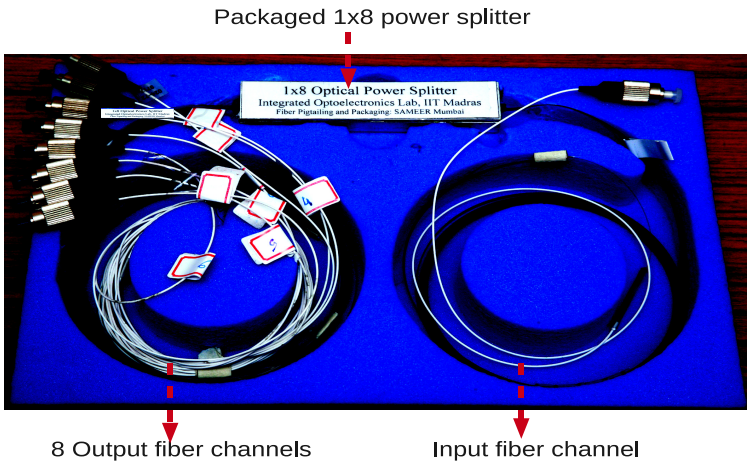


Figure 4.5: Photograph of the packaged 1×8 power splitter (device S3D1) with FC/PC connectorized fiber channels at input/output of the packaged device.

4.1.1 Device Testing

The packaged power splitter devices have been tested for their performance. A schematic of experimental setup used for testing of prototype device is shown in Fig.4.6. The throughput transmission characteristics of the two packaged devices are reported in Fig.4.7. It is evident that the non-uniformity ($\sim$ 4 dB) and excess loss ($\sim$ 16 dB) have been increased a lot after pigtailing. This degradation may be attributed to the mismatches of waveguide-to-fiber mode-sizes and transverse alignments during pigtailing. Difficulties in achieving smooth end facets of the input/output waveguides by mechanical polishing also could lead to the reduction in output power distribution. Besides, mechanical polishing of the end facets of the fiber which is fixed in the V-groove assembly is another main cause of the loss, because the Fresnel loss at end facet of fiber is very high (due to high index contrast and scattering of light).

Conclusions

Packaged devices showing the non-uniformity of $\sim$ 4 dB and excess loss of $\sim$ 16 dB. With a better polishing of waveguide/fiber end facets, with ideal pigtailing with proper alignments of fiber/output ports of the OPS, suitable anti-reflection coatings and appropriate index matching epoxy while fiber pigtailing, one can get low excess loss and

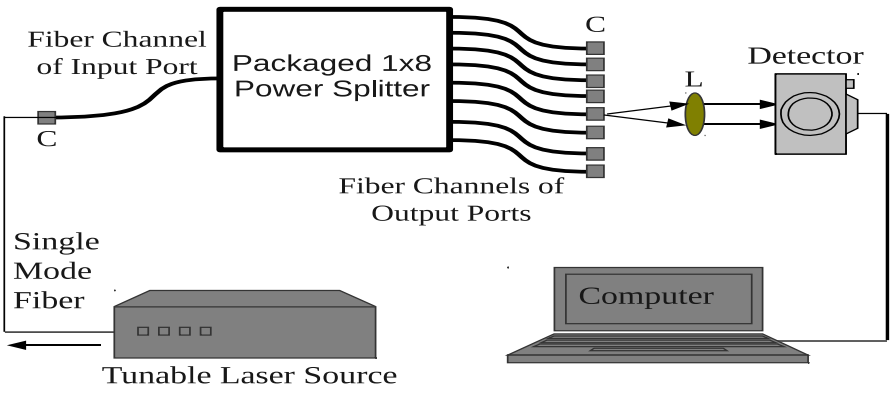


Figure 4.6: Experimental setup for characterization of packaged 1×8 power splitter. (C - Fiber Connector, L - Lens).

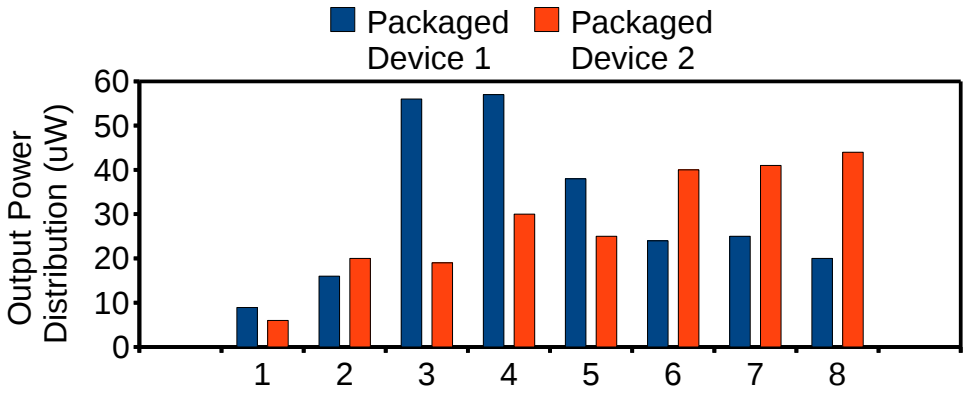


Figure 4.7: Output power distribution of fiber pigtailed and packaged 1×8 power splitter

better uniformity of output power distribution. The corresponding characterization results suggest that such power splitter (with further improved design parameters) can be potentially useful in passive/active optical networks operating in the communication window of $\lambda \sim 1550$ nm.

CHAPTER 5

CONCLUSIONS

5.1 Summary

Integrated optical 1×8 power splitter in SOI platform has been designed based on BPM simulations. Multimode interference based power splitter has been considered in the present work, due to the reason as discussed earlier that it can give lower loss comparing Y junction splitter or free propagation region based power splitters. In order to reduce the fiber-waveguide coupling loss (for the pigtailed device with standard single mode fiber), large cross sectional rib waveguide structures were considered at the input and output sides of the device. Dimensions of multimode interference region were optimized by analyzing many (BPM) simulation results to get eight distinct images with low insertion/excess loss and good output power uniformity.

The output power non-uniformity and excess loss of the device has been further reduced by optimizing the angular and lateral separations of the output waveguides. To make the device compatible for fiber pigtailing, the output ports of the device are separated by 250 μm, with the help of S-bend waveguides. Optimization of the S-bend waveguide parameters were also carried out to minimize the loss. Angular separation of output waveguides also helps to reduce the loss from bend waveguides connected at the output side of the device. In summary, while designing care has been taken to get low excess/insertion loss, uniform output power distribution, less wavelength and polarization dependency. The simulation results with the optimized design parameters show non-uniformity in power distribution among output waveguides as 0.1 dB; excess loss of 0.22 dB. The polarization dependent loss for TE and TM pol. of 0.02 dB ensures that the device is nearly independent on polarization. It has also been observed that the device response is nearly independent of wavelength throughtout in C and L bands.

With the optimized design parameters, the mask has been designed and fabricated as an initial step to realize the device. Photo lithography process parameters were opti-

mized to transfer the pattern from mask to the SOI substrate. Using PPR mask, RIE process parameters for Silicon etching were optimized to realize the rib waveguide structures. After successful fabrication of the device, the end facets of the input and output side waveguides were optically polished to have a maximum surface roughness in the order of 0.1 μm. All the fabrication process parameters were optimized over many attempts and by cross checking the results with appropriate instruments like microscopes, surface profiler and SEM.

Fabricated devices are then characterized in terms of excess loss, insertion loss, polarization dependent loss, non-uniformity in throughput powers and wavelength dependencies (1530 nm < λ < 1580 nm). Characteristics results from four best devices from two different samples have been reported. Comparing the measured values for TM-polarized light, we have noted the typical excess loss of 7.6 dB and the typical insertion loss of 16 dB. Typical output power non-uniformity of 0.7 dB was observed. When the optical power splitter is fabricated in an industrial environment with fine tuned design/fabrication process parameters, then one can obtain excellent devices which can be widely used in real opticcal networks.

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LIST OF PUBLICATIONS BASED ON THIS THESIS

Proceedings

1. **I. Solomon Krubhakar**, R. Narendran, and B.K. Das, "Design and fabrication of integrated optical 1 X 8 power splitter in SOI substrate using large cross-section single-mode waveguides", *Proc. SPIE*, vol. 8173, pp. 81730C-1 to 81730C-6, Oct. 2011.

Conference

1. **I. Solomon Krubhakar**, R. Narendran, Y. K. Karthik and B.K. Das, "Design and fabrication of integrated optical 1 X 8 power splitter in SOI substrate using large cross-section single-mode waveguides", *International Conference on Fiber Optics and Photonics : Photonics - 2010*, Dec. 12-15, Guwahati, India (Oral Presentation).

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