

A Comparison of Approaches to Carrier Generation for Zigbee Transceivers

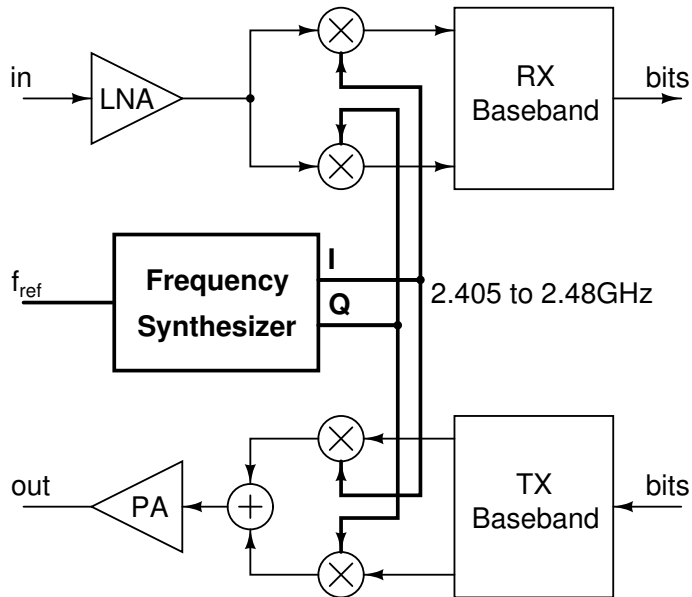
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Leburu Manojkumar
Arun Mohan
Nagendra Krishnapura

Department of Electrical Engineering
Indian Institute of Technology, Madras
Chennai, 600036, India

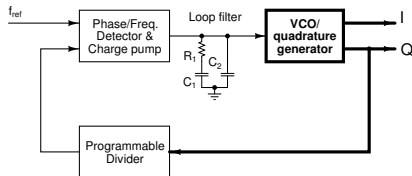
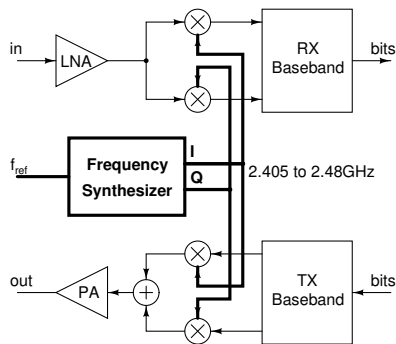
6 January 2009

Zigbee transceiver



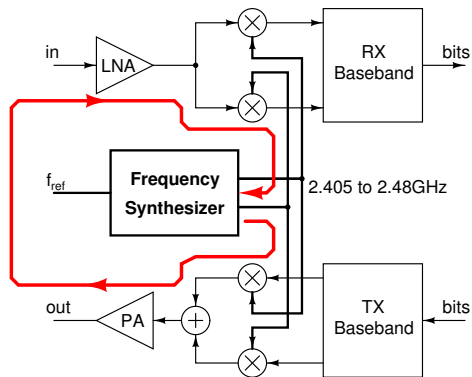
- Local oscillator requirements
- IQ generation by dividing a double frequency waveform
- IQ generation by multiplying half frequency waveforms
- Design details
- Simulation results
- Conclusions

Local oscillator requirements



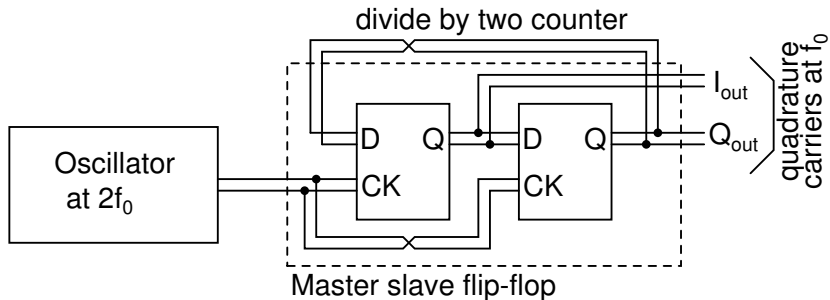
- 2.405-2.48 GHz in 5 MHz steps
- Phase noise ≤ -92 dBc/Hz at 3.5 MHz offset
- Settling time $\leq 200 \mu\text{s}$ (to 40ppm accuracy)
- Spurs ≤ -20 dBc @ 5 MHz, ≤ -50 dBc @ 10 MHz

Choice of oscillator frequency

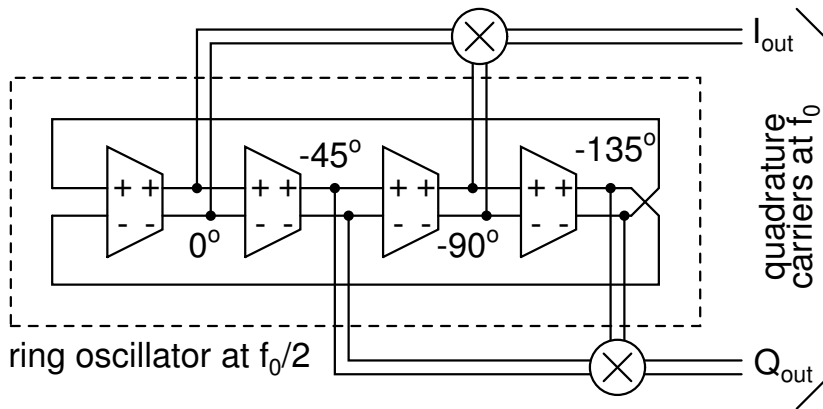


- Tx signal coupling pulls the oscillator and increases jitter
- Oscillator frequency should be different from the carrier

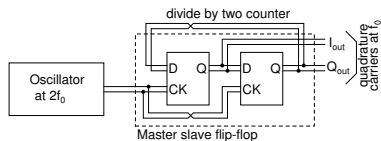
Quadrature generation using divide-by-2



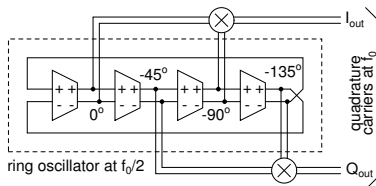
Quadrature generation using multiplication



Comparison

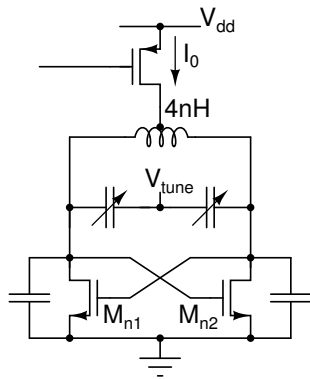
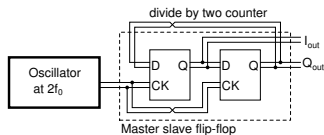


- Higher frequency
- LC oscillator
- Lower phase noise
- More area



- Lower frequency
- Ring oscillator
- Higher phase noise
- Compact

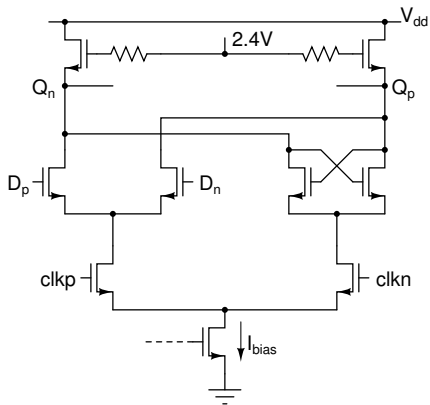
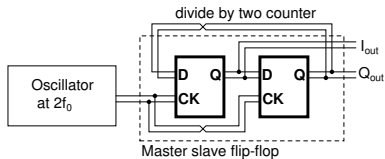
LC oscillator



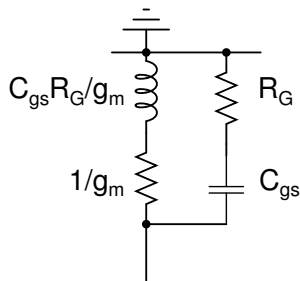
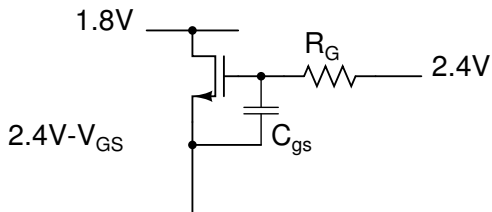
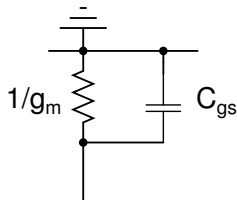
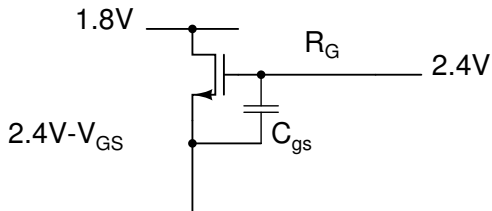
- 140 μm square spiral
- 6 turns
- 6 μm trace width

- 2.06 μm thick top metal
- 2 μm spacing
- 5 section distributed model for simulations

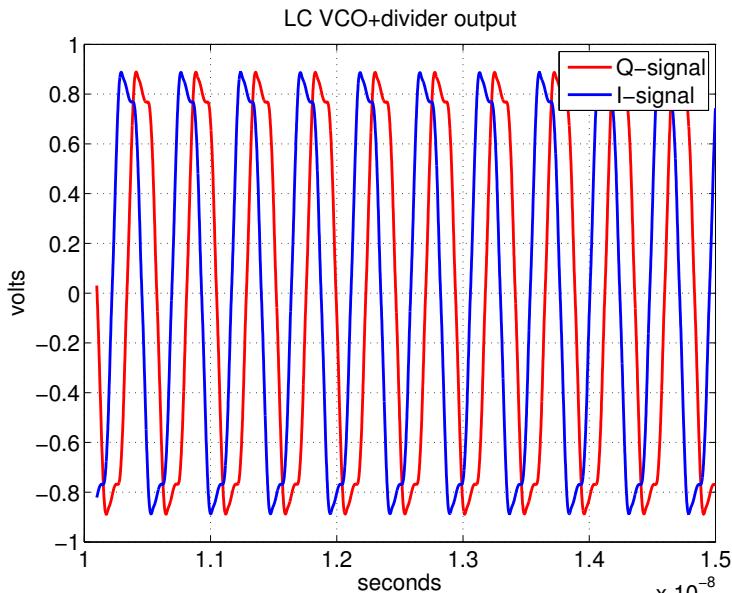
Master slave divide by two



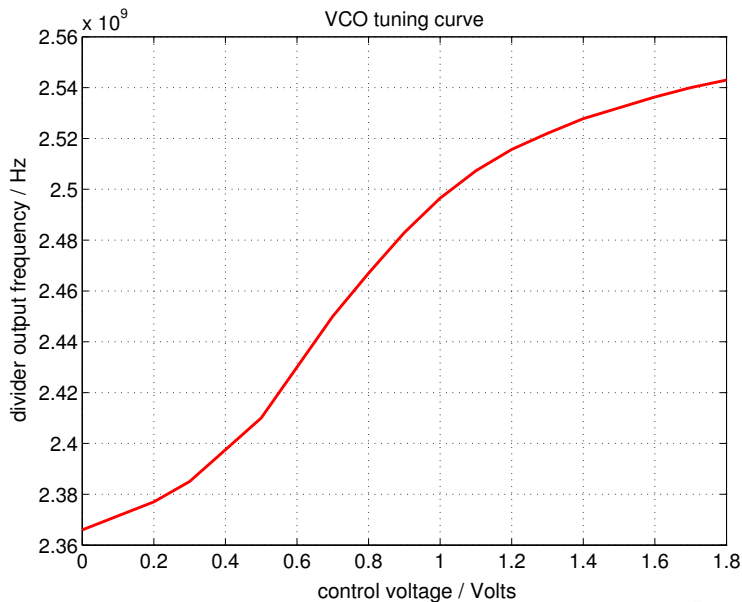
Active inductor load



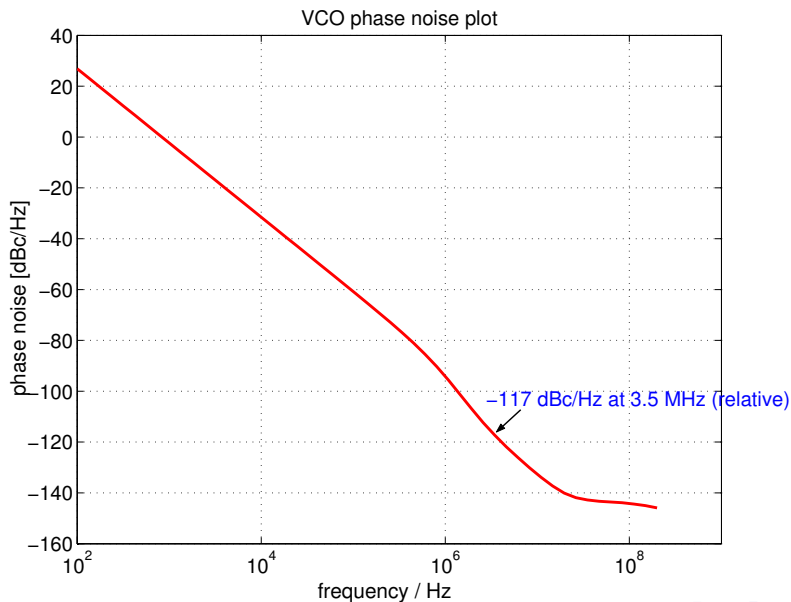
LC VCO+divider waveforms



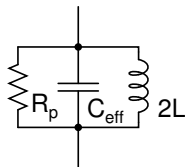
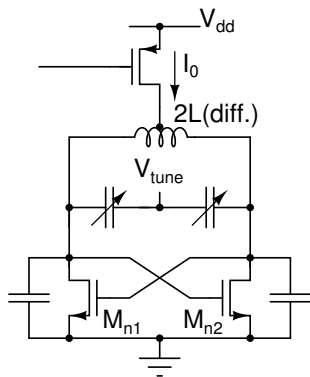
LC VCO+divider characteristics



LC VCO+divider phase noise



Trade off phase noise for area/power?

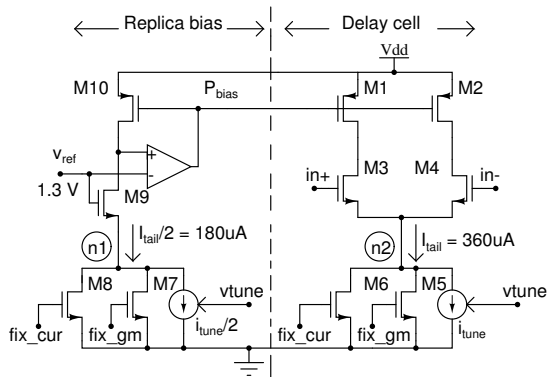
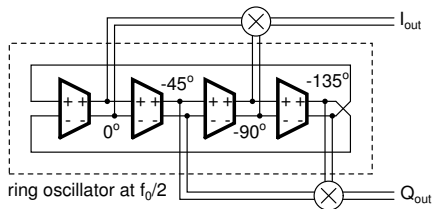


R_p : tank loss
(shunt equivalent)

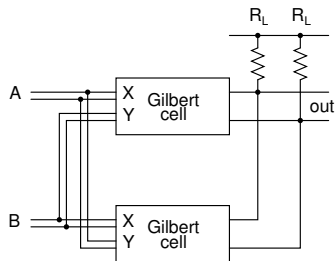
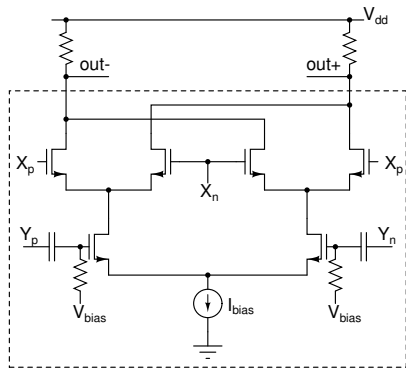
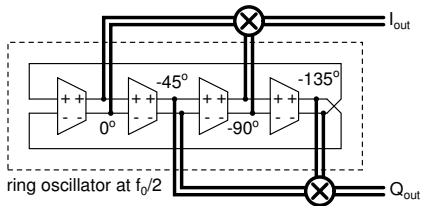
$$L(f) \propto \frac{1}{R_p}$$

$$V_{ppd} = \frac{4}{\pi} I_0 R_p$$

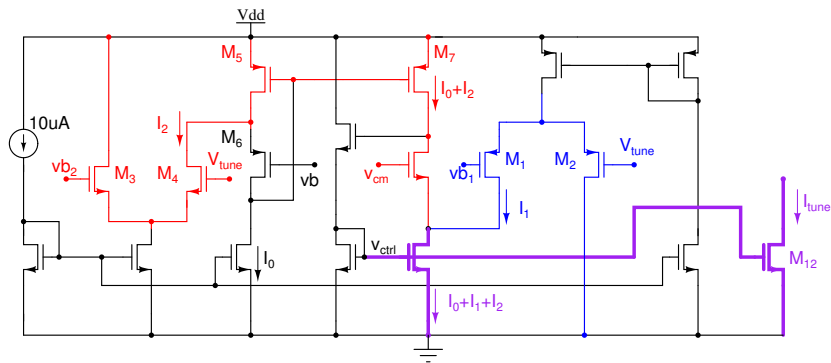
Ring oscillator delay cell



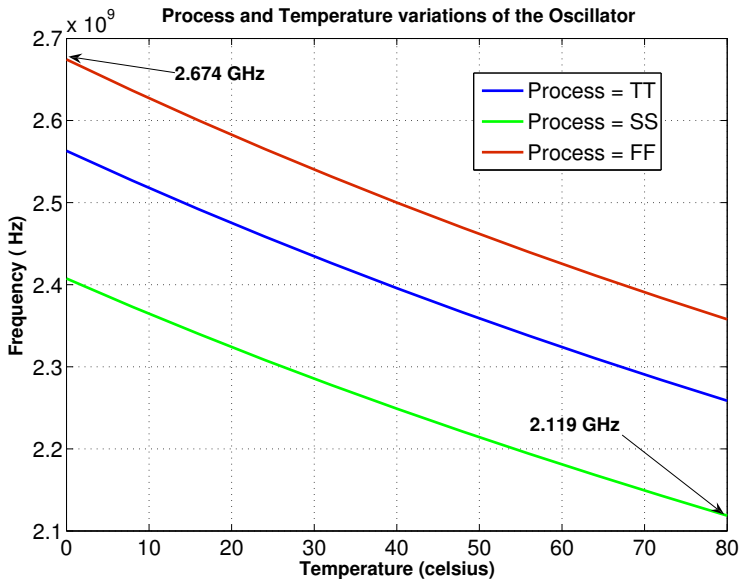
Frequency doubler



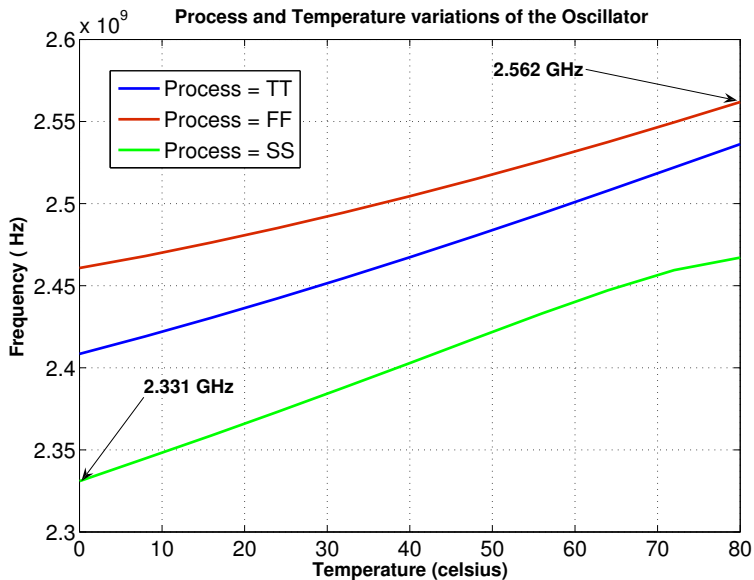
Voltage to current converter



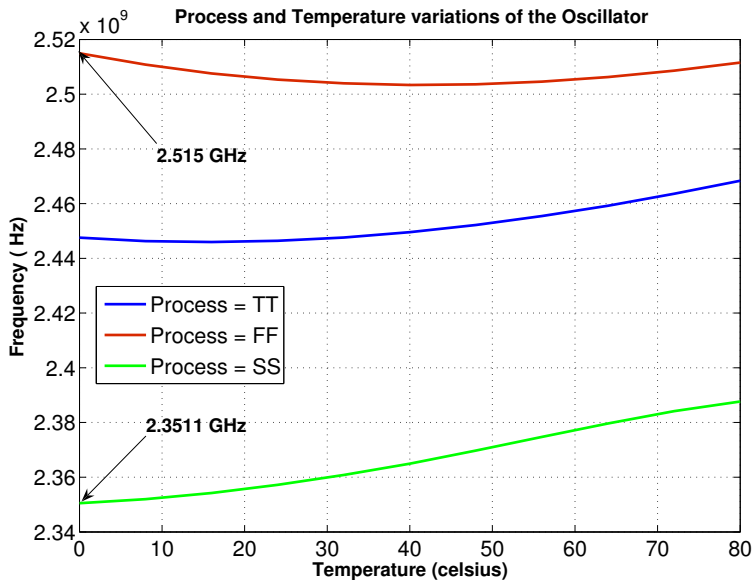
Ring VCO with a constant current biasing



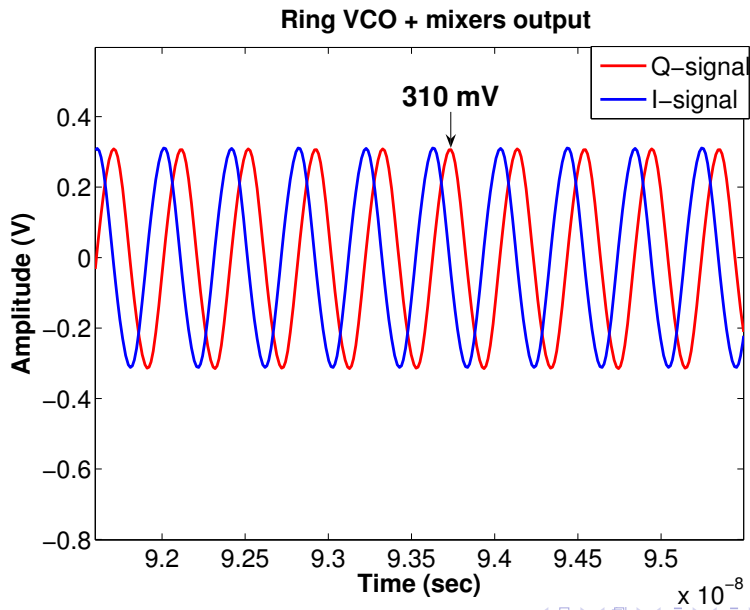
Ring VCO with a constant g_m biasing



Ring VCO with mixed biasing

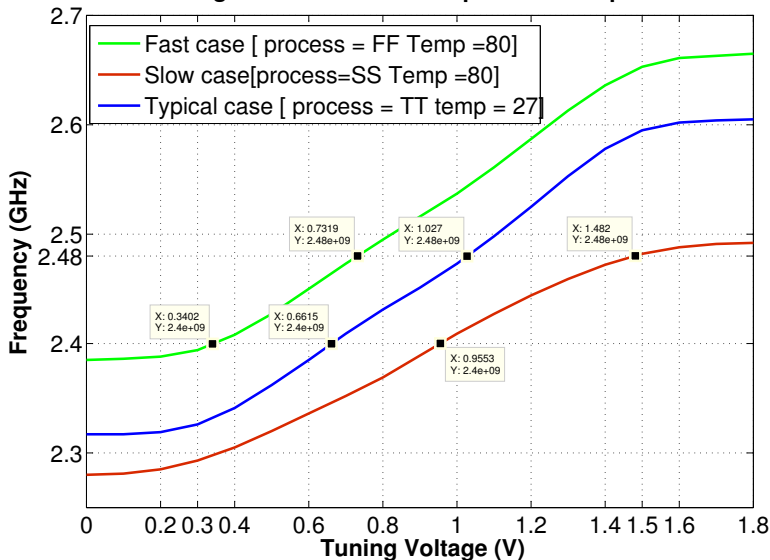


Ring VCO+doubler output waveforms



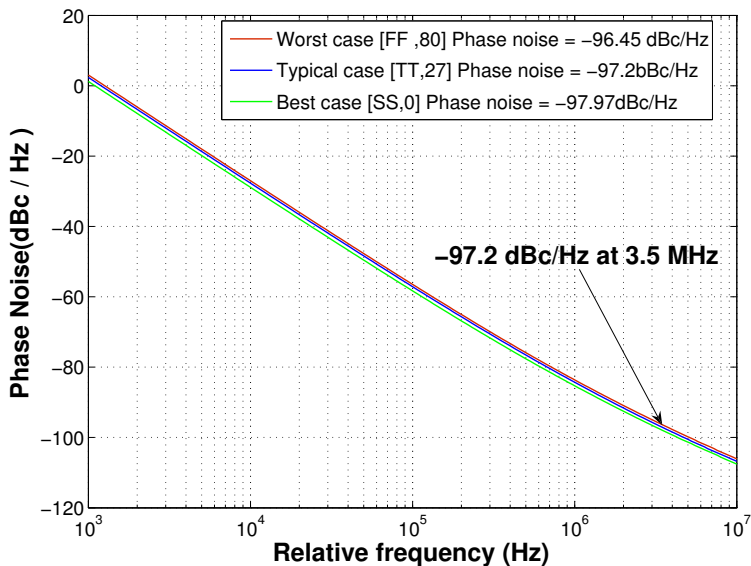
Ring VCO+doubler characteristics

Tuning of the VCO over Temperature and process

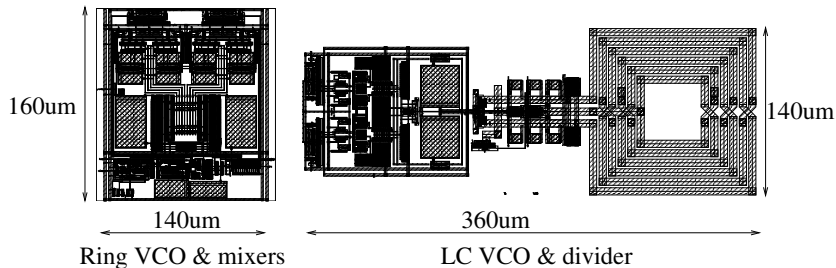


Ring VCO+doubler phase noise

Phase noise for different corners



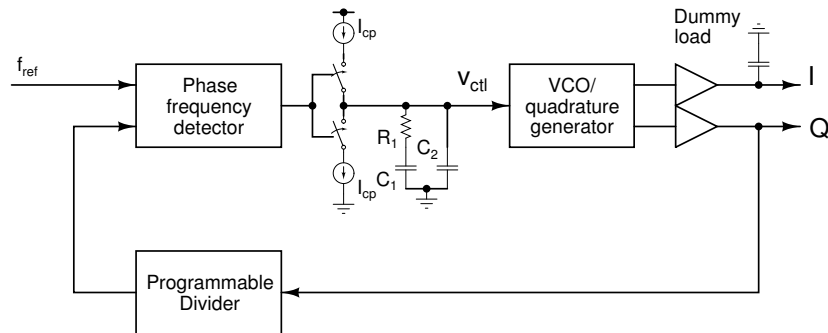
Quadrature generator layouts



VCOs: Performance summary

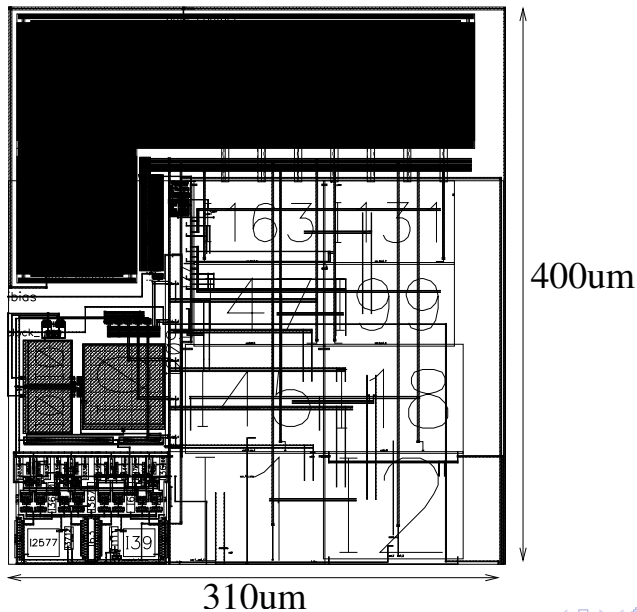
	LC osc. + divider	Ring osc. + doubler
VCO	1 mA	1.44 mA
Bias circuit	—	0.355 mA
V-I converter	—	0.1 mA
Divider	1.8 mA	—
Multipliers	—	0.45 mA each
Buffers	0.7 mA each	0.83 mA each
Total current	4.2 mA	4.455 mA (nom.) 6 mA (max.)
Phase noise	-117 dBc/Hz	-97 dBc/Hz
Area	360 μm x 140 μm	160 μm x 140 μm
K_{VCO}	200 MHz/V	220 MHz/V
Technology	0.18 μm CMOS	

Frequency synthesizer



- $K_{VCO} = 200 \text{ MHz/V}$
- Loop bandwidth = 53 kHz
- zero: 9 kHz
- high freq. pole: 293 kHz

Frequency synthesizer layout



Frequency synthesizer: Performance summary

Programmable divider	1.09 mA
Differential to single ended converter	22 μ A
Phase frequency detector	23 μ A
Charge pump	20 μ A
Bias generation circuits	350 μ A
Total current	1.5 mA
Settling time	110 μs
Area	400 μm x 310 μm
Reference feedthrough	-39 dBc (5 MHz) -50 dBc (10 MHz)
Technology	0.18 μ m CMOS

Conclusions

Ring oscillator based synthesizer

- Meets Zigbee specifications
- Consumes 40% higher power than an LC oscillator
- Occupies $2.25\times$ smaller area than an LC oscillator

LC oscillator based synthesizer

- Phase noise much better than Zigbee requirements
- Area (quality factor) and power limited by amplitude

Comparison valid for finer geometries as well

- No significant advantage for oscillators
- Dividers, multipliers benefit from scaling

References



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