# A 5Gb/s NRZ Transceiver with Adaptive Equalization for Backplane Transmission

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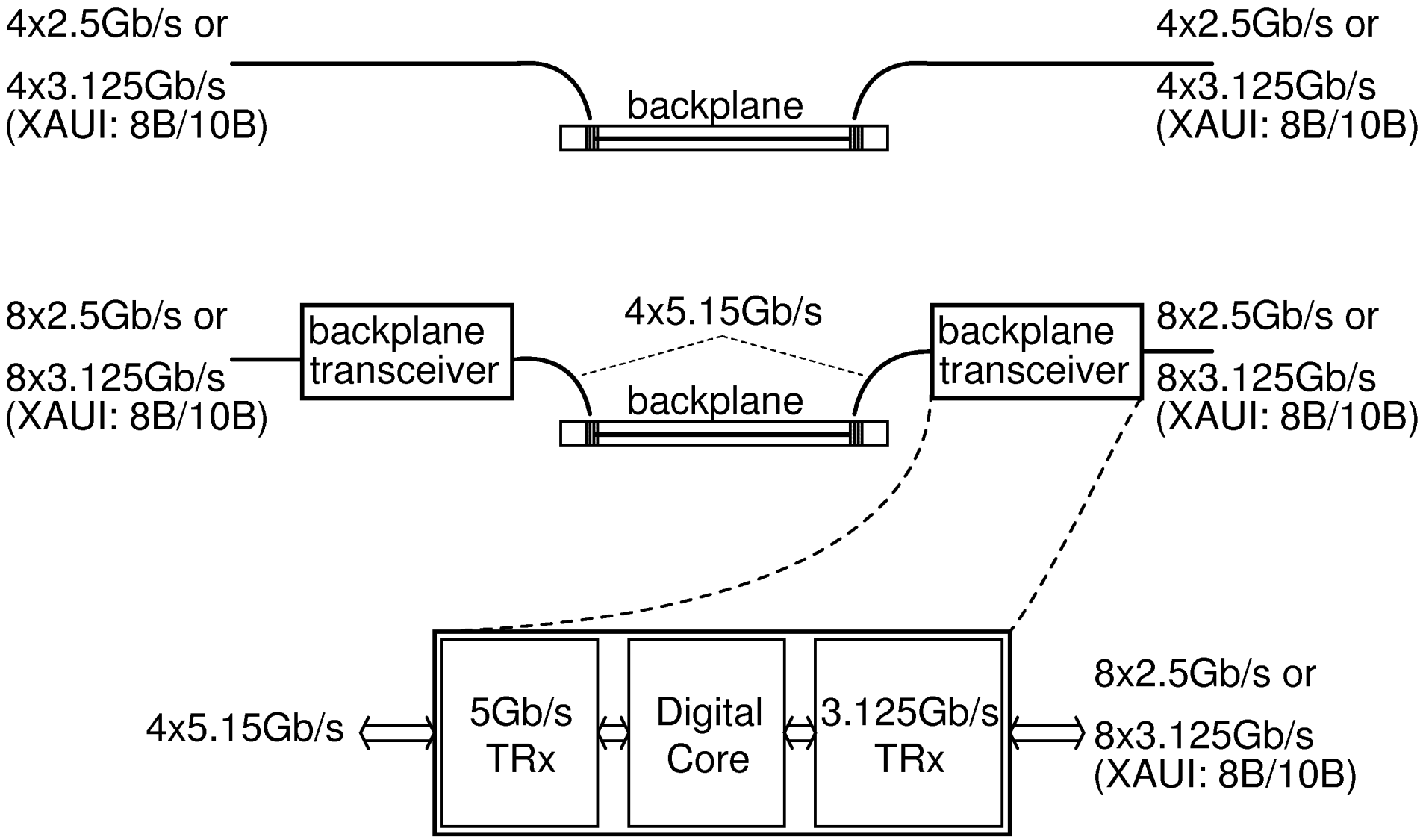
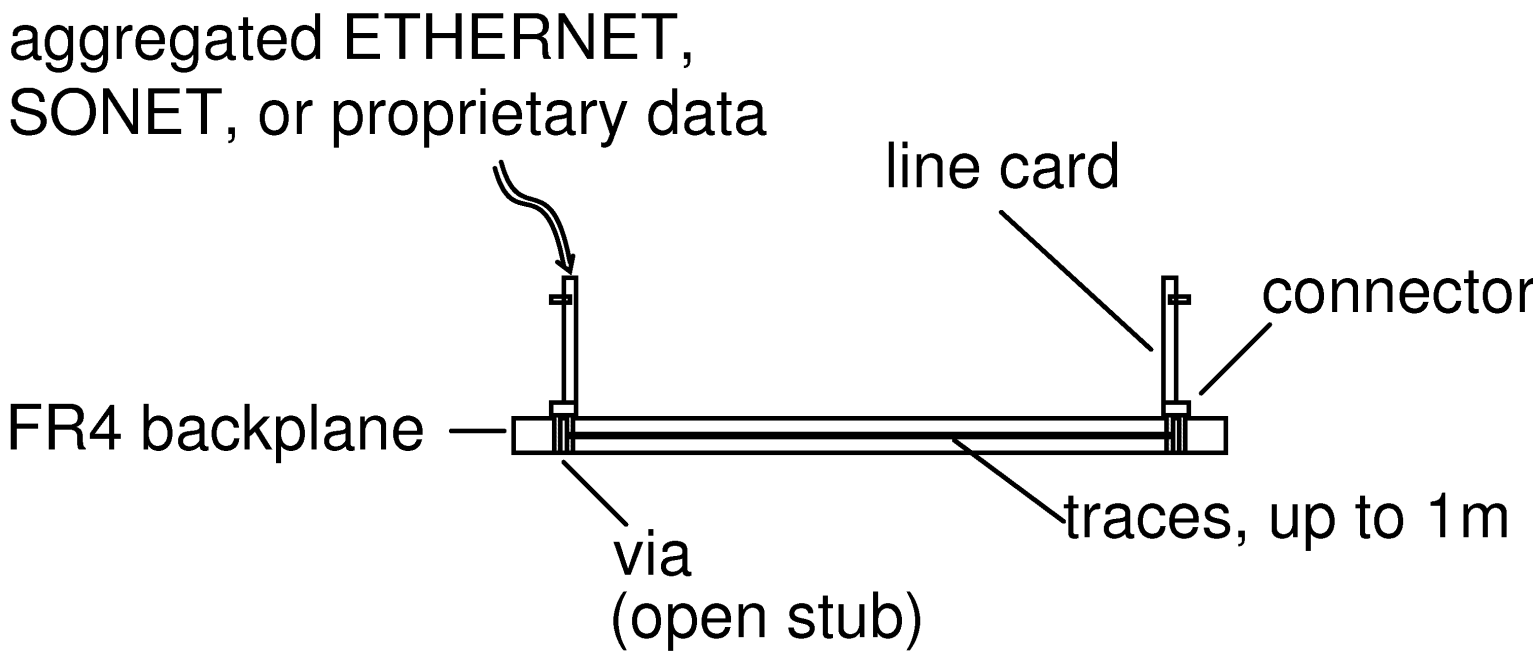
# Outline

- Motivation
- Backplane characteristics and equalization
- Architecture of the chip
- Receiver
- Transmitter
- Clock multiplier unit
- Experimental results
- Conclusions

# Motivation


4x2.5Gb/s or
4x3.125Gb/s
(XAUI: 8B/10B)
backplane
4x2.5Gb/s or
4x3.125Gb/s
(XAUI: 8B/10B)
8x2.5Gb/s or
8x3.125Gb/s
(XAUI: 8B/10B)
backplane transceiver
4x5.15Gb/s
backplane
backplane transceiver
8x2.5Gb/s or
8x3.125Gb/s
(XAUI: 8B/10B)
4x5.15Gb/s
5Gb/s TRx
Digital Core
3.125Gb/s TRx
8x2.5Gb/s or
8x3.125Gb/s
(XAUI: 8B/10B)

# Backplane characteristics



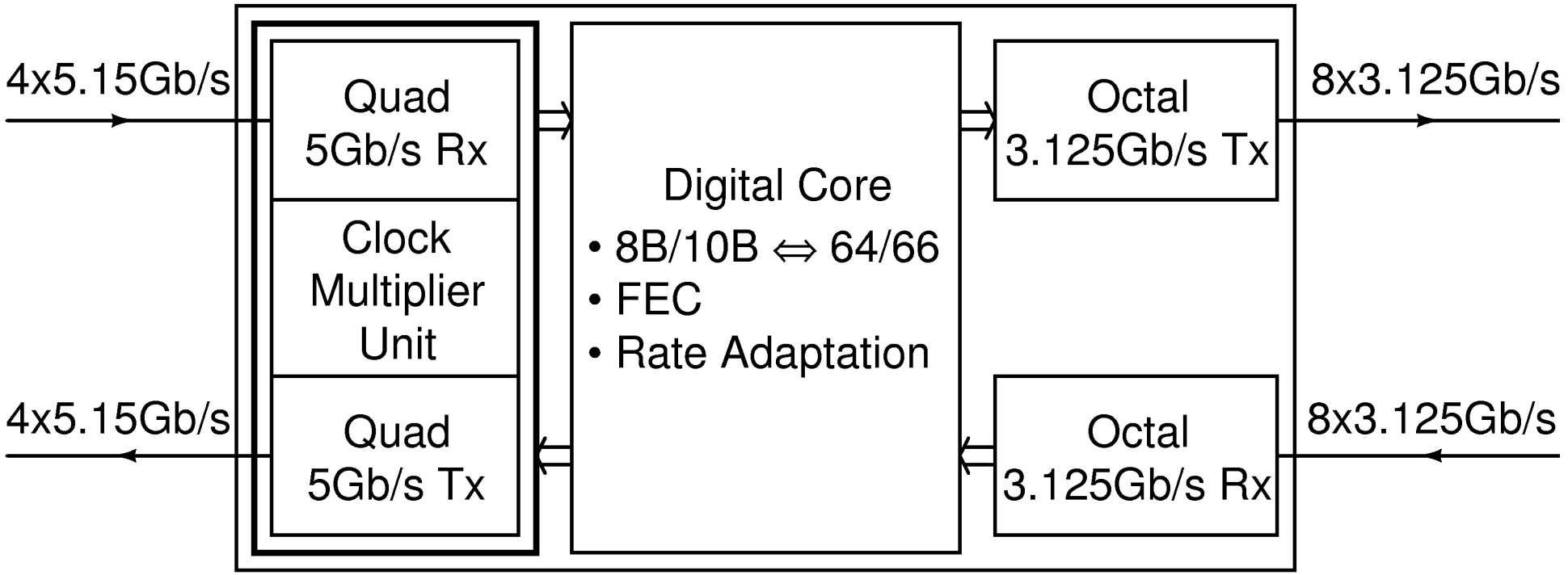

- Attenuation from the trace
- Reflection from vias and connectors
- Crosstalk from connectors

$\Rightarrow$ Need equalization

# Equalization techniques

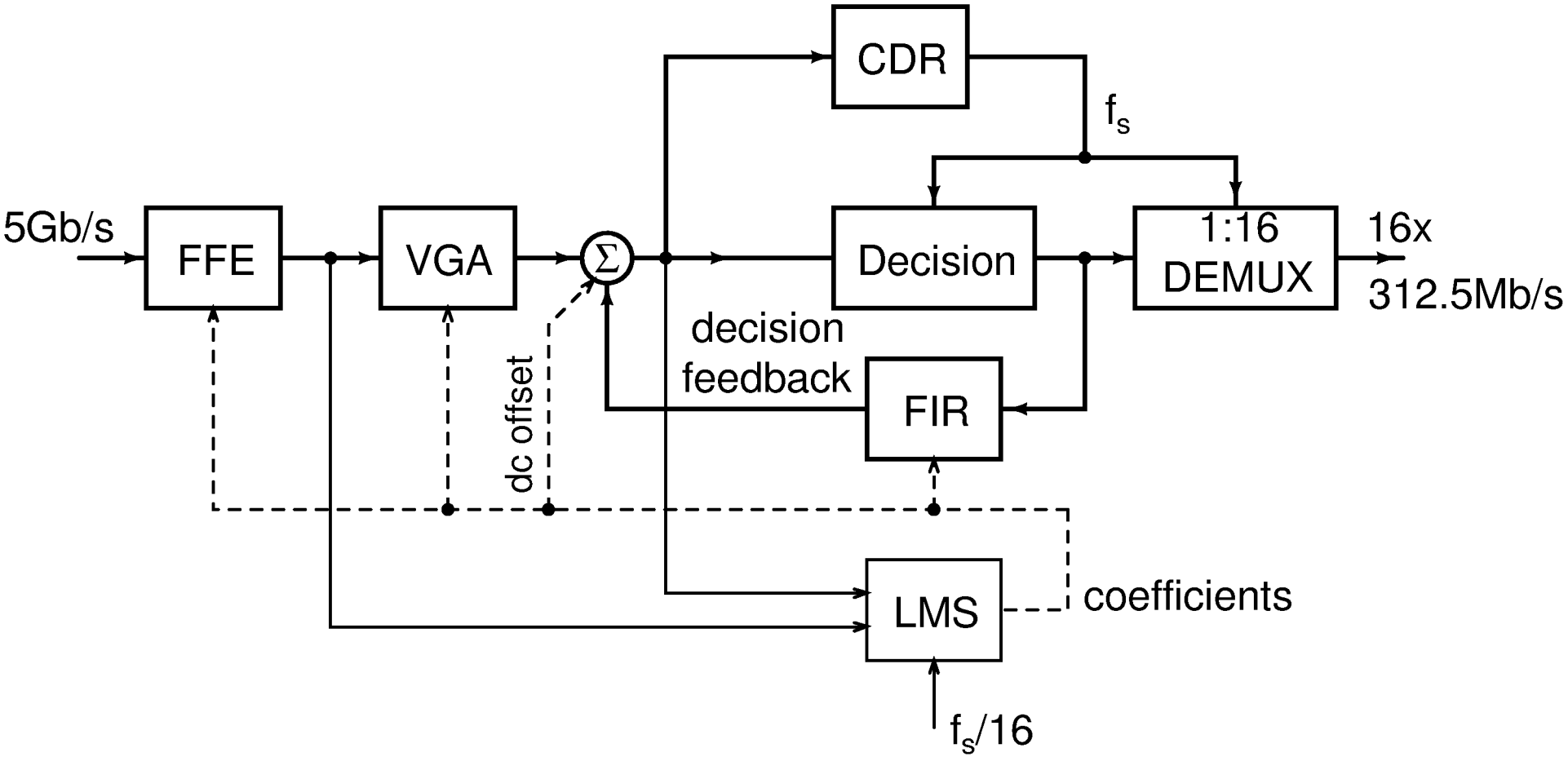
- Transmitter pre-emphasis
  - + Improves eye opening
  - – Increases crosstalk
- Receiver feedforward equalization
  - + Improves eye opening
  - – Amplifies crosstalk
- Receiver decision feedback equalization
  - + Improves eye opening
  - + Doesn’t increase crosstalk
  - – Can only cancel post cursor ISI
  - – Can result in error propagation

# Backplane transceiver chip

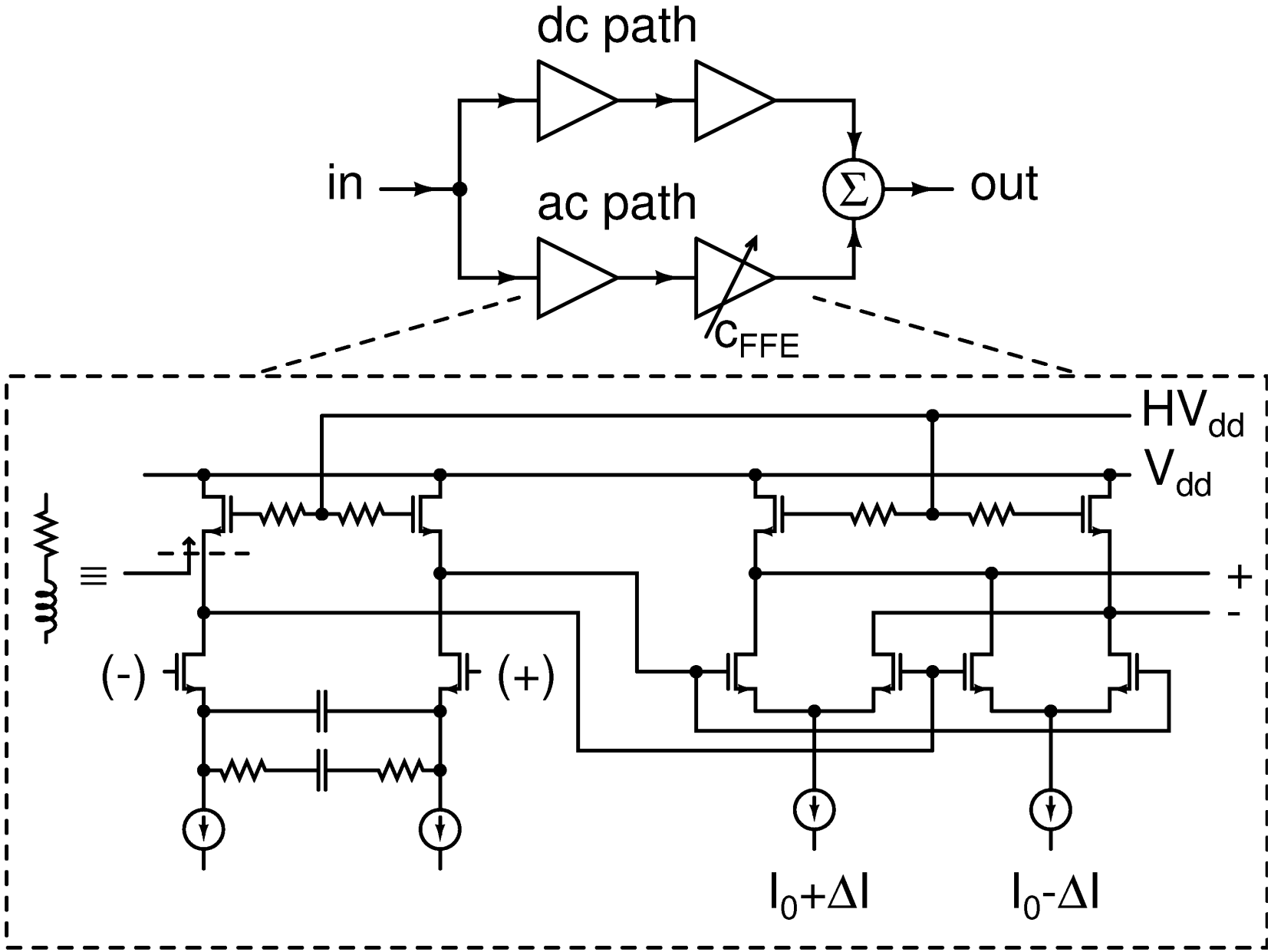



- 8B/10B in XAUI stripped in the digital core
- 2x XAUI ≡ 5.15Gb/s
- FEC: 3.5dB coding gain

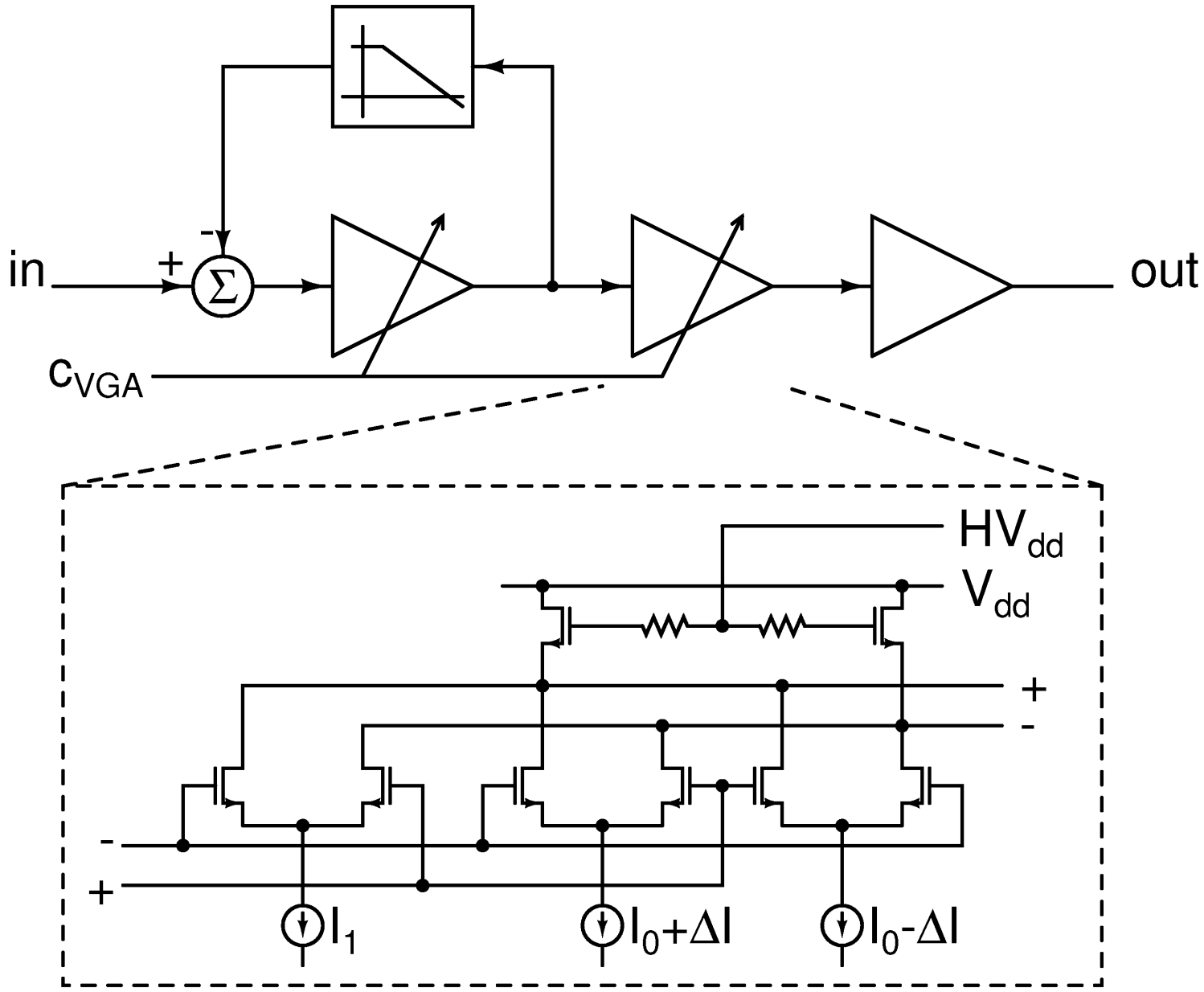
# Receiver architecture



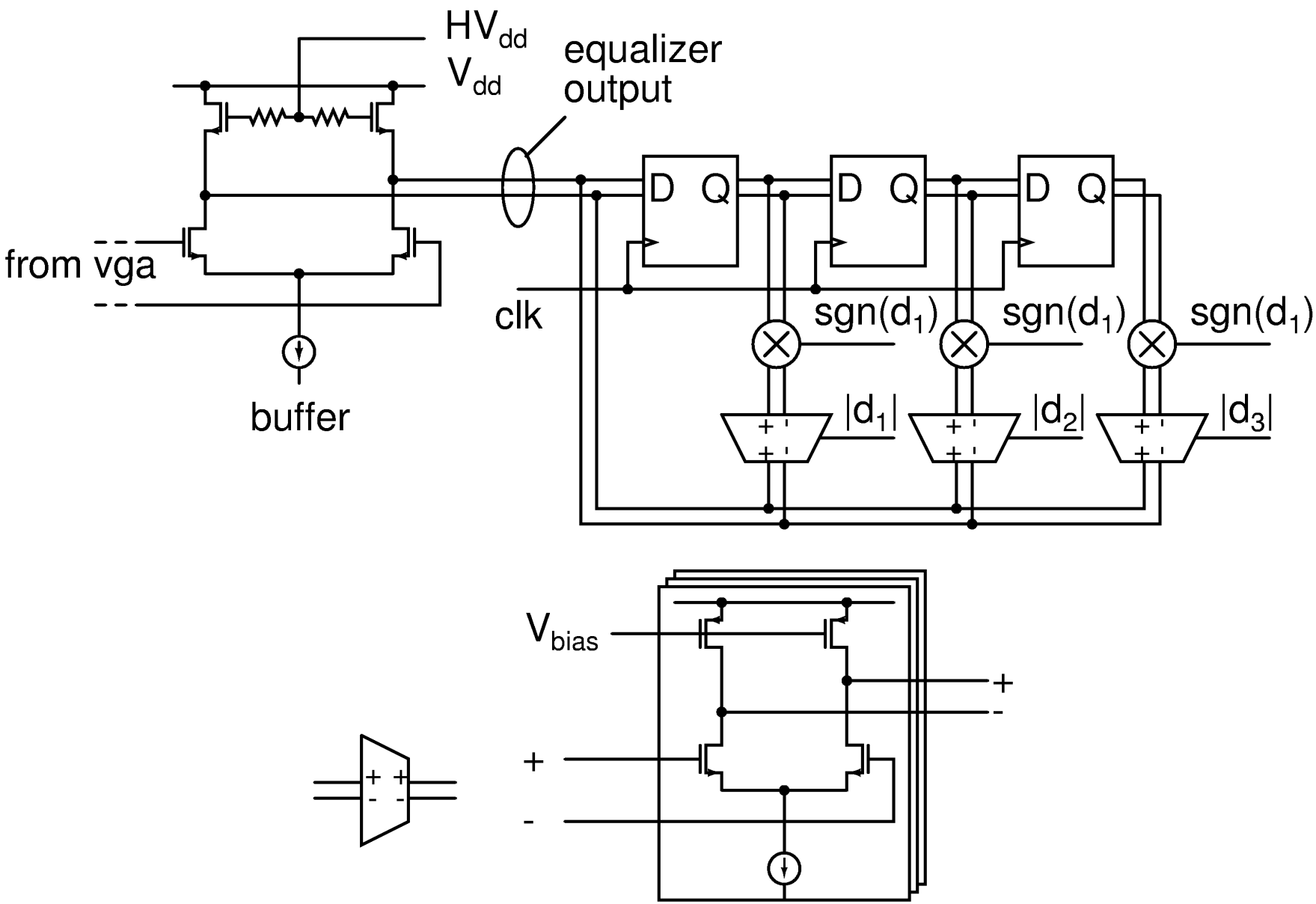
# FFE



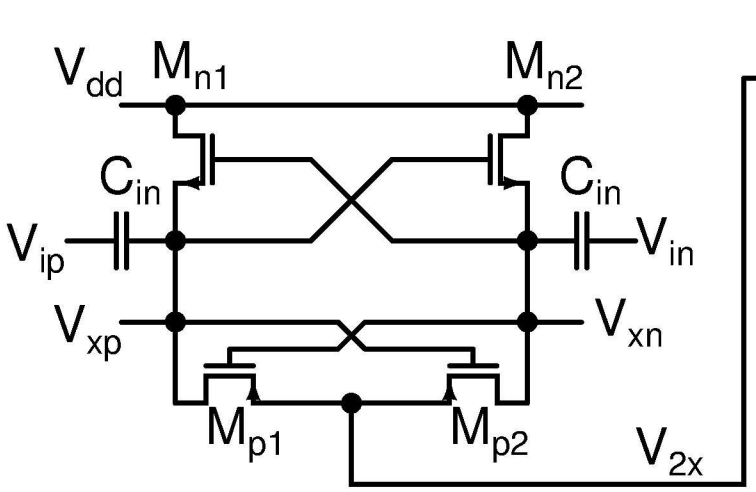
# VGA



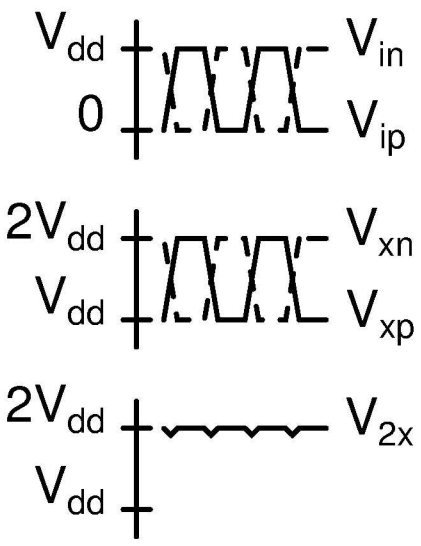
# Decision feedback equalizer



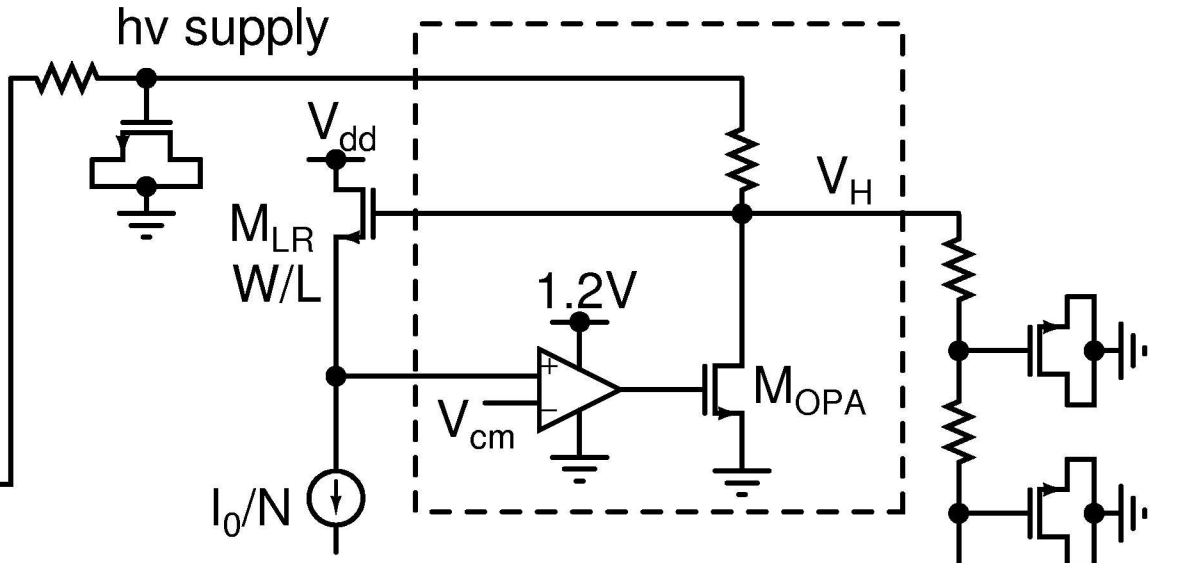
# High voltage bias generator

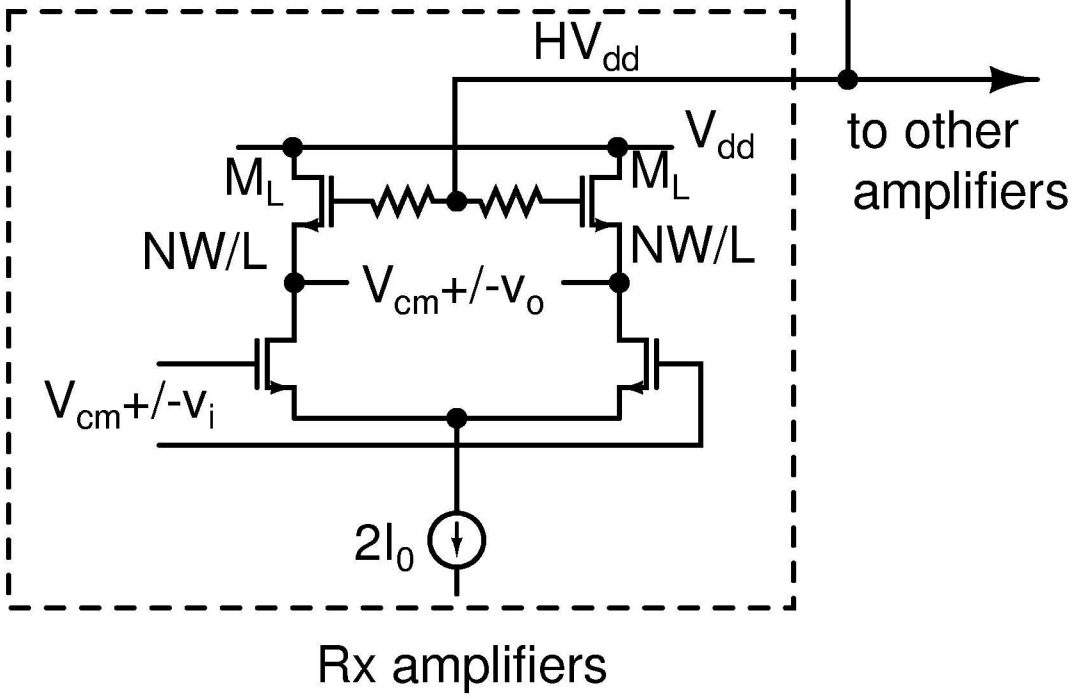



Voltage doubler



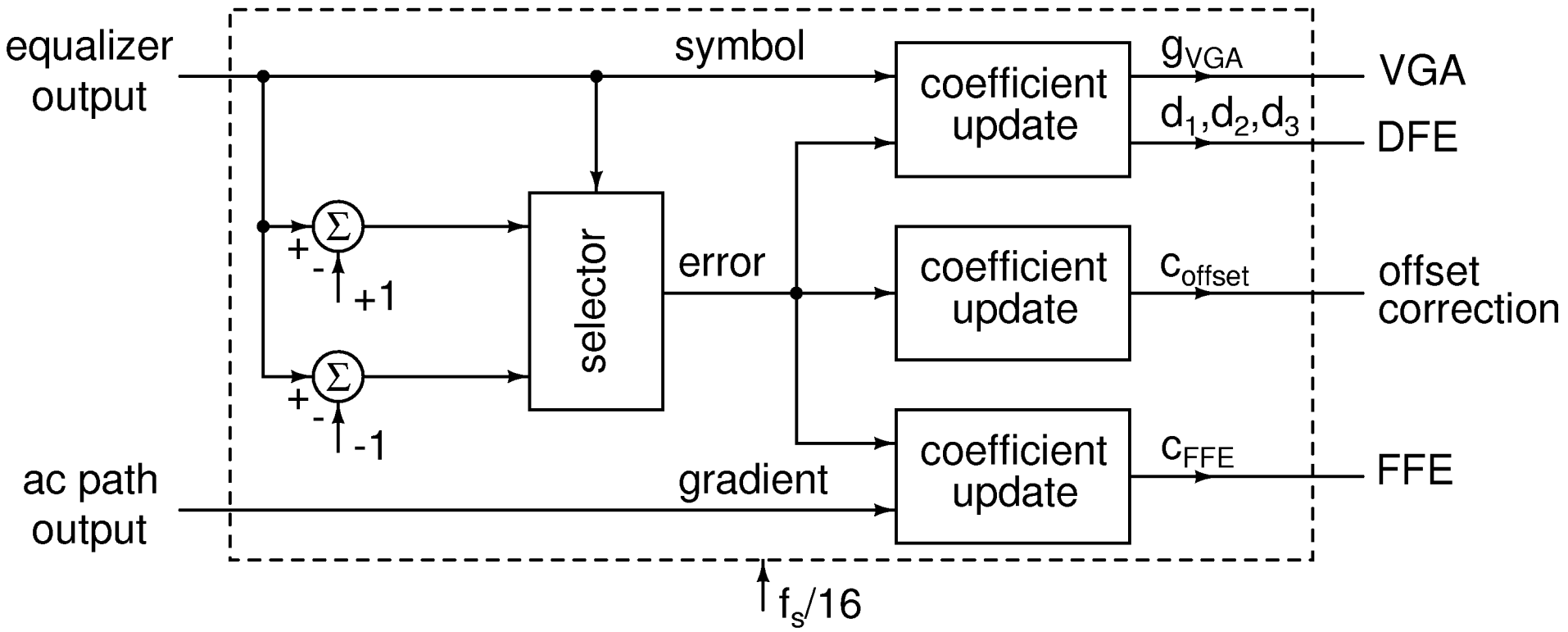

doubler waveforms



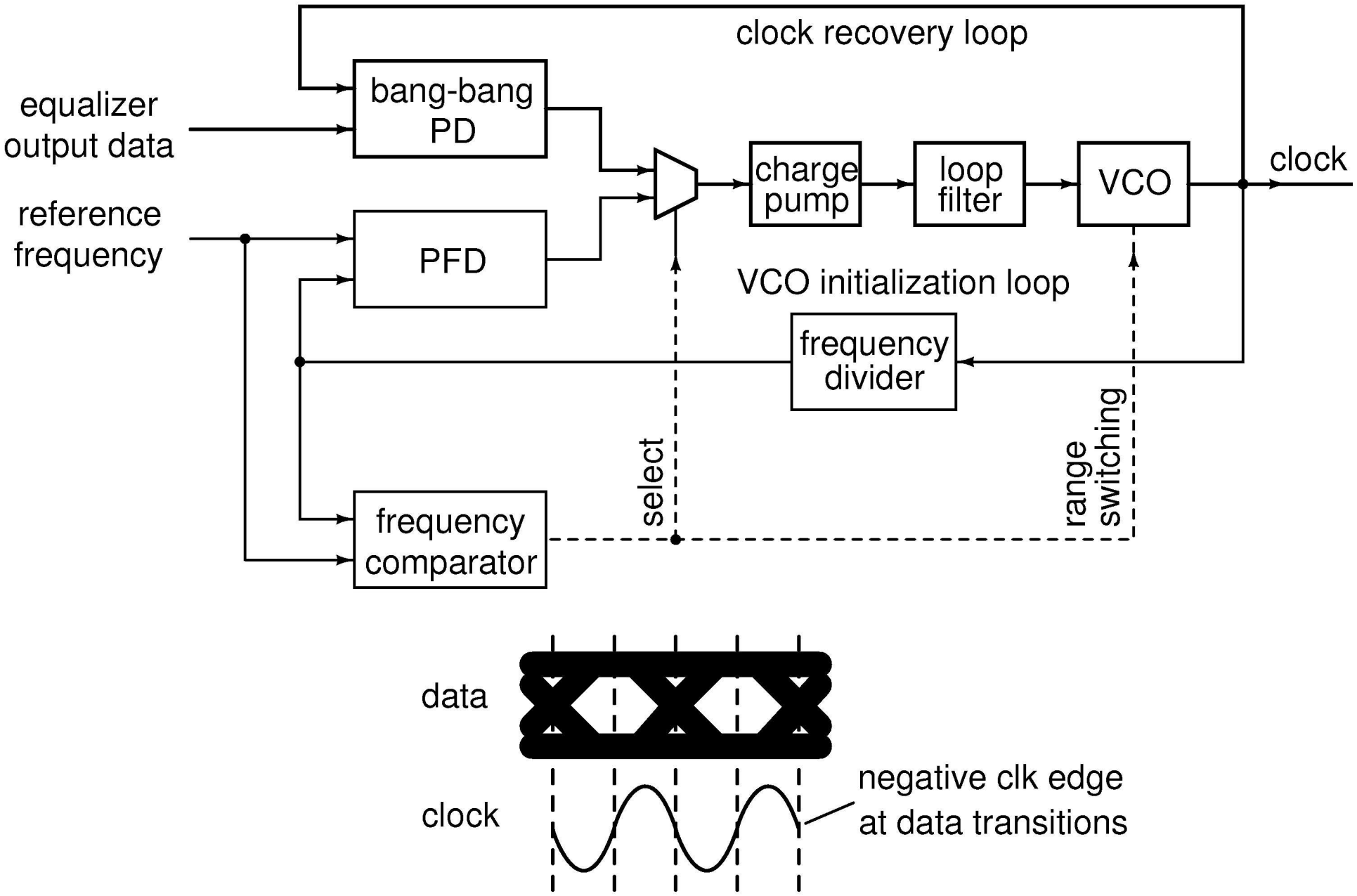

Rx amplifiers

# LMS adaptation

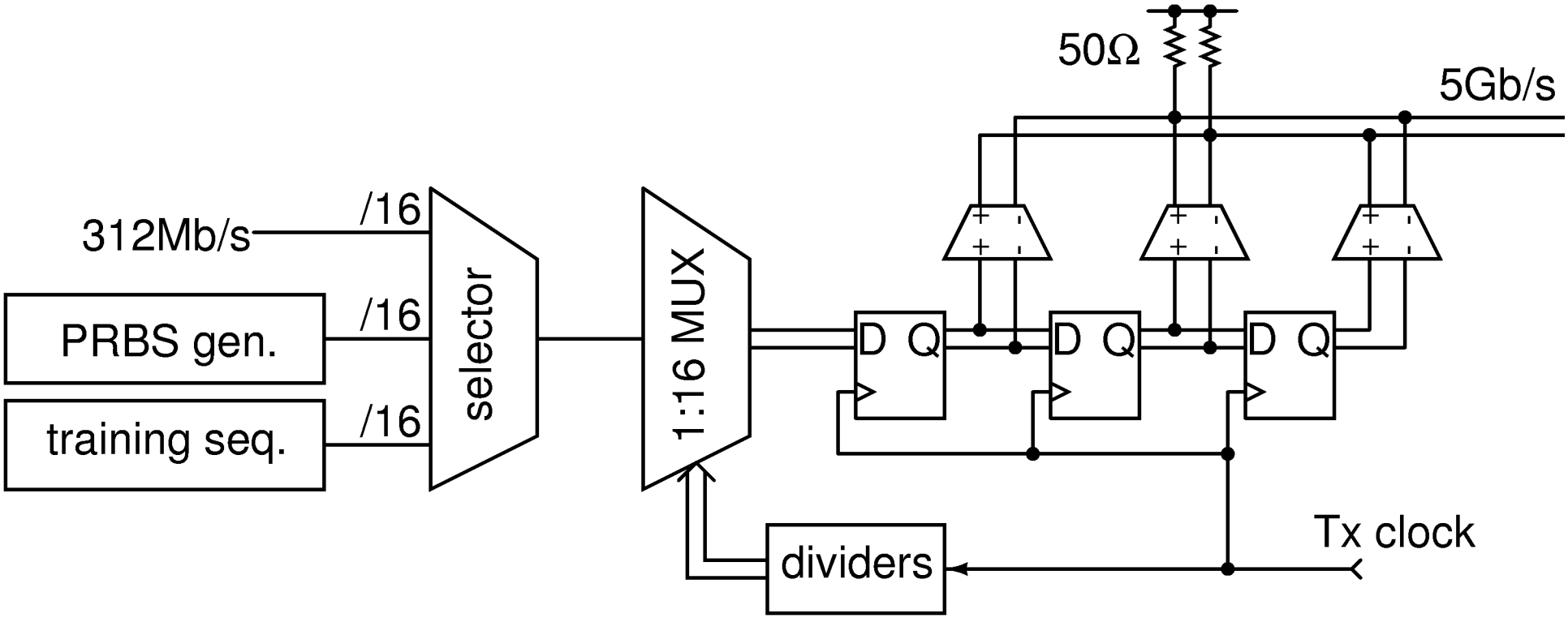



$$c_k[n+1] = c_k[n] - \mu \,\mathrm{sgn}(e[n])\,\mathrm{sgn}\left(\frac{de[n]}{dc_k}\right)$$

# Clock and data recovery

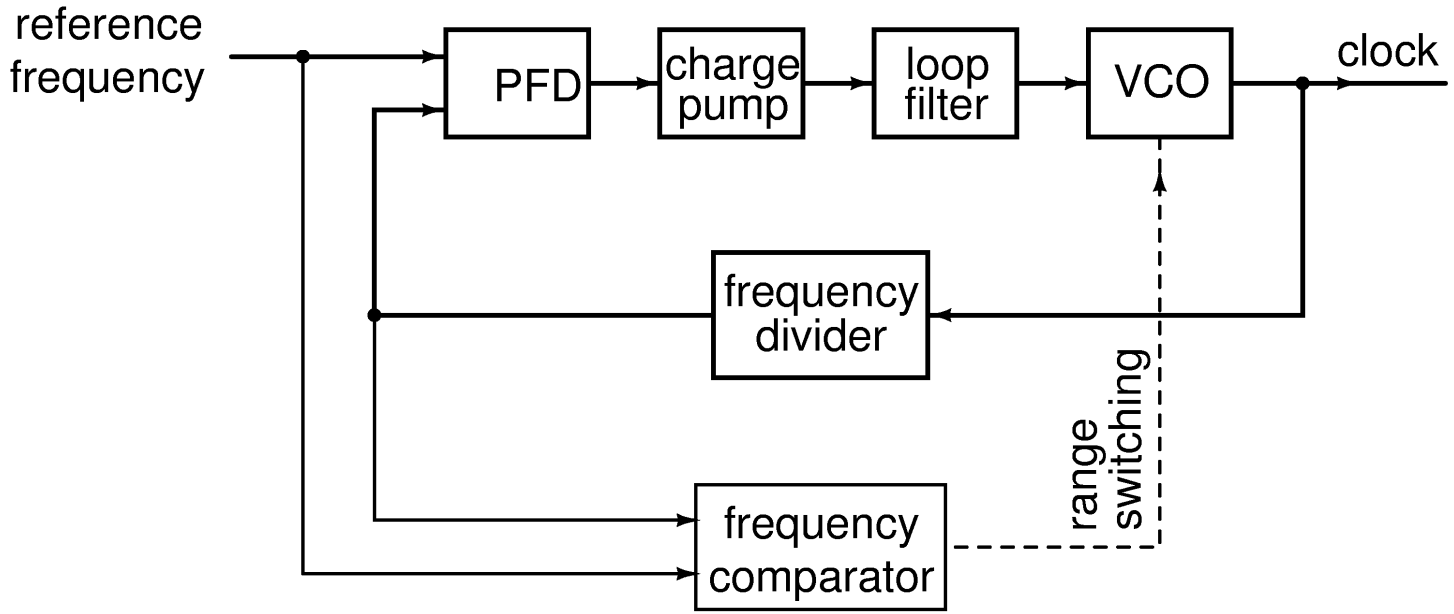


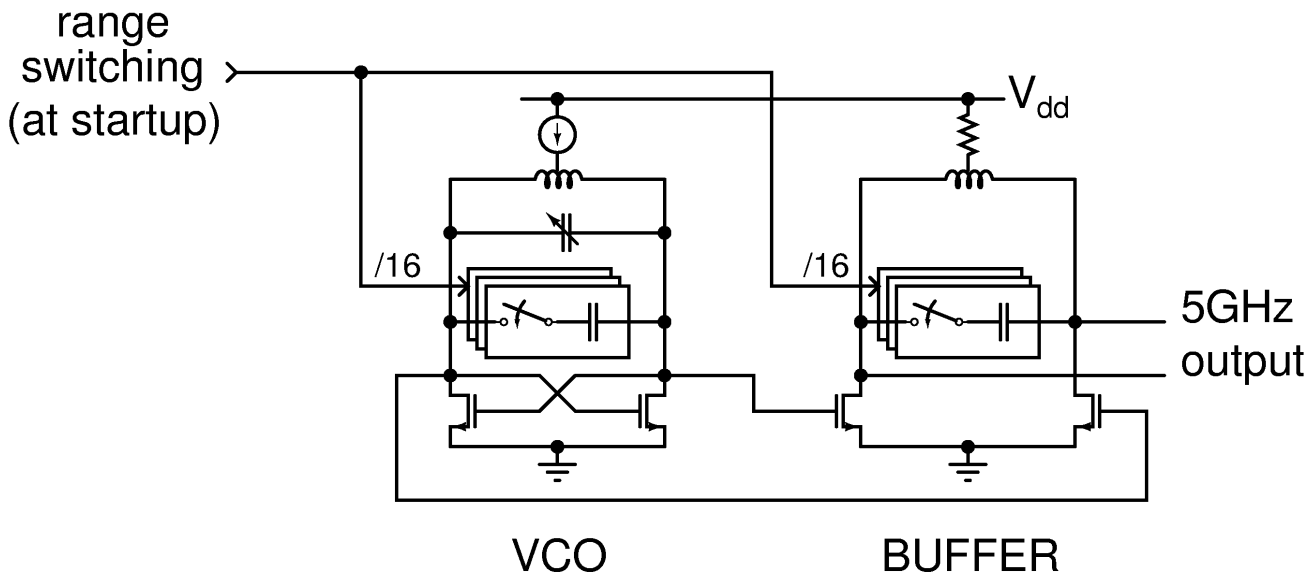
# Transmitter



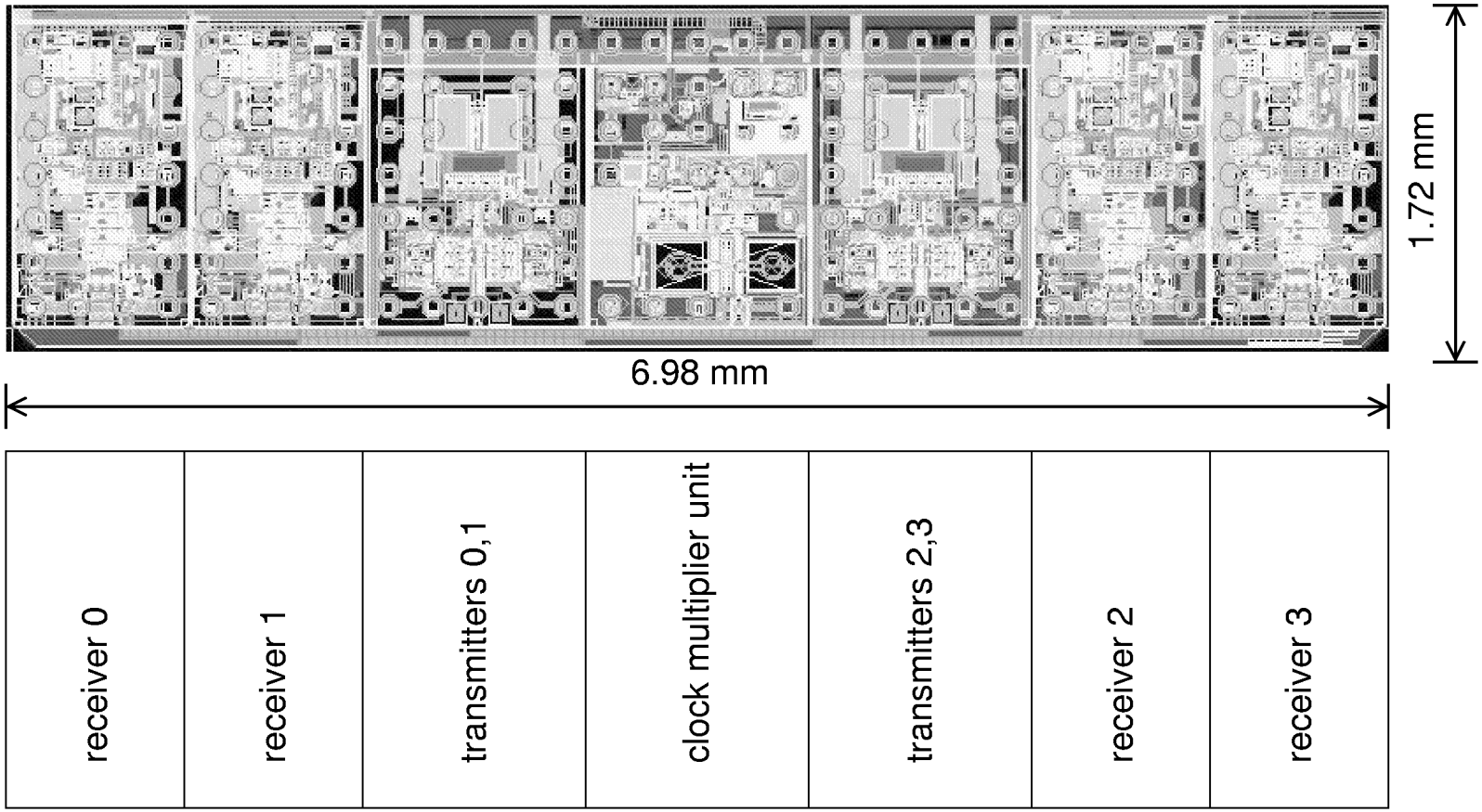

$$y[n]=c_{-1}x[n-1]+c_0x[n]+c_1x[n+1]$$

# Clock multiplier unit



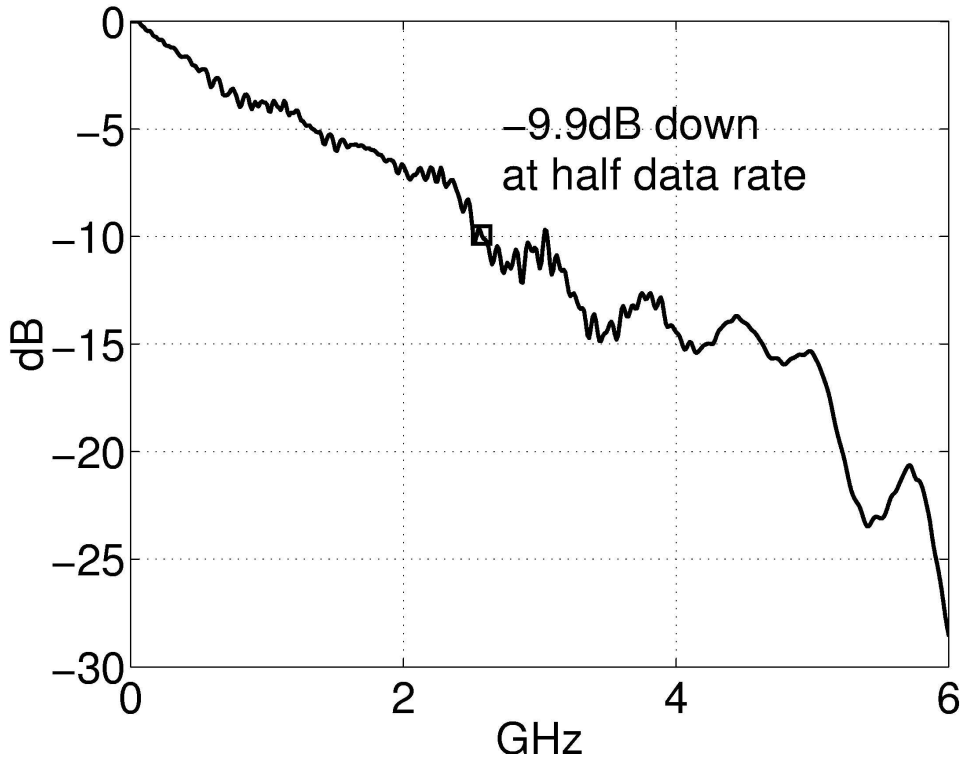



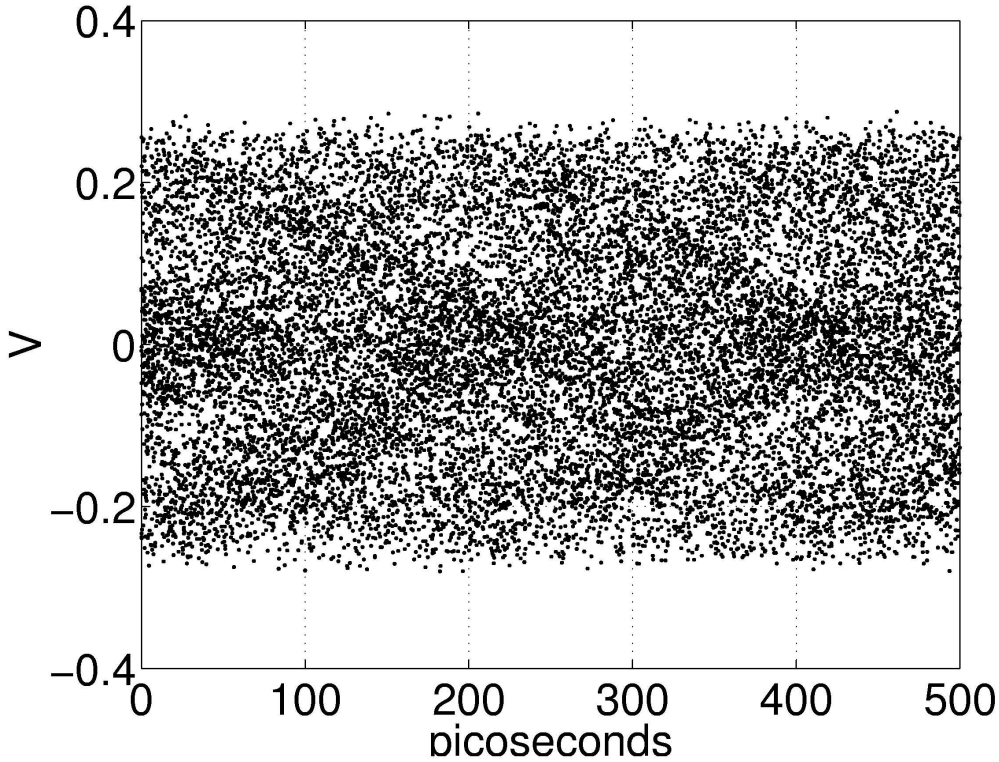
# Quad 5Gb/s transceiver




- 0.13µm CMOS, 8 metal layers

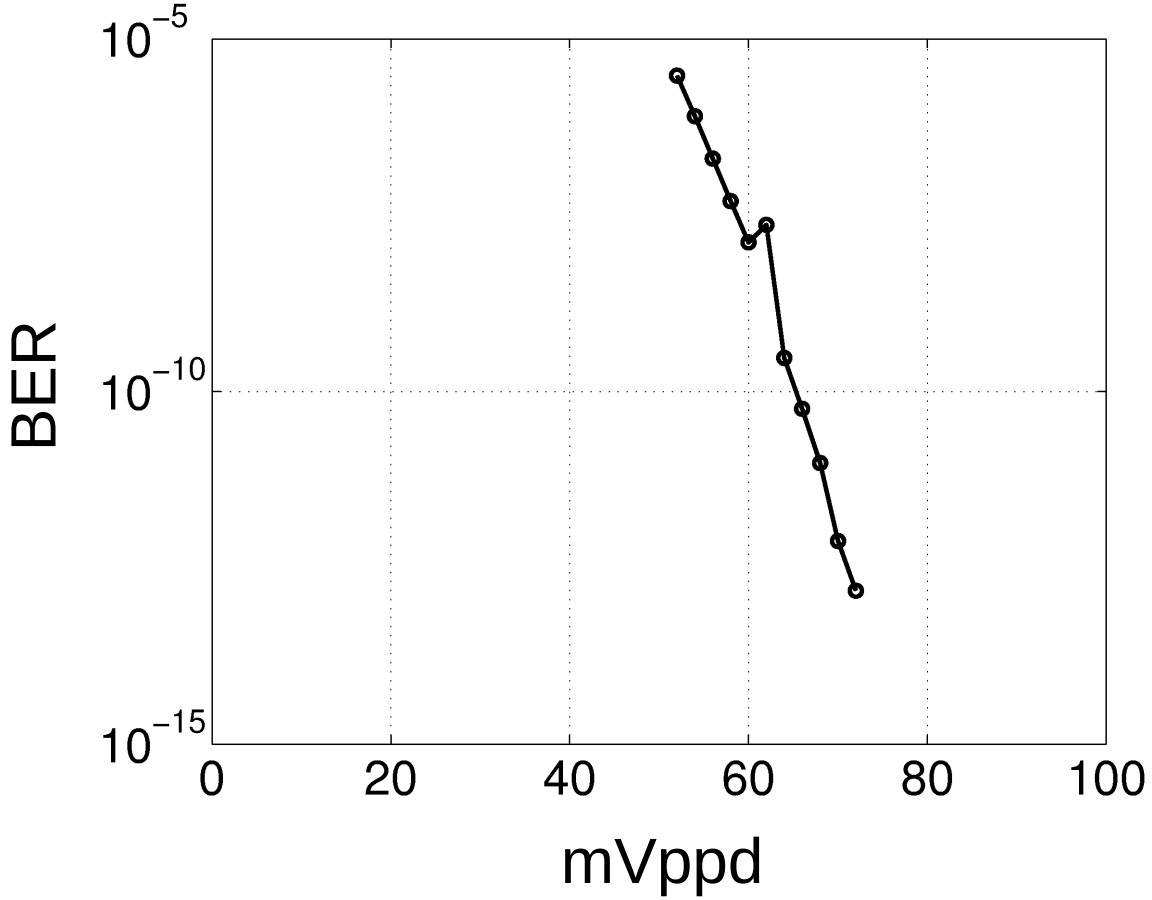
# 30” Backplane response



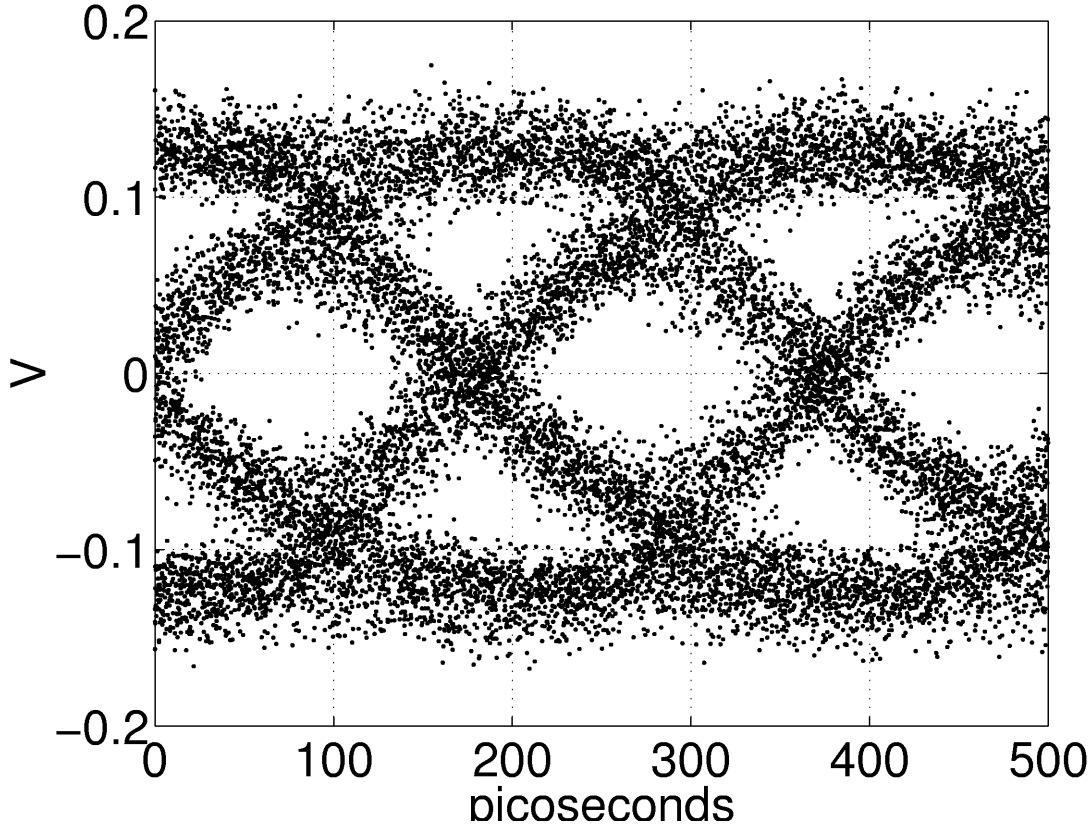

- Completely closed eye at 5Gb/s

# Equalized receiver sensitivity



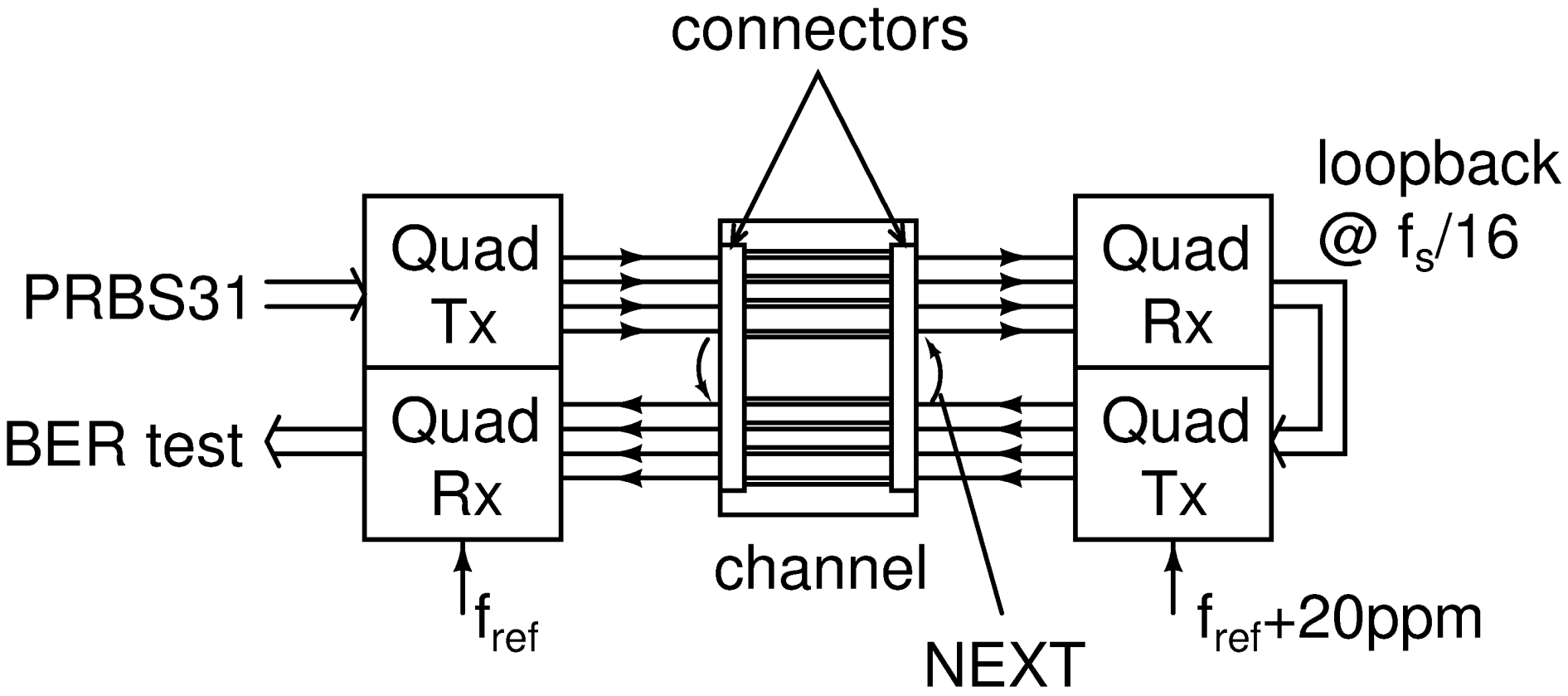

- Data through 30” FR4 backplane to Rx
- No pre-emphasis or FEC

# Transmit pre-emphasis



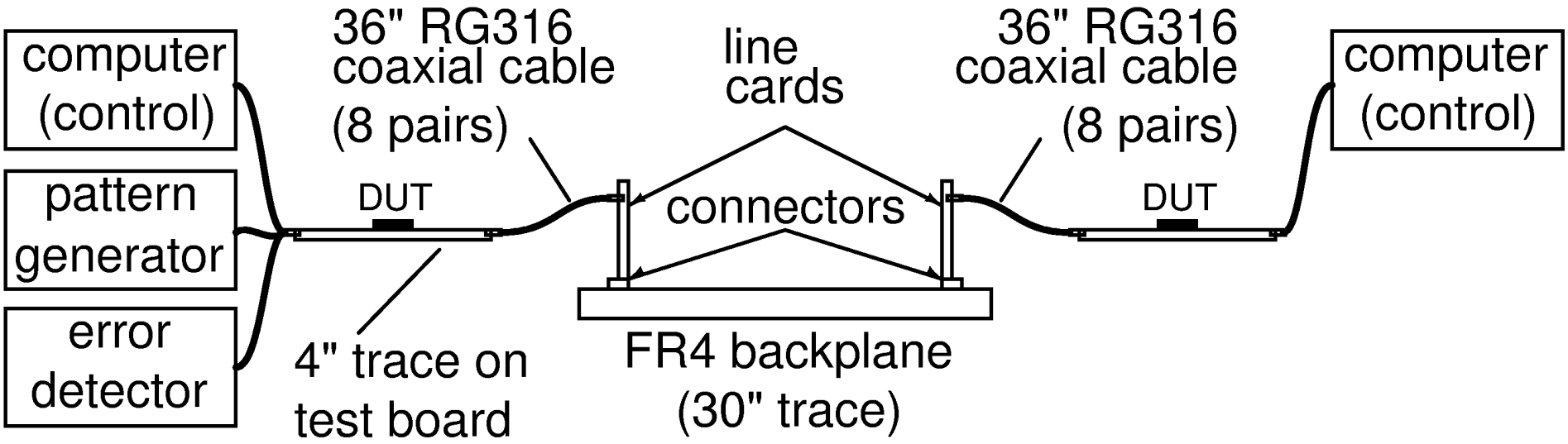

- Tx Data through 30” FR4 backplane
- Pre-emphasis partially opens the eye

# Quad transceiver test setup




- 5.15 Gb/s operation, no FEC
- 30” FR4 backplane, 15m CX4 cable

# Quad transceiver performance




- 5.15Gb/s operation, no FEC
- BER < $10^{-15}$ with 30” backplane
- BER < $10^{-15}$ with 15m CX4 cable

# Performance summary

| | |
|---|---|
| Technology | 0.13µm CMOS |
| Supply voltage | 1.2V |
| Data rate | 5.15Gb/s |
| Power dissipation (4 channels) | 2.1W |
| Chip area, including pads | 12 sq. mm |
| CMU jitter<br>(Tx o/p with a 1010... pattern,<br>Receivers active) | 1.6ps rms |
| Tx total jitter (PRBS31 output) | 4.0ps rms |
| Tx output (programmable) | 200-800mV ppd |
| BER(36” backplane trace<br>+ test board connections) | < 1e-15 |
| BER (15m CX4 cable<br>+ test board connections) | < 1e-15 |
| Rx adaptation time | ~ 200ms |

# Conclusions

- A combination of pre-emphasis, FFE, and DFE can equalize a variety of channels
- The proposed chip enables doubling of data rate over existing channels
- Transmit and receive equalization and FEC can be used individually or in combination for error free transmission in different settings

# Acknowledgments


- Carlos Carvalho, Jose Matos, and Ruben Recinos for layout.
- Thomas Gibbons, Robert Schell, and Robert Schultz for the measurements.