23.2 Dynamically Biased 1MHz Low-pass Filter with 61dB Peak SNR and 112dB Input Range

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In conventional analog filters operated in class-A mode, bias currents are large enough to accommodate the largest expected peak input signal. When only a small input signal (including in-band and out-of-band components) is present, these large bias currents unnecessarily waste power and create noise. A more optimal situation results if bias currents can be dynamically set by the system, depending on the peak value of the total signal being applied or anticipated at the input. However, dynamically varying the bias currents in a filter normally causes unacceptable disturbances at its output. This filter has bias currents that can be varied over several orders of magnitude—for optimum power consumption and noise at each total input signal level—without disturbing the output. Although the filter is internally nonlinear and time-varying, it is externally linear and time-invariant [1].

The chip uses the first-order log-domain filter [2] shown in Figure 23.2.1a as its building block for reasons that will be apparent below. Desired currents are forced into the collectors of the transistors Q_{1p} and Q_{3p} using feedback-controlled current sources I_{fb}. The log-domain filter is linear and time-invariant between the large signal currents i_{1p} and i_{4p} in its input and output transistors (assuming $i_{1p}>0$). The time-domain and frequency-domain relationships between i_{1p} and i_{4p} are given in Figure 23.2.1c. The currents $I_{2,3}$ and the capacitor C_1 determine the dc gain k and the pole ω_p of the filter. The total input current i_{1p} is the sum of a signal current i_{in} and a dc bias I_{bias}. With $i_{in}=0$, the integrated output noise $i_{n,4p}$ (due to collector shot noise of Q_{1p-4p}) is given by the expression in Figure 23.2.1c. The input bias I_{bias} affects the output noise but not the transfer function. I_{bias} can be varied in accordance with the envelope of the input so that it is slightly larger than the minimum required value for i_{1p} to stay positive at all times [3]. Such dynamic biasing lowers the power consumption and the output noise of the filter for small inputs and, at the other extreme, can accommodate large inputs. However, a time varying $I_{bias}(t)$ results in transients in the current i_{4p} of the output transistor Q_{4p}. To overcome this problem, the single-ended filter shown in Figure 23.2.1a is duplicated and operated with the same bias I_{bias} but an opposite input signal $-i_{in}$ as shown in Figure 23.2.1b [4]. Because of the large signal linearity of the log-domain filters the component due to $I_{bias}(t)$ in the two halves of the filter is the same and cancels in the differential output $i_{out}=i_{4p}-i_{4n}$. The relation between i_{in} and i_{out} is linear and time-invariant. At the same time, the use of dynamic biasing accomplishes internal "companding" (compressing/expanding)[1]. A reduction of I_{bias} in Figure 23.2.1 increases the gain (current to voltage) from the input signal i_{in} to the internal voltages - e.g., v_{el}, the emitter voltage of Q_{1p} due to the reduction of the latter's transconductance - of the filter [3, 4] and thus helps maintain an adequate S/N.

A 3rd-order Butterworth filter (based on the RLC ladder in Figure 23.2.2a) with a -3dB bandwidth of 1MHz is fabricated to evaluate the dynamic biasing technique. The RLC prototype is redrawn as an interconnection of 1st-order stages in Figure 23.2.2b. The gain of 2 at the input cancels the 6 dB attenuation of the ladder filter. Figure 23.2.2c shows a simplified picture of the 3rd-order pseudo-differential log-domain filter. Each half of the filter consists of a 3rd-order filter core with logarithmic compression (Q_{1p}) and exponential expansion (Q_{4p}) blocks. The 3rd-order filter core has three stages, each of which is similar to the 1st-order filter core - $Q_{2p,3p}$,$I_{2,3}$ and C_1 - in Figure 23.2.1a.

The dominant source of distortion is the finite output resistance of the bipolar transistors and the current sources. The collector voltage swings of Q_{1p} (and other transistors in the core) are minimized by using a large transconductance in the feedback path around the transistors. A bipolar transistor Q_f driven by a source follower (Figure 23.2.2d) realizes such a large transconductance. An MOS capacitor C_c is used to stabilize the loop. Cascode current sources with long channel MOS transistors are used in the filter to minimize their output conductance and noise. Figure 23.2.3 shows the chip micrograph.

Figure 23.2.4 shows the measured frequency response of the filter for values of the bias current I_{bias} (Figure 23.2.2c) in the range 3μA to 2.5mA. The measured bandwidth is close to 930kHz for all bias currents. There is a small variation in the passband gain when the bias is varied. Although the cutoff frequency and the dc gain of the filter can be tuned (Figure 23.2.1c), there was no need to do so for the measurements presented here. The residual "leakage" of I_{bias} to the differential output due to mismatch is also shown in Figure 23.2.4.

For the following measurements, the bias current I_{bias} is set to twice the amplitude of the single-ended input i_{in} in Figure 23.2.2c, unless that value was less than 3μA, in which case I_{bias} was maintained at 3μA. With such a dynamic biasing arrangement, the measured rms values of the signal and the noise in the differential output are plotted in Figure 23.2.5a vs. the differential input peak. Decreasing I_{bias} decreases the noise, down to 4.4nA rms, corresponding to the smallest I_{bias} of 3μA. Figure 23.2.5b shows measured output signal to noise ratio (S/N), signal to total harmonic distortion ratio (S/D), and signal to 3rd-order intermodulation ratio (S/IM_3, measured with two tones at 980kHz and 1020 kHz) as a function of the differential peak input.

Figure 23.2.6a shows the response of the filter to a 600kHz sinusoid with a differential peak value of 40μA when the bias I_{bias} is switched from 24μA (which is 20% larger than the single-ended peak input) to 114μA. As seen, the output is practically unaffected by transients in I_{bias}. The results in Figs. 23.2.4 and 23.2.6a point to the external time-invariance of the filter in presence of a varying I_{bias}. Figure 23.2.6b shows the current and power consumption of the filter as a function of the differential peak input.

The filter maintains S/N>0 dB and THD < –41dB for total input values ranging over 112dB (Figure 23.2.5b). The filter is not equivalent to a conventional filter with 112dB dynamic range, as the latter would have S/N = 112dB with the largest input. However, it would require orders of magnitude greater power dissipation to achieve this [5].

This dynamically-biased filter is suitable for cases where a modest and a near-optimum power dissipation must be maintained over a large range of input amplitudes. Figure 23.2.7 summarizes measured performance. The chip presented here represents over an order of magnitude improvement in power efficiency compared to previously-published filters.

Acknowledgments:
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References:
[1] Y. Tsividis, "Externally Linear Time-Invariant Systems and their Applications to Companding Signal Processors", IEEE TCAS-II, vol. 44, no. 2, pp. 65-85, Feb. 1997.
[2] M. Punzenberger et al., "A 1.2-V Low Power BiCMOS Class AB Log-Domain Filter", IEEE JSSC, vol. 32, pp. 1968-1978, Dec. 1997.
[3] D. R. Frey et al., "Syllabically Companding Log Domain Filter using Dynamic Biasing", Electron. Lett., vol. 33, no. 18, pp. 1506-1507, 28 Aug. 1997.
[4] N. Krishnapura et al., "Simplified Technique for Syllabic Companding in Log-domain Filters", Electron. Lett., vol. 36, no. 15, pp. 1257-1259, 20th Jul. 2000.
[5] E. Vittoz, "Low power low-voltage limitations and prospects in analog design", in R. J. v. d. Plassche et al., eds., Analog Circuit Design, Low-Power, Low-Voltage, Integrated Filters and Smart-Power, Boston: Kluwer, 1995.

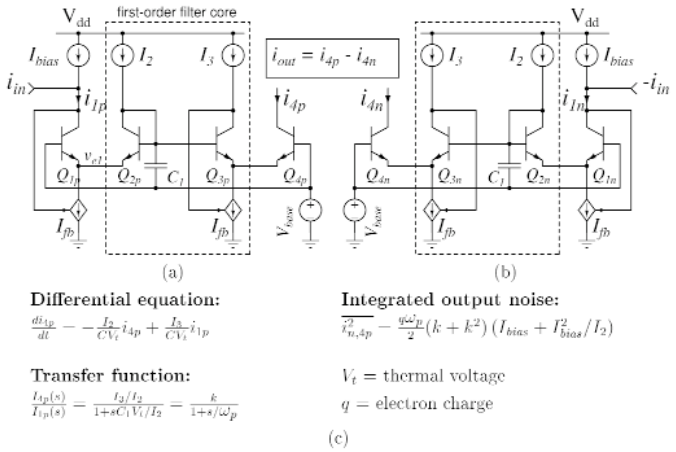


Figure 23.2.1: (a) 1st order log-domain filter, (b) replica, (c) governing equations.

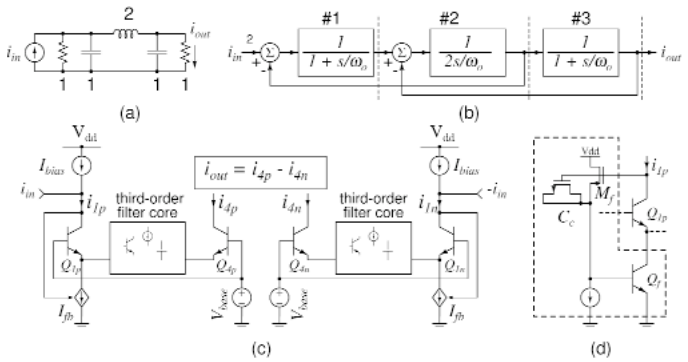


Figure 23.2.2: (a) RLC prototype, (b) block diagram, (c) log-domain realization, (d) feedback circuitry.

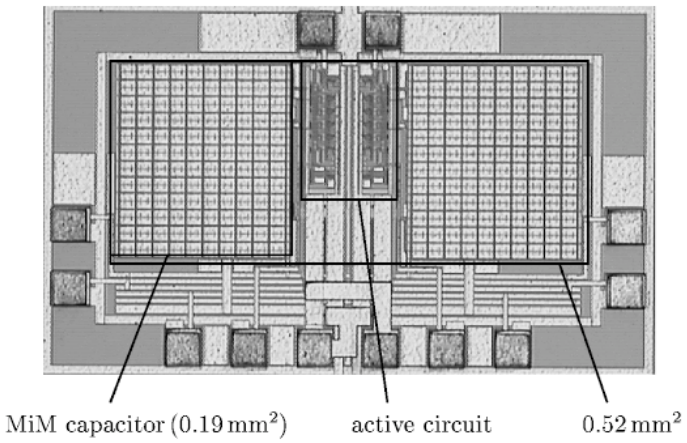


Figure 23.2.3: Chip micrograph.

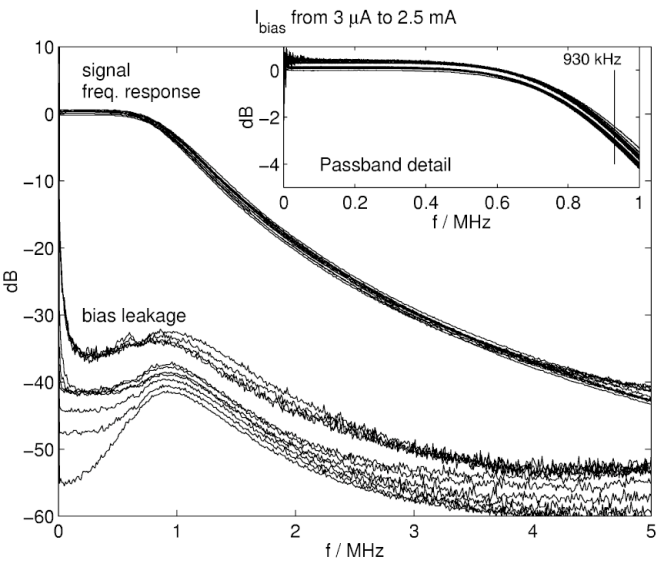


Figure 23.2.4: Measured frequency response.

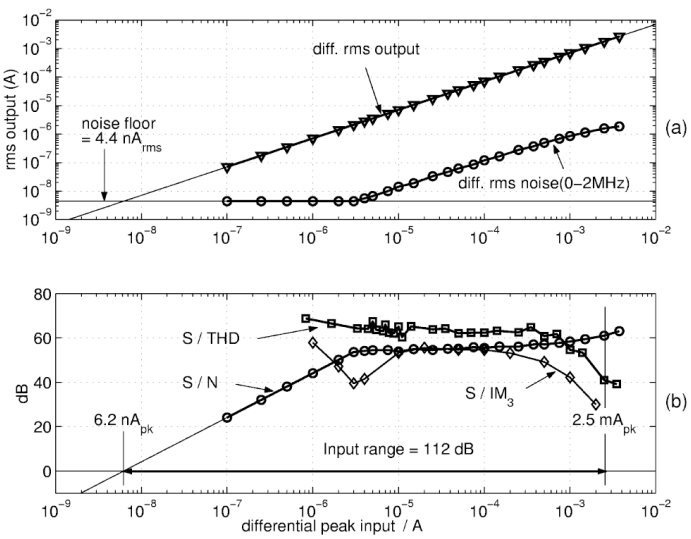


Figure 23.2.5: Measured signal, noise, and distortion.

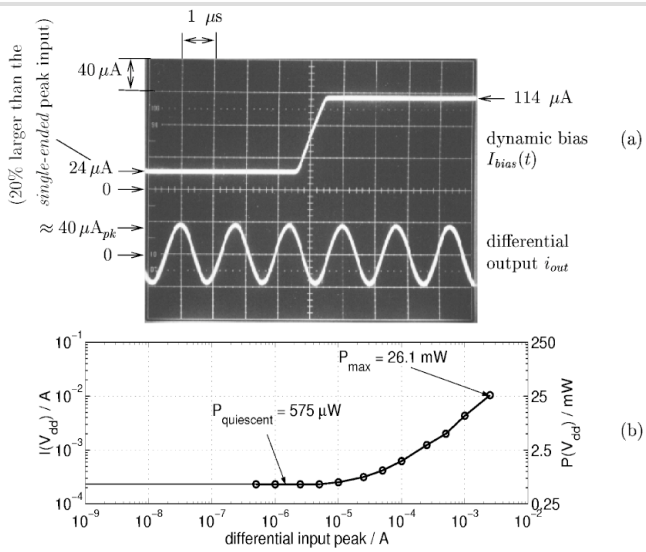
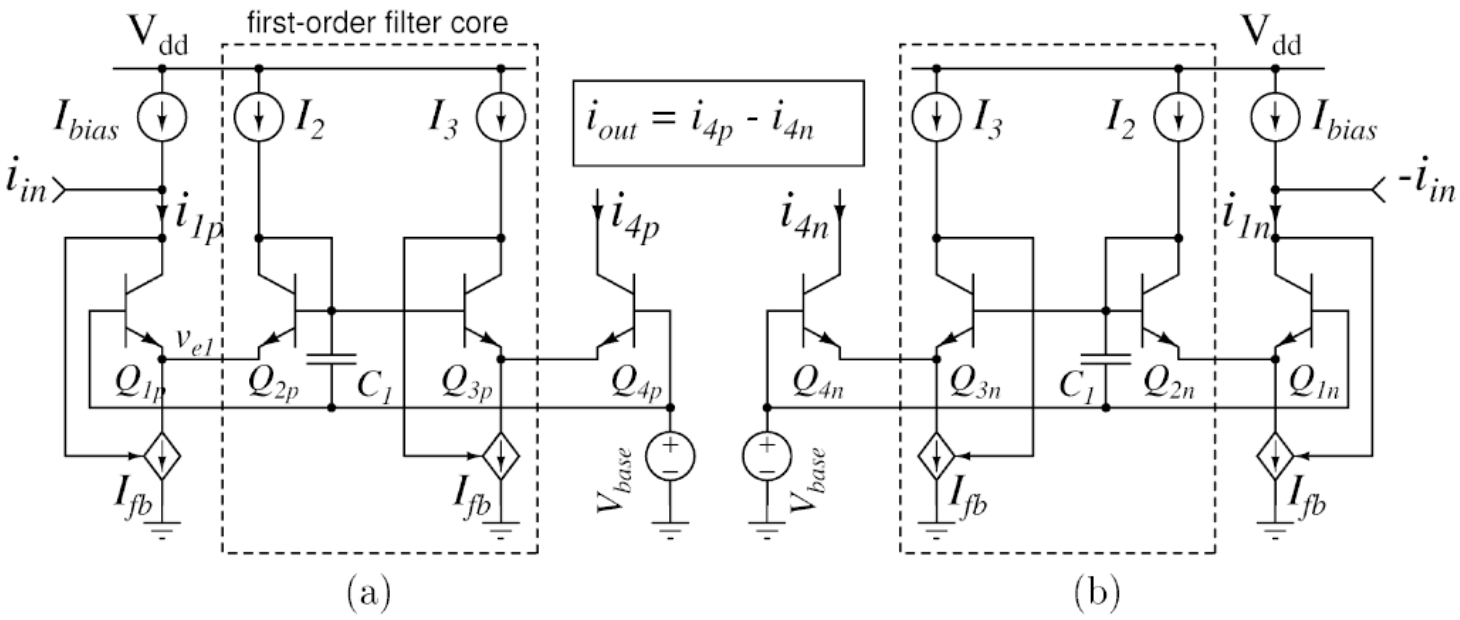


Figure 23.2.6: (a) Differential o/p with a time-varying I_{bias}, (b) power consumption.

Technology	0.25 μm BiCMOS	
Area (excl. pads)	0.52 mm^2	
Supply voltage	2.5 V	
-3 dB Bandwidth (BW)	930 kHz	
I_{bias}	3 μA	2.5 mA
Power diss.	575 μW	26.1 mW
Output noise	4.4 nA	1.5 μA
THD	-64.3 dB	-41 dB
Input range‡ $\mathrm{IR_{dB}}$	112 dB	
$\frac{\text{Max. Power Diss.}}{\text{Order}\cdot\text{BW}\cdot\text{IR}^2}$	5.9×10^{-20} J	

‡Input range: IR, $\mathrm{IR_{dB}}$;
$\mathrm{IR} = I_{max}/I_{min}$, $\mathrm{IR_{dB}} = 20\log_{10}(\mathrm{IR})\}$

Figure 23.2.7: Performance summary and comparison.



Differential equation:

$$\frac{di_{4p}}{dt} = -\frac{I_2}{CV_t} i_{4p} + \frac{I_3}{CV_t} i_{1p}$$

Transfer function:

$$\frac{I_{4p}(s)}{I_{1p}(s)} = \frac{I_3/I_2}{1+sC_1V_t/I_2} = \frac{k}{1+s/\omega_p}$$

Integrated output noise:

$$\overline{i^2_{n,4p}} = \frac{q\omega_p}{2}(k+k^2)\left(I_{bias} + I^2_{bias}/I_2\right)$$

V_t = thermal voltage

q = electron charge

(c)

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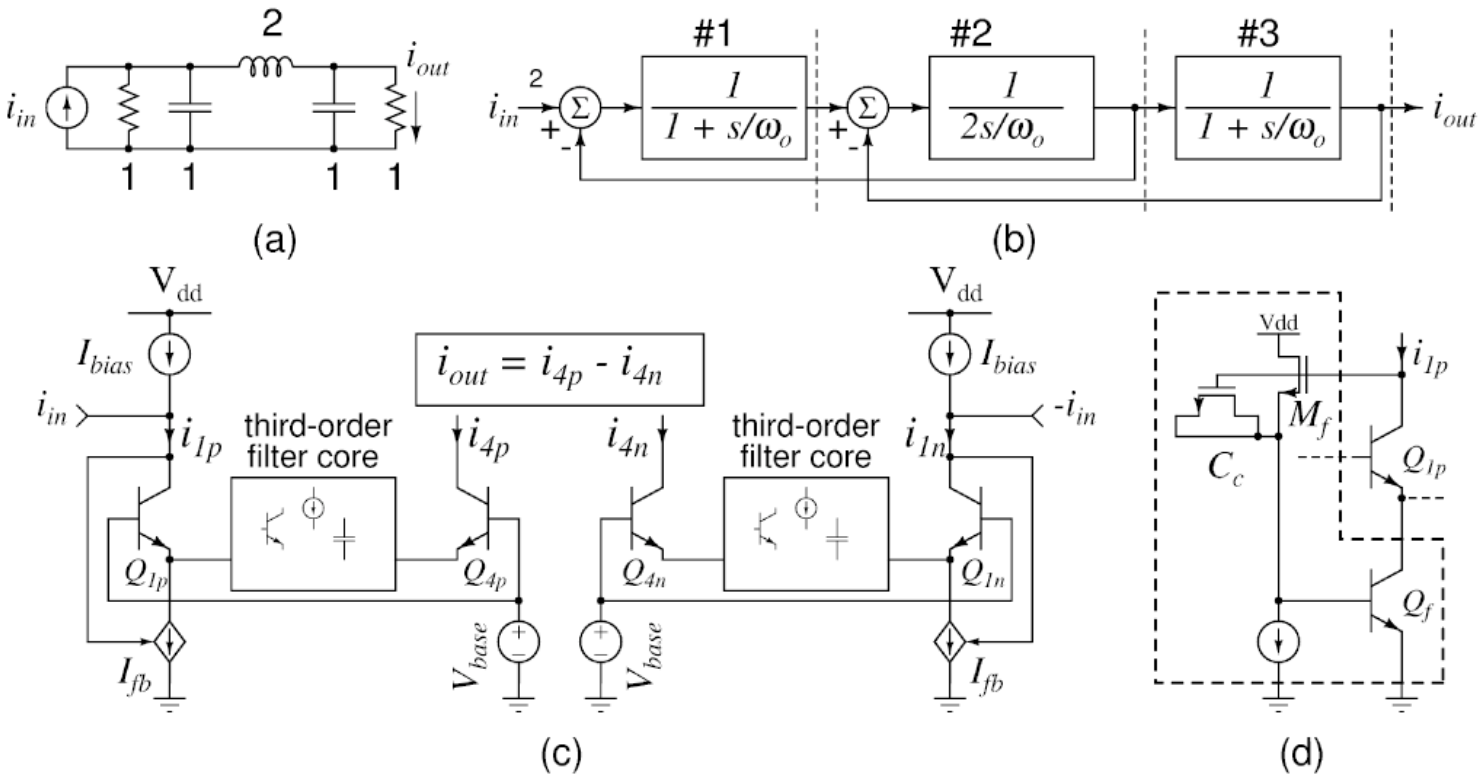

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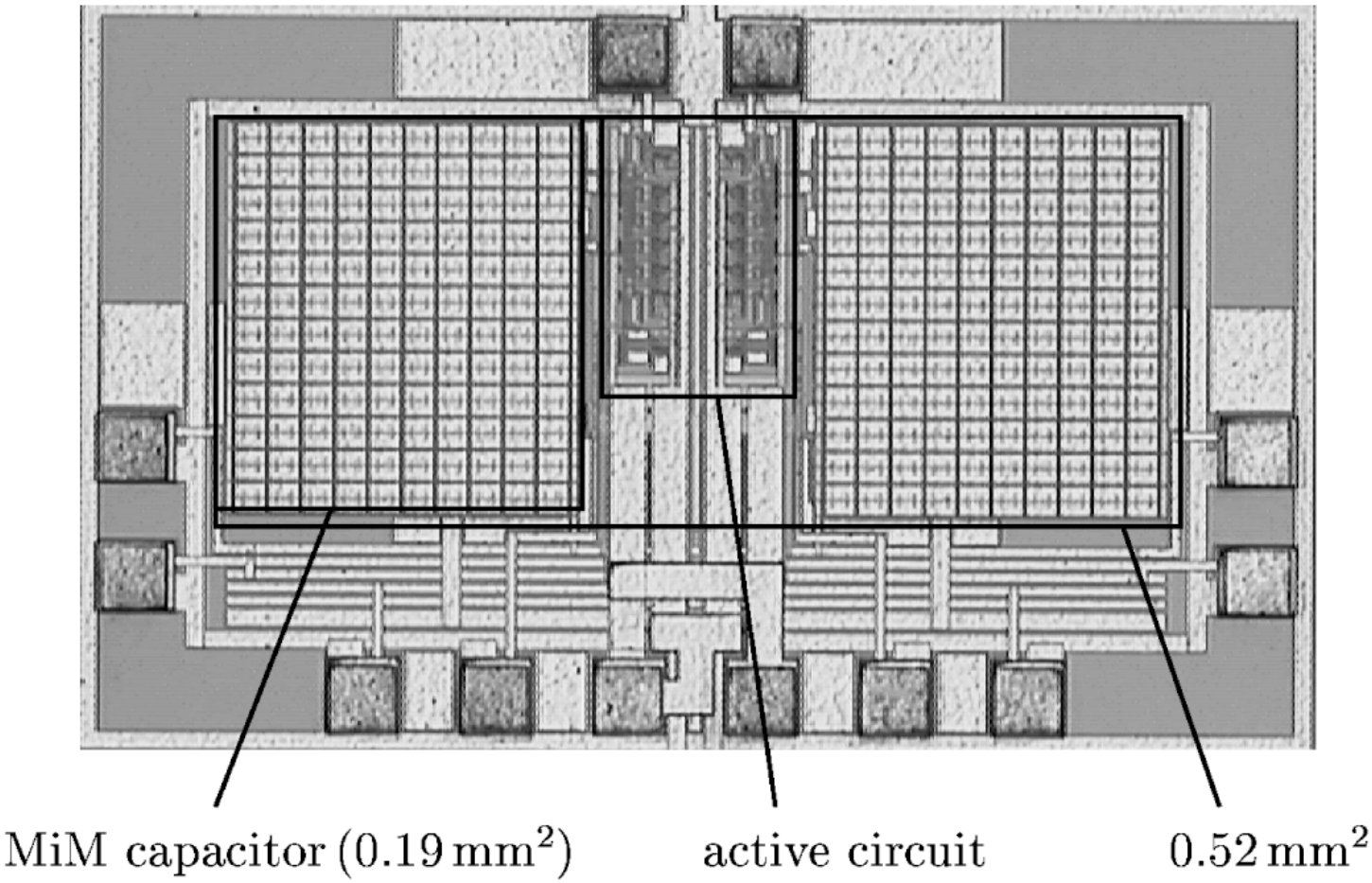

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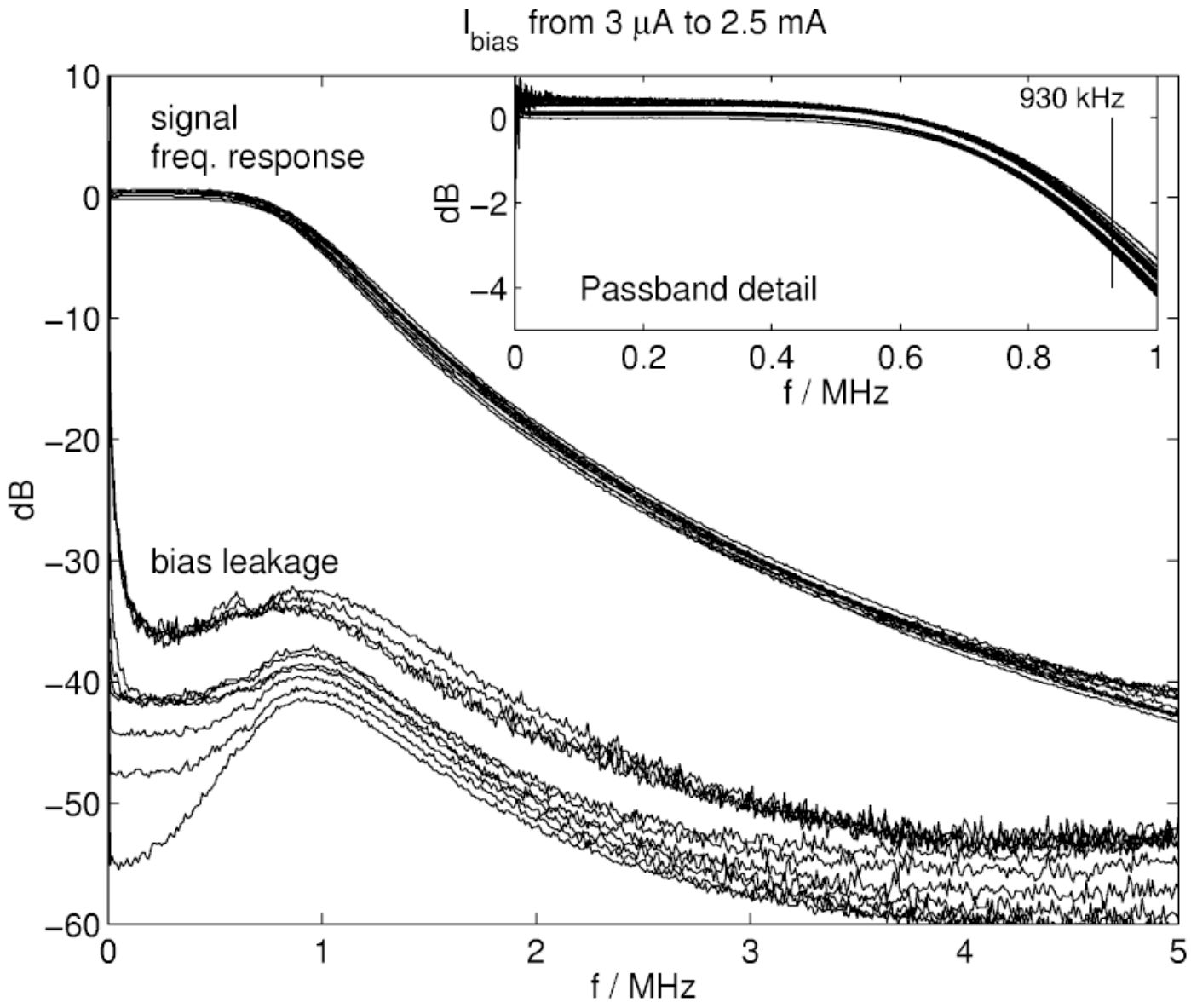

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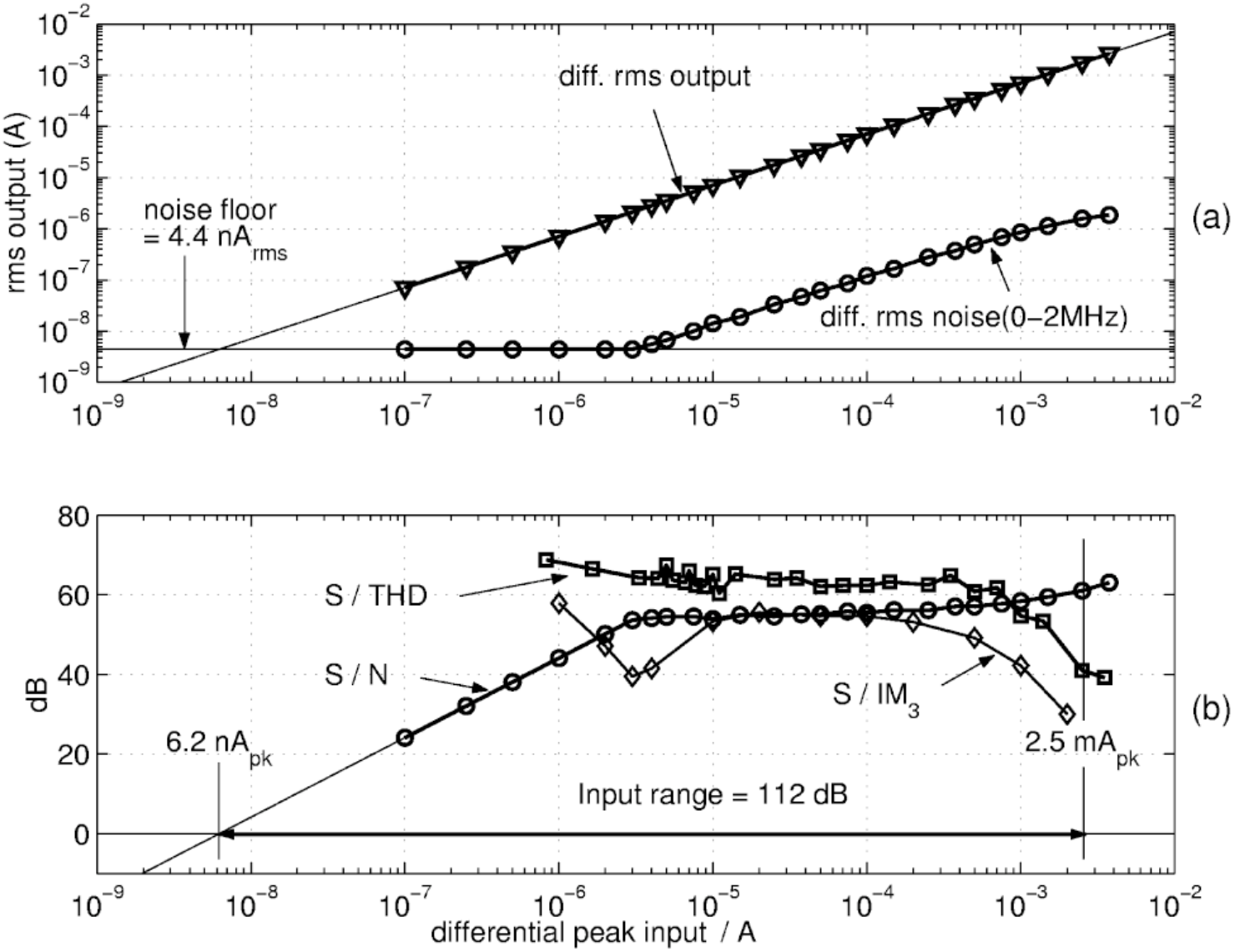

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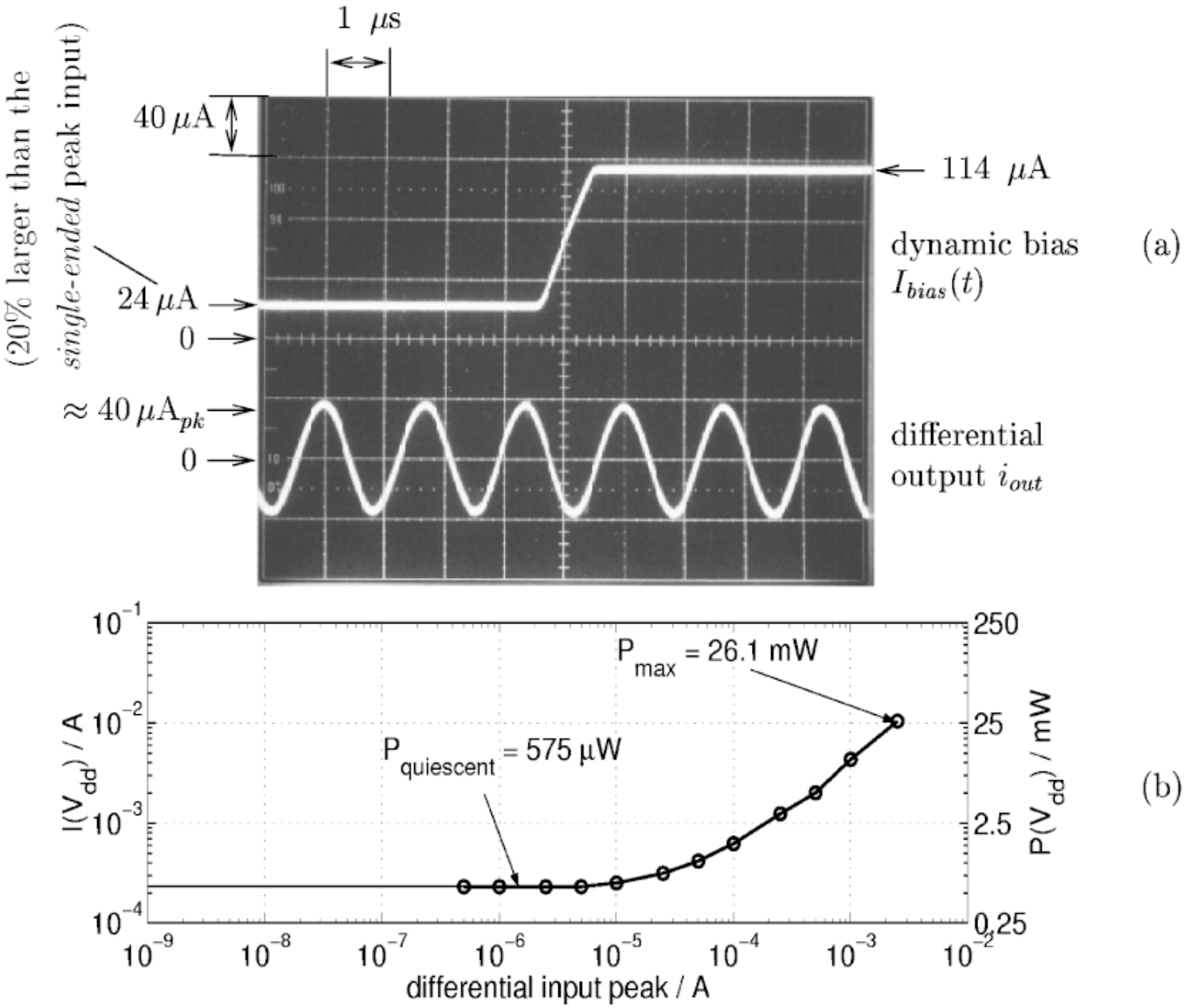

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