Efficient Determination of Feedback DAC Errors for Digital Correction in ΔΣ A/D converters

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Abstract— **Feedback DAC errors in a ΔΣ analog to digital converter are determined by measuring the idle channel output and removing the DAC elements one by one. This method requires simple computation, does not add excess loop delay, and requires no reconfiguration of the ΔΣ modulator. The errors so determined can be used to correct the output codes in the digital domain or the DAC elements in the analog domain. This technique is a useful alternative to the popular dynamic element matching at high speeds as excess delay cannot be tolerated and at low oversampling ratios where DEM can result in tones. Simulation results indicate that the correction values can be obtained to an accuracy that is sufficient to reduce noise and distortion to nearly ideal levels.**

I. MOTIVATION

Multibit ΔΣ A/D converters are capable of a significantly higher in-band signal to quantization noise ratio (SQNR) compared to their single bit counterparts because they have an inherently smaller quantization step and they permit higher out of band gains[1]. They are also less prone to idle channel tones[1]. The single biggest drawback of multibit modulators is the nonlinearity of the feedback DAC which increases distortion and quantization noise in the signal band. Dynamic element matching (DEM) is an effective and popular technique to convert the distortion into shaped noise and significantly improve the in band performance. However, this requires multiple stages of gates or switches in the digital feedback path-e.g. data weighted averaging (DWA) for a 4 bit DAC requires a four stage barrel shifter driven from the accumulated input. Higher order dynamic element matching schemes require more complex computations. For high speed modulators the delay introduced by the DEM logic can be a significant fraction of the sampling period and is best avoided.
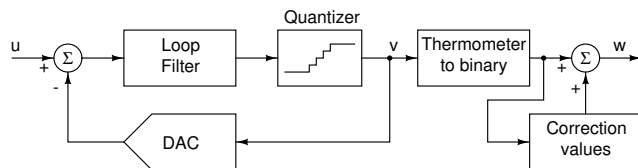

Fig. 1.   Multibit ΔΣ modulator with digital correction

An alternative is digital correction of feedback DAC errors[1] as shown in Fig. 1. Errors in DAC output values from the ideal values are measured, stored digitally, and added to the output of the modulator so that the final digital output accurately corresponds to the analog output of the DAC. In this case, the correction circuitry is outside the loop and does

not contribute to excess delay. To implement this technique, the relative errors between DAC elements must be available in digital form. A possibility is to reconfigure the loop as a single bit modulator[2] and measure all the elements of the multibit DAC against a single element. But this reconfiguration requires modifying the loop filter because a single bit modulator is not stable with the high OBGs typical of multibit modulators, resulting in an overhead in the design of the loop filter and additional simulation effort for verifying the circuit in all modes. To overcome these shortcomings, a method for determining DAC errors using minimal modifications to the ΔΣ modulator is investigated. It is based on observing the output of the modulator with the input set to zero and DAC elements removed one at a time.

The next section describes the prototype system in which the proposed correction techniques are investigated. It turns out that estimating DAC errors is simple and intuitive when the number of quantizer levels is large. Such a case is described in Section III. Section IV describes the more complicated case which occurs when the number of levels is small. Hardware required for implementing the proposed technique is described in Section V. Simulation results demonstrating the technique are given in Section VI.
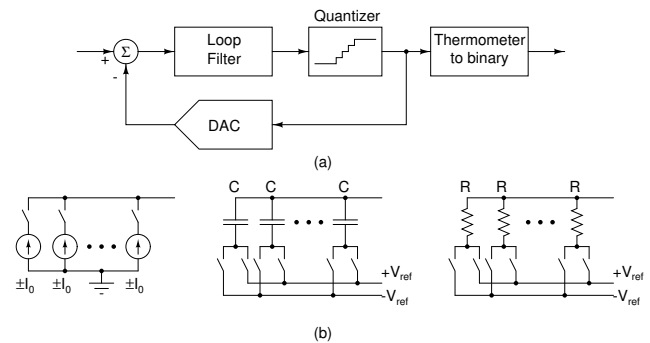
II. EXAMPLE SYSTEM

Fig. 2.   (a) Multibit ΔΣ modulator, (b) Current source, capacitor, and resistor DACs with complementary switching

Fig. 2 shows a ΔΣ A/D converter with multibit feedback. It can be a discrete time or a continuous time modulator. The following assumptions are made:

- The DAC elements—current sources, resistors, or capacitors—are switched in a complementary fashion (Fig. 2). i.e. Based on the digital code, a current source

I_k in a current steering DAC provides a feedback current of $+I_k$ or $-I_k$ or a capacitor in a switched capacitor DAC provides a feedback charge of $+CV_{ref}$ or $-CV_{ref}$. This is the case with most implementations.

- The quantizer's output is thermometer coded. Thermometer to binary conversion is done outside the loop by summing up the thermometer outputs[3].

In the rest of the paper, dimensionless DAC elements with a nominal unit value of 1 and actual values of $D_{1...N}$ are considered. These can represent current sources, capacitors, or resistors. With N elements, the DAC output has $N+1$ possible values with $-\sum_{k=1}^{N} D_k$ (nominally $-N$) for the smallest input code and $\sum_{k=1}^{N} D_k$ (nominally $+N$) for the largest input code. With each increment in the input code, one of the units switches from negative to positive (nominally, a step of 2).

The mismatch between DAC current sources is estimated from idle channel measurements. In the idle state, the quantizer output switches between a few levels, typically three to five, in the middle of the range. Two example systems will be considered:

- 17 levels: There are 16 DAC units $D_{1...16}$. The units $D_{1...6,11...16}$ are not switched in the idle state.
- 5 levels: There are 4 DAC units $D_{1...4}$. Only D_1 and D_4 can be expected to be not switched in the idle state.

The correction value for a given code in Fig. 1 is the cumulative error contribution of all DAC elements for that code. In this paper, we estimate the difference between pairs of DAC elements. These errors can then be summed appropriately to obtain the correction values.

III. PRINCIPLE

The technique presented here is based on observing the idle channel digital output with DAC units removed one at a time. When a particular DAC element is removed, its contribution to the DAC output is zero, instead of being ± 1. In order to obtain the correct digital output, the corresponding input bit to the thermometer to binary decoder is also set to zero in Fig. 2. The digital output V is simply the number of DAC elements that have a positive weight. With zero inputs, the modulator forces the average output of the DAC to be D_{off}, an offset in terms of DAC units which is used to represent the effect of the offset due to the offset of the loop filter and imperfect disabling of the input. The digital output of the modulator, which is the input to the DAC represents the sum of D_{off} and the average nonlinearity contributed by the DAC at that particular output value.

In a 17 level DAC, $D_{1...6,11...16}$ are not switched in the idle state. $D_{1...6}$ contribute with a positive sign and $D_{11...16}$ contribute with a negative sign. First, remove D_1 from the circuit (Fig. 3(a)). When an element is removed, its contribution is zero. Since D_1 does not change its sign, and the DAC output is subtracted from the input, this is equivalent to providing an input of D_1 to the modulator (Fig. 3(b)). The average digital output $V_{av,1}$ equals $D_1 + D_{off} + NL|_{D_1+D_{off}}$ where $NL|_{D_1+D_{off}}$ is the input referred nonlinearity of the DAC at an average output of $D_1 + D_{off}$.
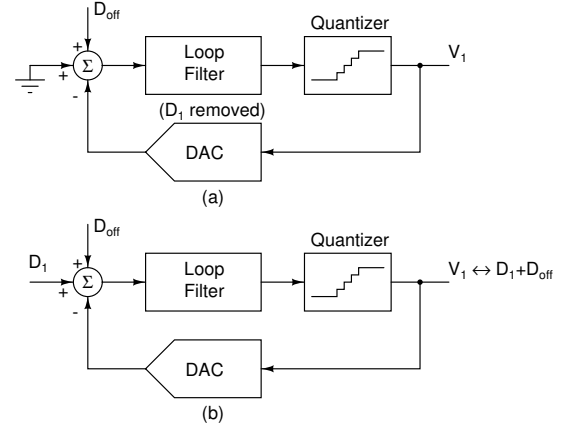

Fig. 3. (a) Idle state with D_1 removed from the DAC, (b) Equivalent picture with an input of D_1 to the modulator and the DAC kept intact.

Next, remove D_2 from the circuit. This is equivalent to providing an input of D_2 to the modulator. The average digital output $V_{av,2}$ equals $D_2 + D_{off} + NL|_{D_2+D_{off}}$ where $NL|_{D_2+D_{off}}$ is the input referred nonlinearity of the DAC at an average output of $D_2 + D_{off}$. Since D_1 and D_2 differ by a very small amount, the nonlinear contributions $NL|_{D_2+D_{off}}$ and $NL|_{D_2+D_{off}}$ can be considered identical to a first order.

Thus, the difference between D_1 and D_2 can be calculated very simply by taking the difference between the corresponding average digital outputs. Similarly difference between successive units from D_2 to D_6 can be calculated.

$$D_{k+1} - D_k = V_{av,k+1} - V_{av,k} \qquad k = 1 \ldots 5 \qquad (1)$$

$D_{11...16}$ are switched negatively in the idle channel. Removing one of them, say D_{11}, is equivalent to driving the modulator with an input $-D_{11}$. Therefore the signs in Eq. 1 have to be reversed.

$$D_{k+1} - D_k = V_{av,k} - V_{av,k+1} \qquad k = 11 \ldots 15 \qquad (2)$$

The differences $D_7 - D_6$ to $D_{11} - D_{10}$ still need to be calculated. For this, a dc offset is added to the input to shift the switching activity to different elements of the DAC. For instance, with the 17 level DAC example above, adding an offset of 8 (4 LSB offset) causes the sources D_{11} to D_{14} to be switched instead of D_7 to D_{10}. This enables calculation of differences $D_k - D_{k-1}$ for $1 \leq k \leq 9$ using the method outlined above. Adding an offset of -8 (-4 LSB offset) causes D_3 to D_6 to be switched and enables calculation of $D_k - D_{k-1}$ for $8 \leq k \leq 15$. Thus, with two values of added offset, all successive differences can be calculated. The added offset need not be very accurate. It is required only to shift the switching activity to a different set of DAC units. Alternatively, the role of "inner" ($D_{5...12}$) and "outer" ($D_{1...4}, D_{13...16}$) elements can be interchanged by changing the connections in the DAC or in the flash quantizer.

IV. WHEN THE NUMBER OF LEVELS IS SMALL

Now consider a 5 level DAC. In this case, the method outlined in the previous section cannot be used. The DAC

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element D_2 switches even with zero inputs. So, removing it is not equivalent to a constant input of $-D_2$. More elaborate calculation is required as shown below.

As before, the outputs are calculated with inputs tied to zero and DAC elements removed one by one. In this case we have to keep track of the average contribution of each DAC element. The contribution of a particular element is $+1$ if it is switched positively and -1 if it is switched negatively. The average contribution of a DAC element is the accumulated contribution of that particular element divided by the number of cycles.

Define v_{kl} to be the average contribution of element l when element k is removed from the DAC. With any element removed, the feedback loop forces the average output of the DAC to be equal to D_{off}. This is expressed by the following equation, written in matrix form for compactness:

$$\begin{bmatrix} 0 & v_{12} & v_{13} & v_{14} \\ v_{21} & 0 & v_{23} & v_{24} \\ v_{31} & v_{32} & 0 & v_{34} \\ v_{41} & v_{42} & v_{43} & 0 \end{bmatrix} \begin{bmatrix} D_1 \\ D_2 \\ D_3 \\ D_4 \end{bmatrix} = \begin{bmatrix} D_{off} \\ D_{off} \\ D_{off} \\ D_{off} \end{bmatrix} \quad (3)$$

Each row relates the average output of the DAC to the average usage of the elements with one element removed. Taking the difference between successive pairs of equations, we get

$$\begin{bmatrix} -v_{21} & v_{12} & v_{13}-v_{23} & v_{14}-v_{24} \\ v_{21}-v_{31} & -v_{32} & v_{23} & v_{24}-v_{34} \\ v_{31}-v_{41} & v_{32}-v_{42} & -v_{43} & v_{34} \end{bmatrix} \begin{bmatrix} D_1 \\ D_2 \\ D_3 \\ D_4 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$
$$(4)$$

Simultaneously solving these equations yields the value of three current sources in terms of the fourth. But it involves difficult operations. Since we are only interested in measuring small differences between nominally identical units, the calculations can be greatly simplified and each equation can be solved separately.

The first step is to rewrite the term $-v_{21}D_1 + v_{12}D_2$ which occurs in the he first row in Eq. 4 in terms of the difference $D_1 - D_2$ and the sum $D_1 + D_2$. Doing so yields

$$\frac{v_{21}+v_{12}}{2}(D_2-D_1) = \frac{v_{21}-v_{12}}{2}(D_2+D_1)+\cdots \quad (5)$$
$$(v_{23}-v_{13})D_3+(v_{24}-v_{14})D_4$$

The DAC units on the right hand side can then be replaced by their nominal value of unity, resulting in

$$\frac{v_{21}+v_{12}}{2}(D_2-D_1) \approx (v_{21}+v_{23}+v_{24})$$
$$-(v_{12}+v_{13}+v_{14}) \quad (6)$$

$v_{21}+v_{23}+v_{24}$ and $v_{12}+v_{13}+v_{14}$ are the average outputs of the DAC with D_2 and D_1 removed respectively.

$$D_2-D_1 \approx 2\frac{V_{av,2}-V_{av,1}}{v_{21}+v_{12}} \quad (7)$$

In general, the difference between successive DAC units is

$$D_{k+1}-D_k \approx 2\frac{V_{av,k+1}-V_{av,k}}{v_{k+1,k}+v_{k,k+1}} \quad (8)$$

$v_{k+1,k}$ and $v_{k,k+1}$ are the average contributions of D_k (with D_{k+1} removed) and D_{k+1} (with D_k removed). Comparing Eq. 7 to Eq. 1 or Eq. 2, we can see that the former has additional terms related to the average contribution of each source when the other is removed. If the units D_{k+1} and D_k do not switch when the other is removed, the weights $v_{k+1,k}$ and $v_{k,k+1}$ both become $+1$ or -1 and Eq. 7 reduces to Eq. 1 or Eq. 2.
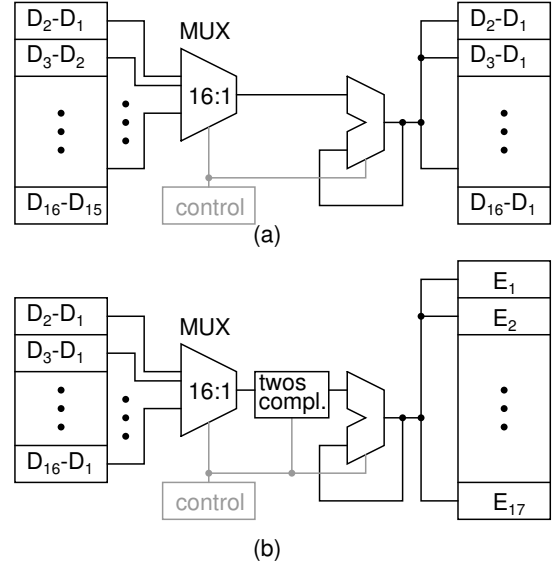
V. IMPLEMENTATION

Fig. 4. (a) Obtaining differences wrt to one of the elements, (b) Obtaining the correction values for each output code

The method outlined in the previous sections result in the difference in the values of successive DAC elements. The average values $V_{av,k}$ and $V_{av,k+1}$ in Eq. 1 and Eq. 2 are simply the output of the decimation filter with the respective DAC elements removed. These values need to be stored and subtracted to obtain the mismatch between successive elements. To obtain the correction values $E_0 \ldots E_N$ for each output code from these, two steps are required. First, the errors of all DAC elements are computed with respect to one of the elements, say the first one, by appropriately summing the differences between successive elements.

$$D_k-D_1 = (D_k-D_{k-1})+(D_{k-1}-D_{k-2})+\ldots+(D_2-D_1) \quad (9)$$

Subtracting $D_k - D_1$ from D_k for $k = 2 \ldots N$ make all the DAC units equal to D_1. Since the output of a complementary switched DAC goes from the negative sum of all units to positive sum of all units, with one unit changing sign at each step (Section II), the correction values $E_0 \ldots E_N$ (for output codes $0 \ldots N$ respectively) are given by the expression below

$$\begin{bmatrix} E_0 \\ E_2 \\ \vdots \\ E_N \end{bmatrix} = \begin{bmatrix} -1 & -1 & \ldots & -1 \\ +1 & -1 & \ldots & -1 \\ \vdots & & & \\ +1 & +1 & \ldots & +1 \end{bmatrix} \begin{bmatrix} 0 \\ D_2-D_1 \\ \vdots \\ D_N-D_1 \end{bmatrix} \quad (10)$$

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Circuits required to implement Eq. 9 and Eq. 10 are shown in Fig. 4. The summation in Eq. 9 is done using an appropriately controlled MUX and accumulator as shown in Fig. 4(a). Eq. 10 can be implemented as shown in Fig. 4(b) by summing mismatch values with appropriate signs. The hardware required is the same as in Fig. 4(a) with the addition of a 2's complement generator. Since the operations in Fig. 4(b) are done after those in Fig. 4(a), the same hardware can be used for both. Three sets of registers are required to store difference between successive values, difference wrt to a single element, and correction values for each output code. Once the errors are determined and the correction values stored, these circuits are inactive.

The number of cycles required for averaging depends on the desired accuracy after correction and total qunatization noise of the modulator (which has to be filtered by averaging). Once a desired degree of filtering is achieved, the accuracy to which the DAC units are measured is limited by the nonlinearity of the $\Delta\Sigma$ modulator (i.e. $NL|_{D_2+D_{off}}$ and $NL|_{D_2+D_{off}}$ are not quite identical as assumed in section III). The correction values obtained by the first correction can be used to linearize the modulator. The process of removing DAC elements one by one and measuring successive differences can be repeated with this improved modulator. In this manner, the correction values can be progressively refined.

When the number of elements is small, the average usage of each element has to be tracked. This can be accomplished by a counter whose clock is gated by the thermometer code output corresponding to that element. Eq. 8 requires a division operation. Since this has to be done only once for each element, compact hardware that takes many cycles to complete can be used.

have errors with $\sigma = 0.003\,\mathrm{LSB}$. The $\Delta\Sigma$ modulator is driven with a sinusoid with an amplitude of half the full scale. Fig. 5(a) and Fig. 5(b) show the output spectra for the ideal case and in presence of DAC nonlinearities. The latter shows an increased noise floor and significant distortion. Fig. 5(c) shows the output spectrum after obtaining the correction values once. The noise level is nearly down to the ideal level. Distortion is reduced significantly, but still visible above the noise floor. Fig. 5(d) shows the output spectrum after determining the correction factors for a second time with the improved modulator as described in the previous section. The noise and distortion are down to ideal levels. The results are summarized in Table I. The last column shows the standard deviation of DNL of the DAC. It is reduced by about an order of magnitude in each correction step. Table I shows the results of simulation of a modulator with an $OSR = 64$. A similar improvement is seen in the noise and distortion performance.

TABLE I

Results for OSR=16, OBG=3, 17 levels

	SNR	HD$_2$	HD$_3$	σ_D
Ideal	83.0 dB	—	—	—
Without correction	78.4 dB	-60.2 dB	-69.7 dB	3×10^{-3}
With correction	82.9 dB	-84.6 dB	-91.1 dB	1.6×10^{-4}
With refined correction	83.1 dB	—	—	1.5×10^{-5}

Results for OSR=64, OBG=3, 17 levels

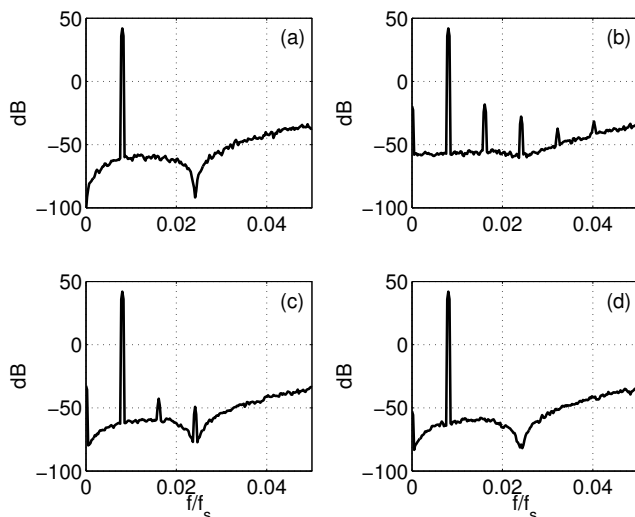|	SNR	HD$_2$	HD$_3$	σ_D
Ideal	122.6 dB	—	—	—
Without correction	82.6 dB	-60.1 dB	-69.8 dB	3×10^{-3}
With correction	112.3 dB	-87.7 dB	-93.7 dB	1.2×10^{-4}
With refined correction	122.0 dB	-111.6 dB	-121.9 dB	1.2×10^{-5}

VI. SIMULATION RESULTS

Fig. 5. $\Delta\Sigma$ modulator output spectrum showing performance improvement with digital correction: (a) Ideal, (b) Without correction, (c) After first correction, (d) After refining the correction values

The ideas outlined above are tested with a $\Delta\Sigma$ modulator with $OSR = 16$, $N = 17$, $OBG = 3$. The DAC elements

VII. CONCLUSIONS

An efficient method for estimating errors in the feedback DAC for digital correction in $\Delta\Sigma$ modulators is proposed. This requires no reconfiguration of the modulator loop. This technique also does not require switches in the signal path that can add to excess loop delay in continuous-time $\Delta\Sigma$ modulators (For example, with a current steering DAC, an element can be removed by setting the bias voltage of the current source to zero). The technique is based on removing one of the DAC elements of a $\Delta\Sigma$ A/D converter and measuring its value using the same $\Delta\Sigma$ A/D converter. The measurment accuracy of DAC units is limited by the nonlinearity of the converter, but can be refined by repeated measurements after applying the correction values from the previous step. Simulation results prove the efficacy of the proposed technique in lowering the noise floor and distortion levels.

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