A 5.3 GHz Programmable Divider for HiPerLAN in 0.25μm CMOS

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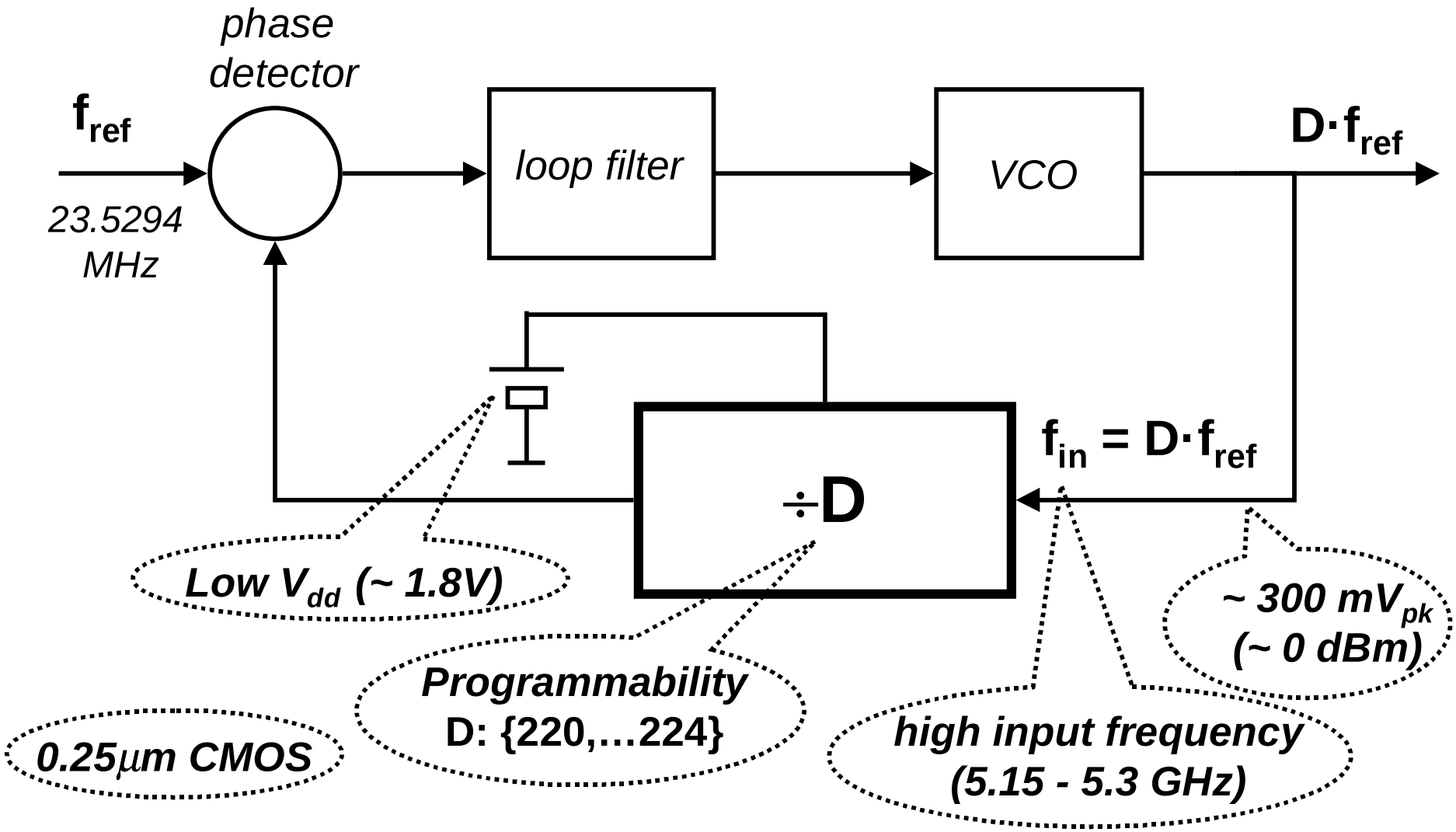
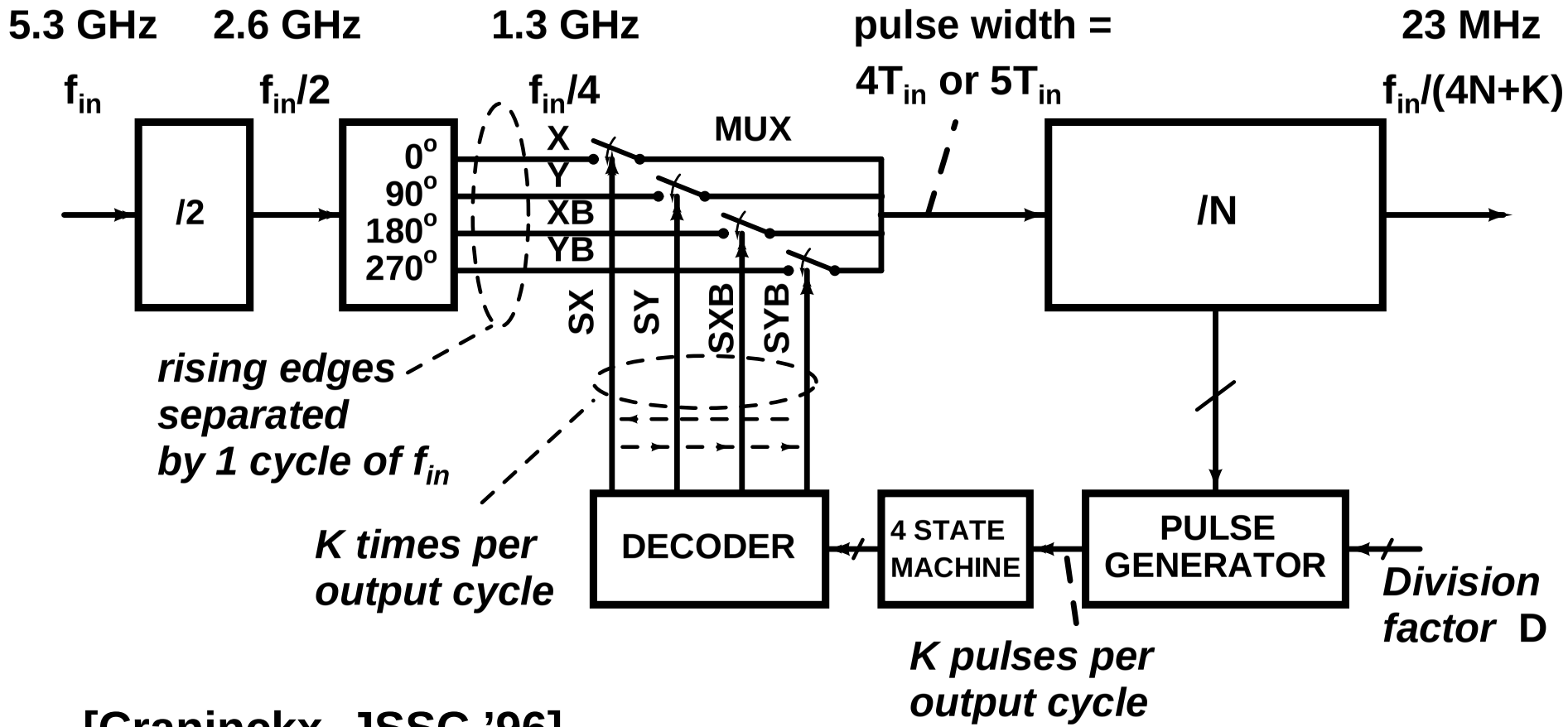
Programmable divider for a HiPerLAN carrier synthesizer(5 channels)



Outline

- Divider architecture:
  - Phase switching.
  - Timing issues.
  - Solution: Signal retiming.
- Circuit implementation:
  - High speed ÷2(D-Flip Flop) stage.
- Measurement results.
- Comparison & conclusions.

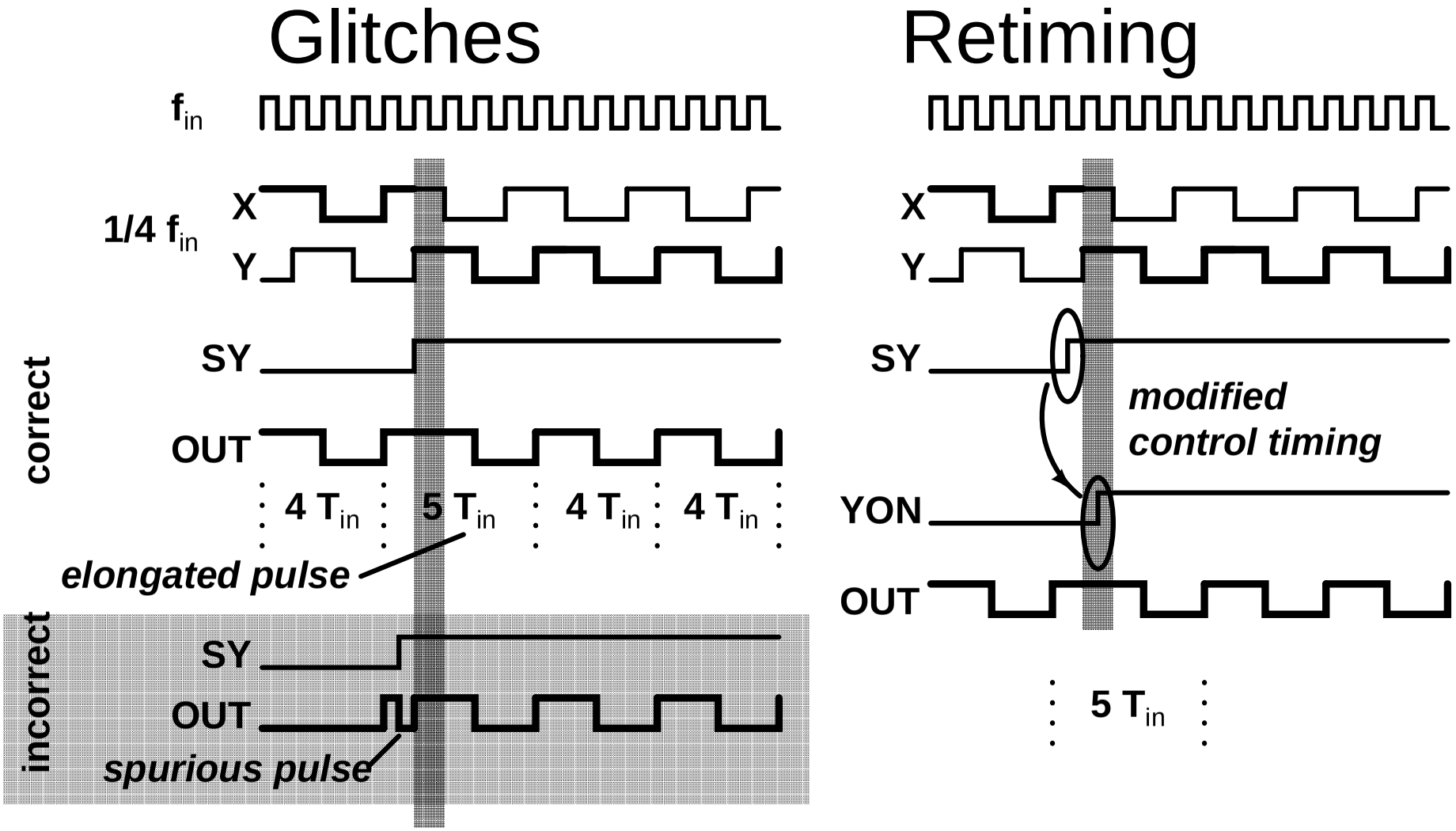
Phase switching divider



[Craninckx, JSSC '96]

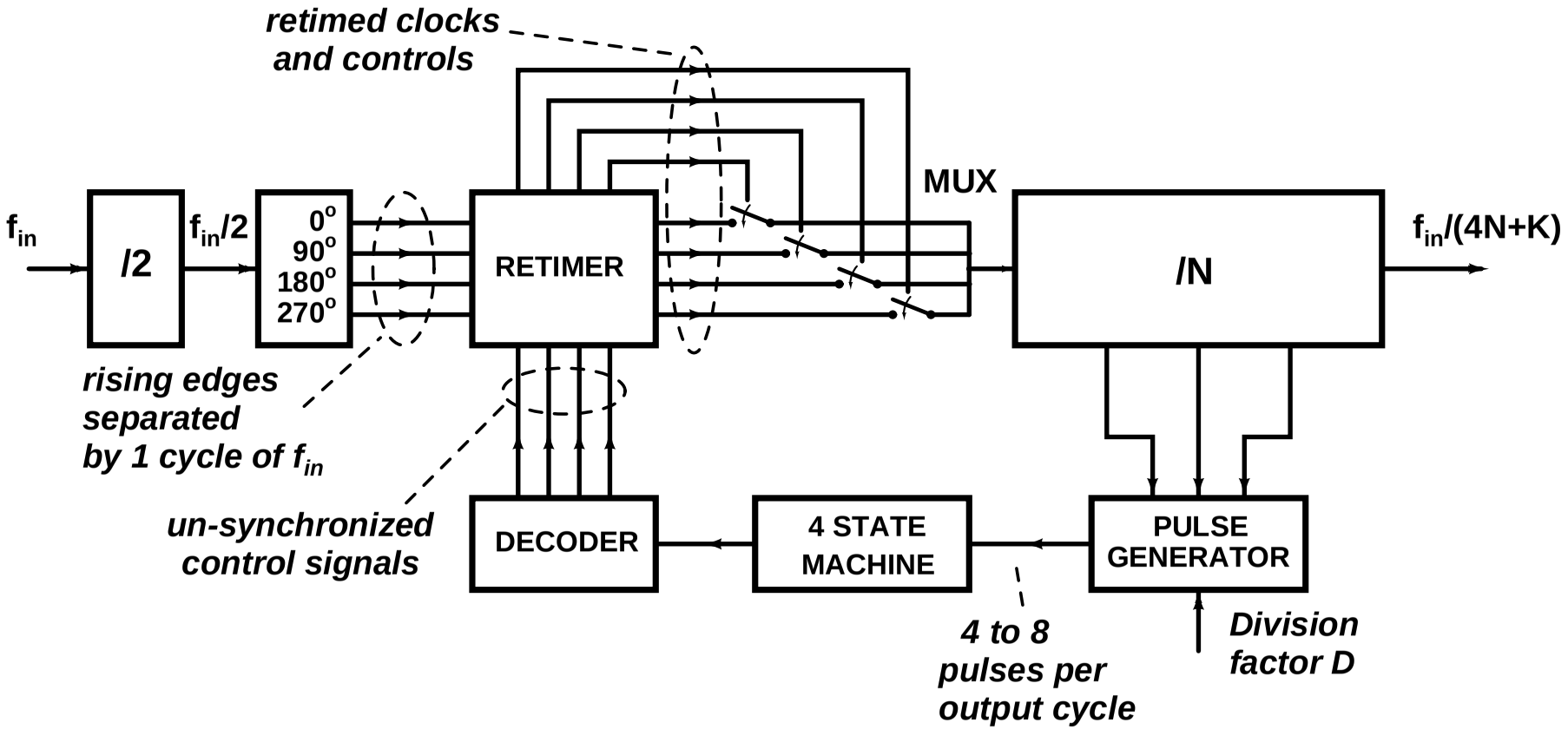
- K phase switches per output cycle: ÷ (4N + K)

\+ No high speed feedback loops around multiple flip-flops.



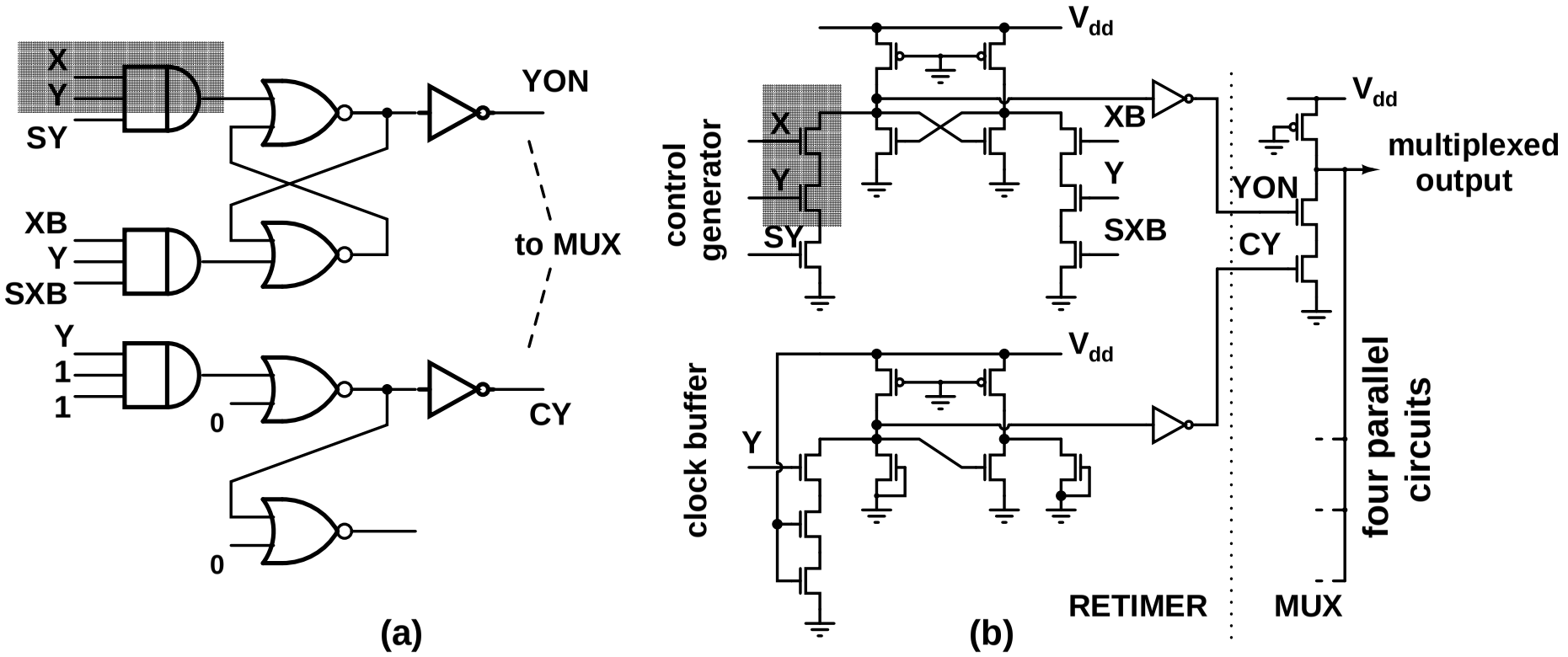
- clock-X to clock-Y when both X & Y are in the same state.
- Retimer circuit: enforces control timing for each of the four possible clock transitions.

Phase switching divider with retiming



- Retimer inserted after the second stage.

Retimer: Implementation

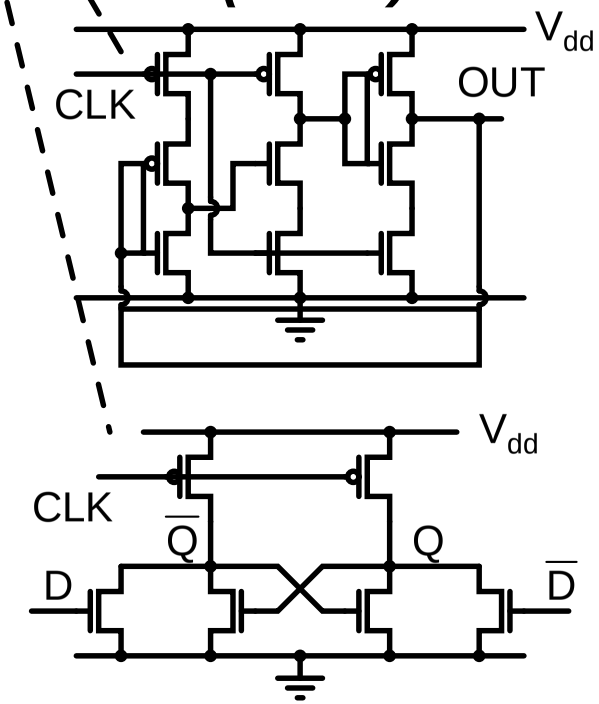


- New control generated when both clocks are high.
- Clock and control go through identical paths.
- Feedforward operation $\Rightarrow$ high speed.

High speed ÷2 stages / latches

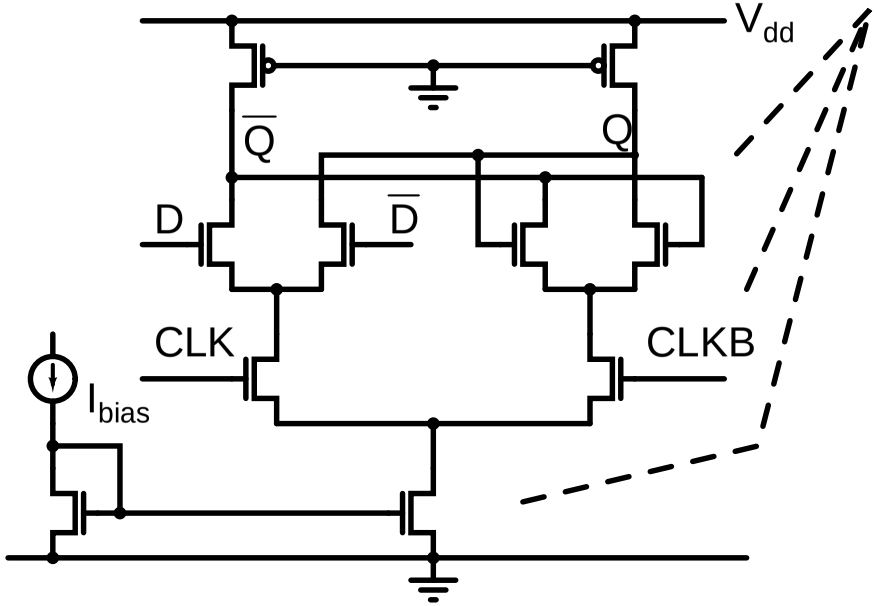
pMOS in signal path

(TSPC)



(Razavi '95)

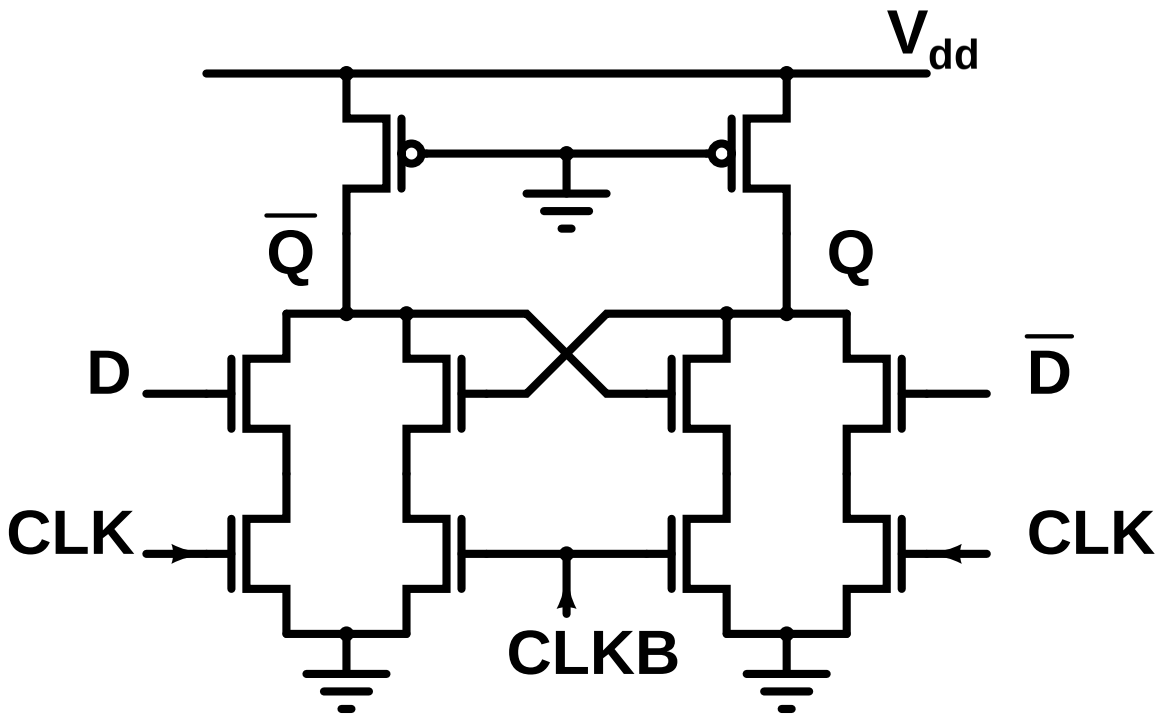
stacked devices
too little headroom



(source coupled logic)

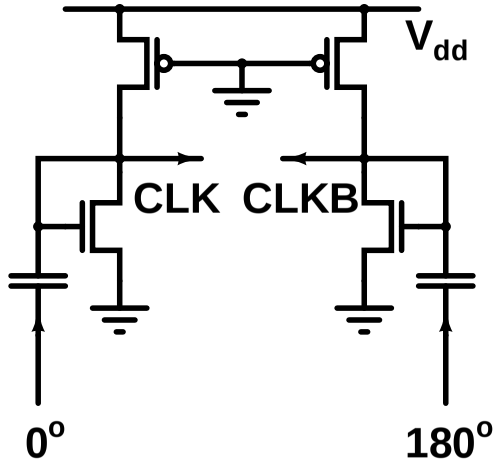
- Goals: Low V_{dd}(1.8 V) & high speed(5.5 GHz)
- pMOS: much smaller drive than nMOS.

Pseudo-nMOS low voltage latch

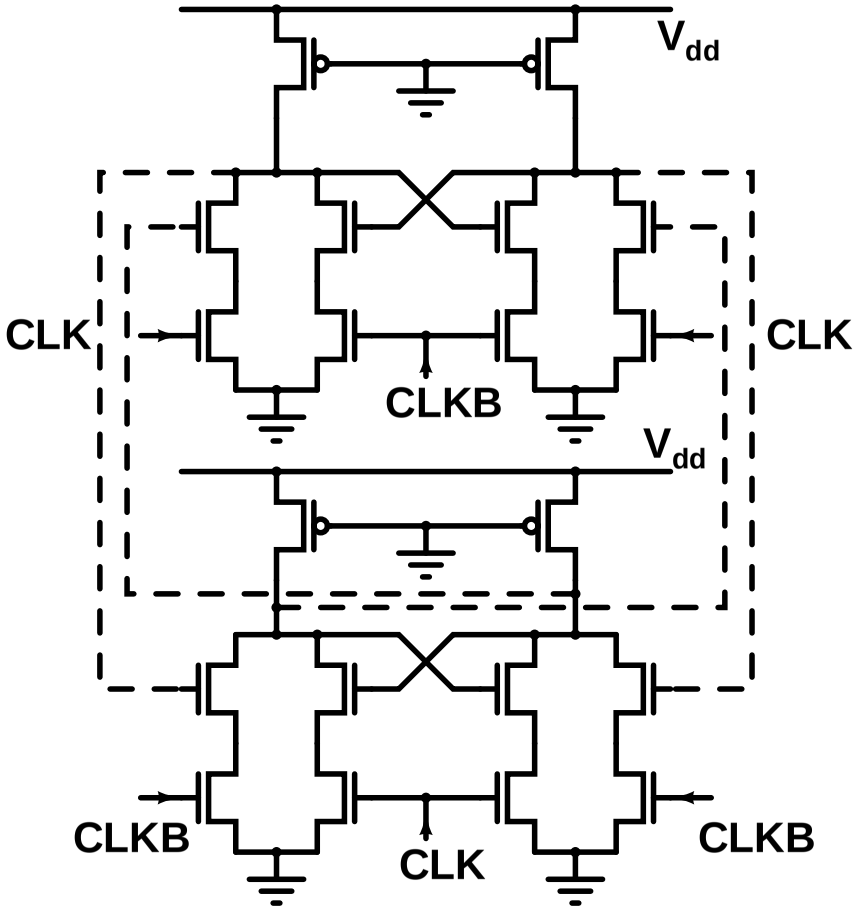


- 0.25μm CMOS, V_{dd} = 1.8 V: 3 stage ring osc.
  - CMOS: 2.8 GHz.
  - pseudo-nMOS: 6 GHz.

5.5 GHz ÷2 stage

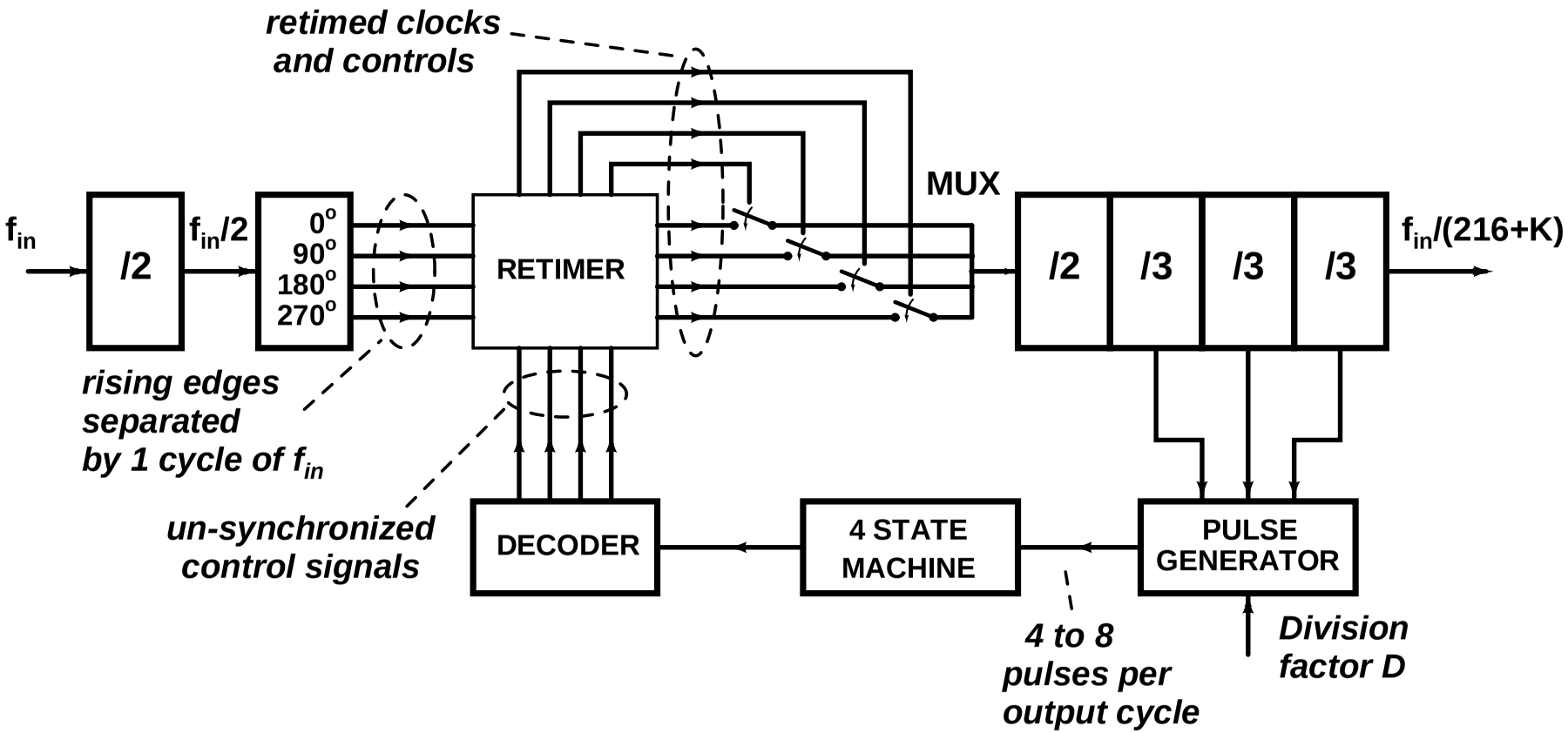


input ac coupling



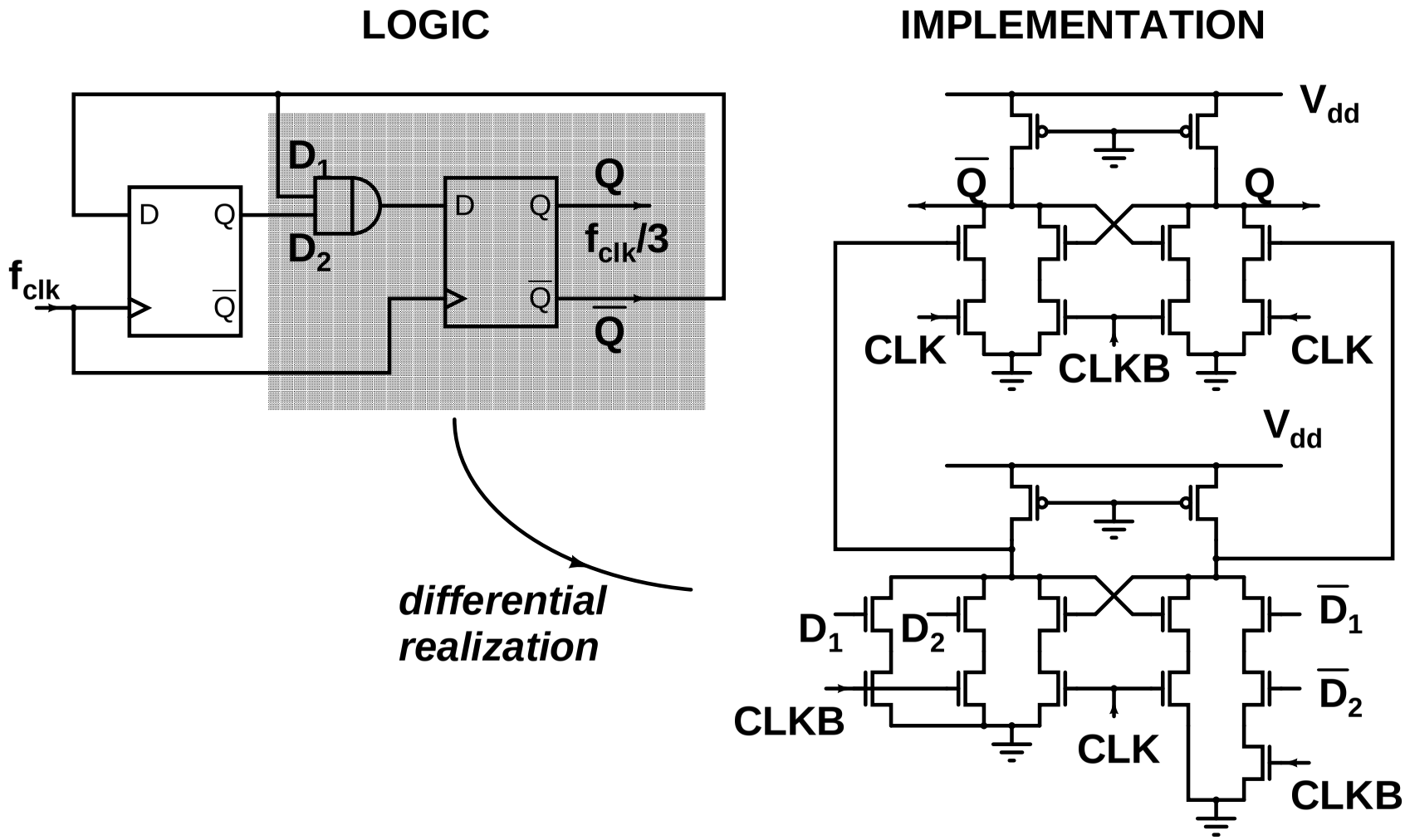
- 5.5 GHz ÷2 with 300mV$_{pk}$ (SE) inputs at V$_{dd}$ = 1.8V.
- Disabled by pulling CLK, CLKB inputs to the rails.

Programmable divider



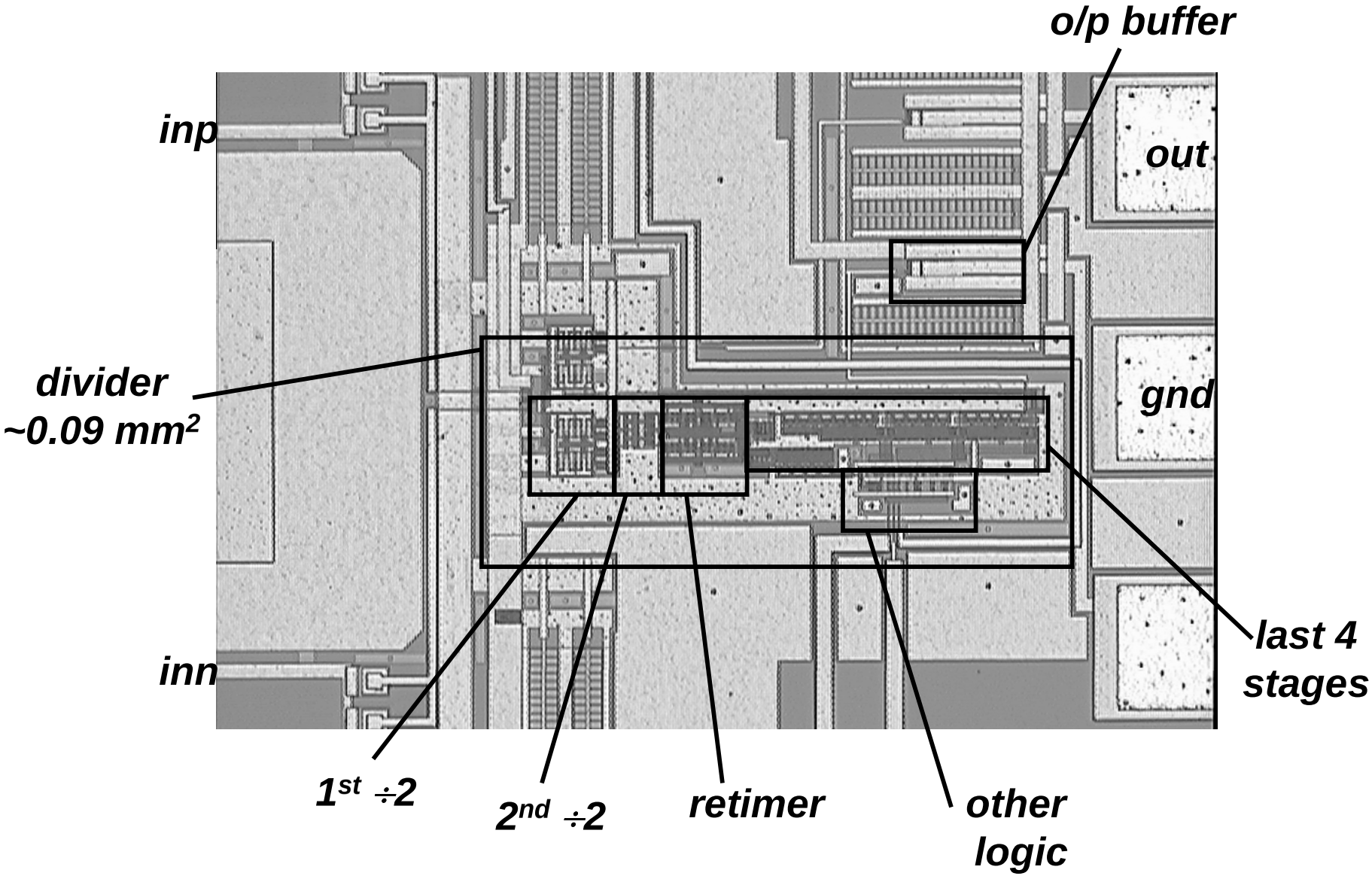
- {220, …, 224} = 216 + {4, …,8} $= 2^3 \cdot 3^3 + \{4, \ldots,8\}$
- ÷3 stages-similar to ÷2, with gated input branches.

÷3 stage

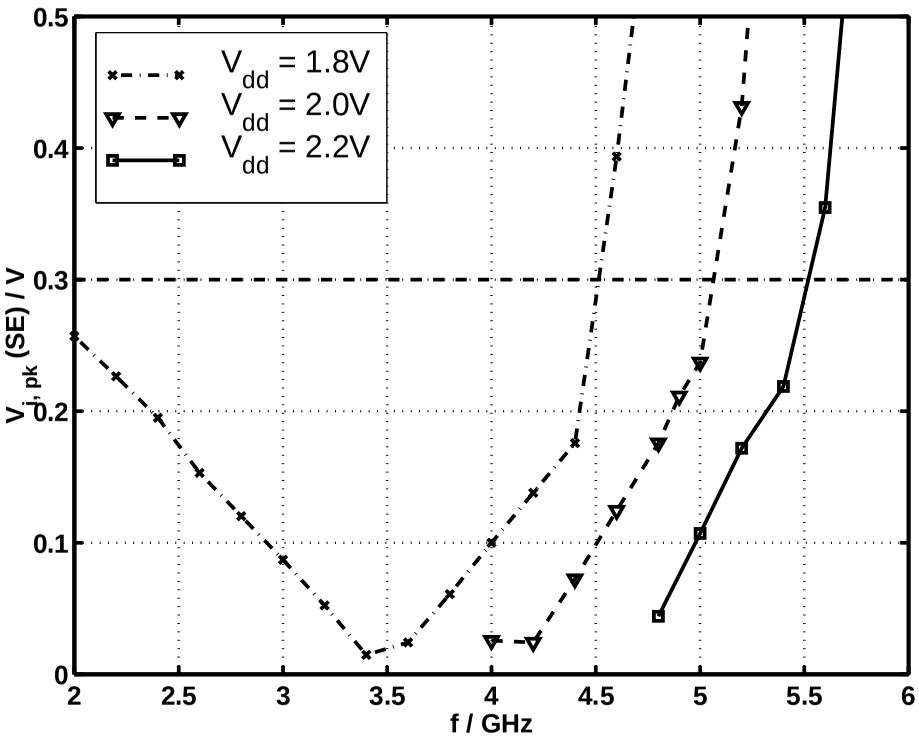


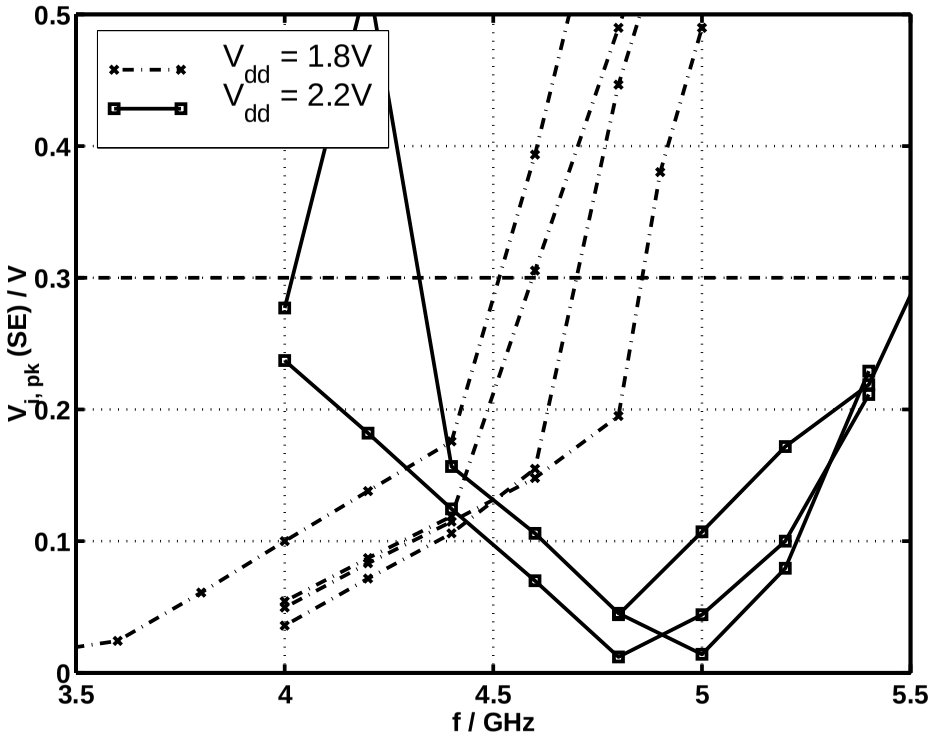
- AND gate: combined with the DFF input branches.

Chip Photograph



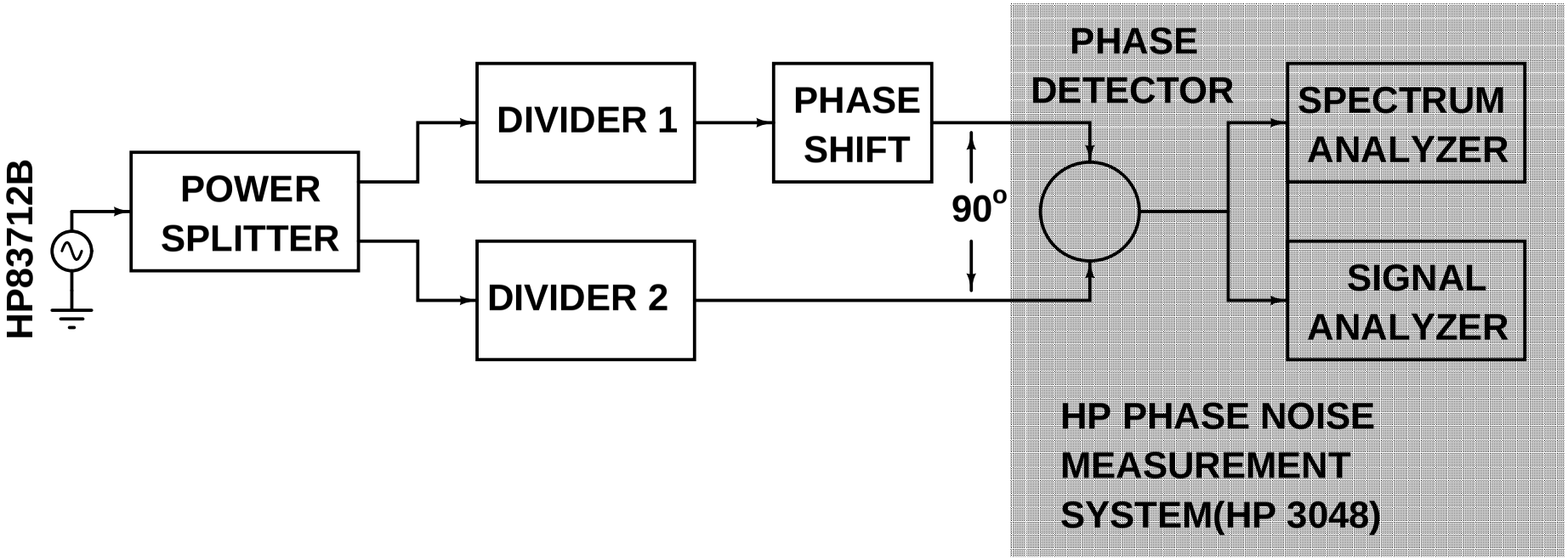
Measurements: Sensitivity





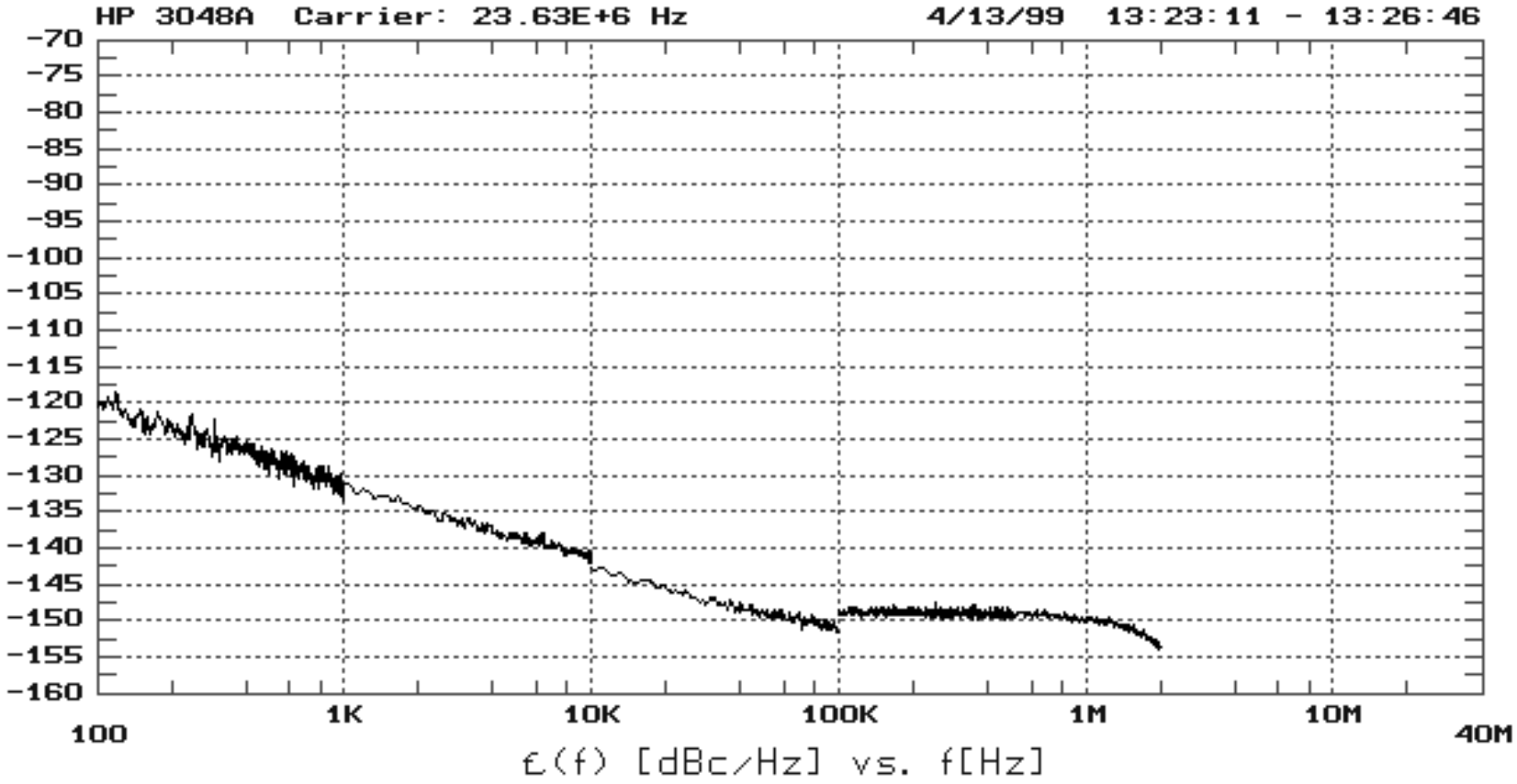
- 5.5 GHz operation with V_{dd} = 2.2 V, 300mV_{pk}(SE) input.
- Changed technology: major discrepancy between models and process.

Phase noise measurement setup



- Divider contributes phase noise inside the loop bandwidth.
- The inputs to the phase detector are 90^{o} apart.
- Measured noise = 3 dB + noise of each divider.
- Input referred phase noise(@ 5.5 GHz): + 47dB (220x).

Measurements: Phase Noise



- o/p phase noise from 2 dividers & o/p buffers.
- ~ -131 dBc/Hz @ 1 kHz offset.
- 1/f behavior down to 1Hz.

Summary

Technology	**0.25 μm CMOS**
Chip Area	**0.09 mm^2**
V_{dd} **$I(V_{dd})$** **$f_{in,\ max}$** **Sensitivity**	**2.2 V** **26.8 mA** **5.5 GHz** **300 mV pk., SE**
o/p phase noise **(5.5 GHz signal i/p)**	**-131 dBc / Hz** **@ 1 kHz**
V_{dd} **$I(V_{dd})$** **$f_{in,\ max}$** **Sensitivity**	**1.8 V** **17.4 mA** **4.5 GHz** **300 mV pk., SE**
o/p phase noise **(4.5 GHz signal i/p)**	**-133 dBc / Hz** **@ 1 kHz**

Comparison of CMOS dividers

		Tech.	$f_{in,\ max}$ GHz	V_{dd} V	P_d mW	Input V_{pk}	Phase Noise (input ref.) dBc/Hz@1kHz
This work	**÷220 … ÷224**	**0.25 μm**	**5.5**	**2.2**	**59**	**0.3**	**-83.2**
De Muer '98	÷8/9	0.7 μm	1.5	5.0	55	0.16	-93.9
Kurizu '97	÷4	0.15 μm	11.8	2.0	20	1.0	
Craninckx '95	÷2	0.7 μm	1.7	3.0	7.5		-87.9
Razavi '95	÷2	0.1 μm	13.4	2.6	26	1.3	
Foroudi '95	÷16	1.2 μm	1.5	5.0	13	0.35	
Cong '88	÷4/5	0.4 μm	4.2	3.5		0.5	
Maeda '97	÷256	0.2 μm	14.5	0.6	22	1.0	

Conclusions

- Programmable divider for HiPerLAN in CMOS.
- Retiming circuit for reliable phase switching.
- 5.5 GHz low voltage ÷2 stage in 0.25μm CMOS.
- Low phase noise achieved at a high input frequency.

Acknowledgments

- W. Fischer for layout, V. Boccuzzi for testing.
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