Fall 2004; E6316: Analog Systems in VLSI; 4 bit Flash A/D converter

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You are required to design a 4bit Flash A/D converter at 500 MS/s. The block diagram is shown in Fig. 1.

1   Specifications

- The A/D should have 4 bits of resolution and operate at 500 MSamples/s.

- The range of the A/D converter should be 1 V differential

- The circuit should use a 3.3 V supply and be designed using 3.3 V transistors (nch3, pch3) in the technology `tsmc025`.

- The circuit should be fully differential

- Use 2x interpolation

- Use a gain of 2 to 4 in the preamplifiers (before the comparators). The preamplifier should have sufficient bandwidth for the worst case test below.

- Design the comparators for the worst case input waveform (Fig. 2. i.e. The preamplifier-comparator combination should recover from a large input to correctly detect the sign of a small input of the opposite sign.

- You can choose the common mode level of the input as long as the maximum input voltages do not go beyond the supply rails ($\{0, 3.3\}$ V). The input source has a $50\,\Omega$ resistance at each differential input.

- You can choose the common mode level and the amplitude of the clock input as long as the maximum clock voltages do not go beyond the supply rails ($\{0, 3.3\}$ V). You can use single ended or differential clock inputs. Use ideal sources followed by $50\,\Omega$ resistances for the clock sources. You can use either sinusoidal or rectangular clocks. The rise and fall times <u>cannot be less than 20%</u> of the clock period.

- You can choose the internal common mode voltages as you wish.

- The current sources in the comparators should be realized using MOS transistors (e.g. Fig. 4). You can use ideal current sources to supply the reference branch current.

- Try to minimize the power dissipation while meeting the above specifications.
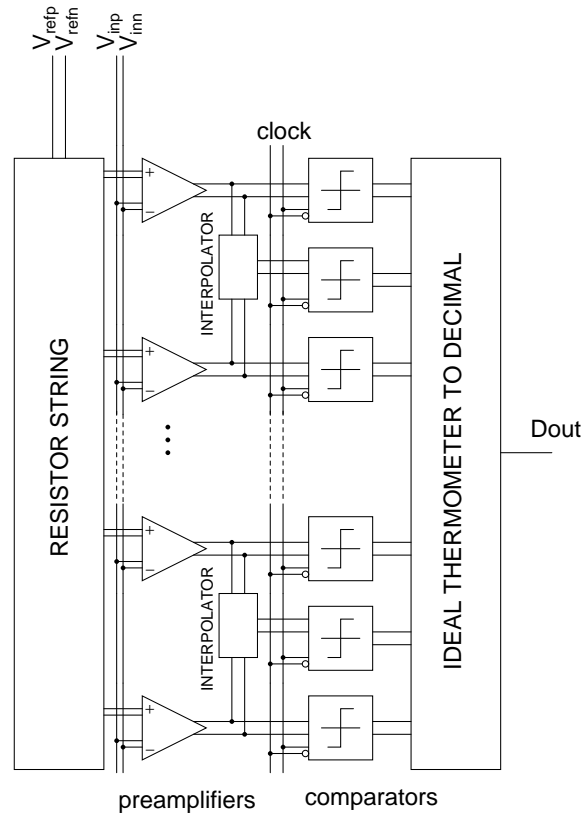
Figure 1: A/D converter block diagram

2 Report

Please submit a single document including all the following.

- A brief description of the design of each stage

- Schematics—use a sensible hierarchy

- DC characteristics of the A/D converter. INL and DNL.

- The Signal to Noise and Signal to Distortion ratios of the A/D converter for sinusoidal inputs of peak to peak value $V_{ref}/4$ and V_{ref} and $f_{in}/f_s = 1/64, 31/64$.

- Transient simulation with a sinusoidal input of an amplitude half the full scale and $f_{in} = 5/64 f_s$. Plot the input and the output of the thermometer to decimal decoder one below the other.

- Power consumption of the A/D converter. Breakdown of the power consumed in each stage (Resistor string, preamplifiers, comparators).

- Transient simulation of a preamplifier followed by a latch with the input alternating between (See Fig. 2)

    1. +1 LSB and -1 LSB.

    2. +15 LSB and -1 LSB.

In addition to these, you also need to submit the Cadence database of your design. Instructions for these will be provided later.
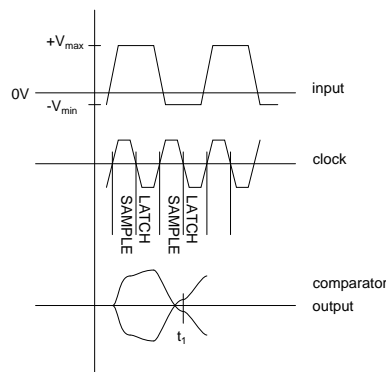

Figure 2: Comparator specifications

3   Design

The design has been covered in the class at an architectural level. Design of the building blocks will be covered in subsequent classes. The building blocks given here are guidelines. You can use different circuit topologies, while sticking to the given basic architecture.

3.1   Architecture

You can use the architecture in Fig. 1. It consists of a resistor string that provides the reference voltages followed by an interpolating string which gives $2^N - 1$ comparisons. This is followed by an array of comparators which convert the analog "comparisons" to digital levels. For easy comparison of the digital output to the input, an idealized thermometer to decimal converter is used.

3.2   Resistor string

A differential resistor string is shown in Fig. 3. You can assume that you have ideal reference voltage sources $V_{refp,n} = V_{cm,ref} \pm V_{ref}/4$. Design the string such that there is no transition at 0 V input in the

A/D converter characteristics. You also need to determine the number and the value of output voltages such that interpolation by 2x results in 15 comparisons as required in a 4 bit converter.
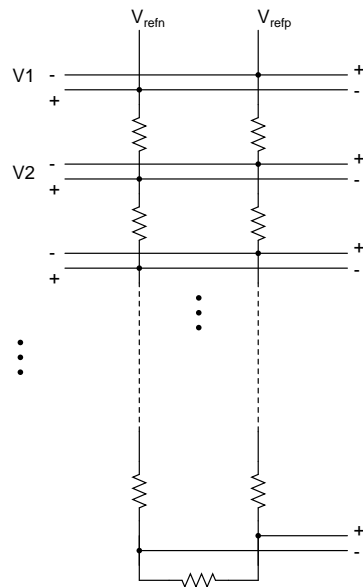

Figure 3: Resistor string

3.3 Preamplifiers

A differential difference preamplifier is shown in Fig. 4. The differential voltage $V_{ip} - V_{in}$ is compared to $V_{rp} - V_{rn}$. In this design, the common mode voltages of the input and the reference voltages need to be equal. The differential output is positive if the input is larger than the reference and negative otherwise.
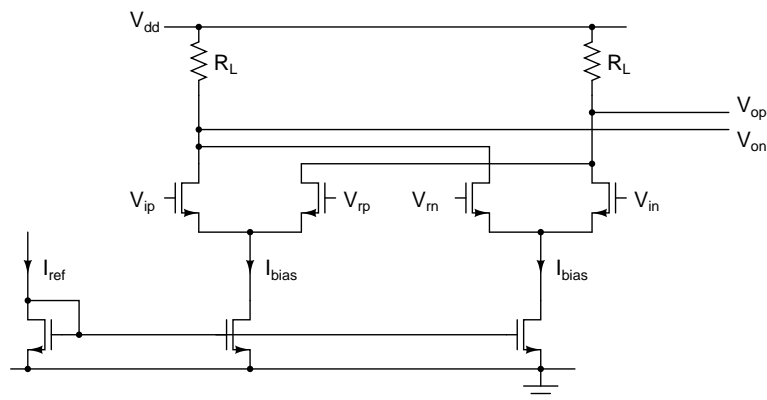

Figure 4: Preamplifier

3.4 Comparator

To determine the sign of the preamplified voltage a comparator, such as the one in Fig. 5 can be used. A cascode structure is used to minimize the effect of output switching on the input. A clock is used to reset the output after each cycle.
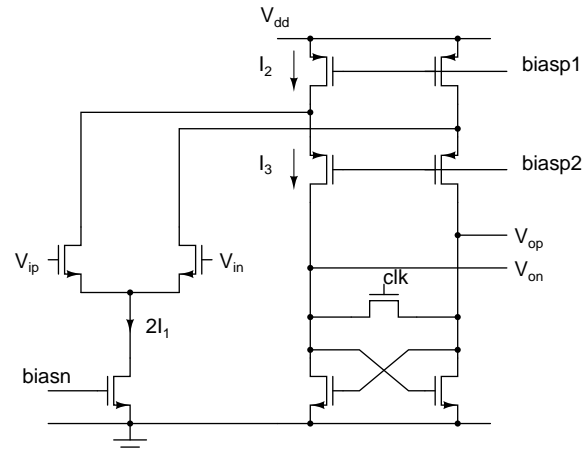

Figure 5: Comparator

3.5 Interpolation

Fig. 6 and Fig. 6 show two techniques for interpolating between preamplifier voltages. In the passive interpolation method shown in Fig. 6, resistors are used between preamplifier outputs for interpolation. In Fig. 7, comparators with two inputs are used for interpolation. Passive interpolation reduces the preamplifier gain by reducing the load resistance. Active interpolation doesn't have this problem, but needs extra differential pairs in the comparator.

3.6 Thermometer to decimal converter

In this project, you won't be designing the decoder or the bubble correction logic. You will use an ideal thermometer to decimal converter—in other words, a D/A converter with a thermometer input—to "decode" the digital output of the comparators. One way of realizing this is shown in Fig. 8. It is basically a current steering DAC. By adjusting the gain of the voltage controlled current sources and the load resistor, the output can be scaled. Having an LSB of 1 V makes the output a decimal representation of the thermometer code. The values can also be adjusted to obtain the same range as the A/D converter in which case, the output can be overlaid on the input for comparison.
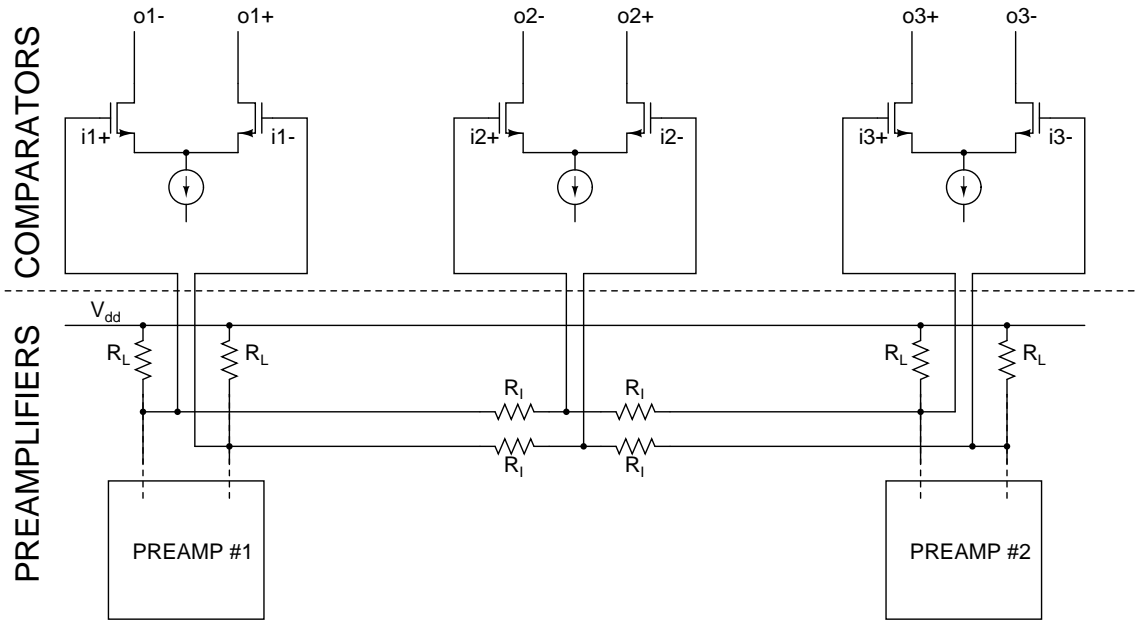
Figure 6: Interpolation using resistive dividers

4 Simulations

4.1 Differential sources

Fig. 9 is a convenient way of ensuring that signals are differential and have a given common mode voltage.

4.2 DC characteristics of the A/D converter

DC characteristics imply that the input is constant, or changing very slowly. The A/D converter is still being clocked. So this has nothing to do with "dc" analysis. A convenient way to determine the DC characteristics is to have an input that slowly ramps up the input voltage. The input is adjusted so that it ramps up by a small fraction of the LSB ($V_{LSB}/16$ or less) in every clock cycle. The output of transient analysis (for a sufficiently long duration) can be used to determine the switching thresholds of the A/D converter (correct to $LSB/16$). See Fig. 10. Make sure that the initial transients have fully settled before applying the ramp.

4.3 Signal to Noise and Signal to Distortion ratios

For these, take the DFT of the digital output from the ideal thermometer to decimal converter. Make sure that you sample once every cycle as outlined in the handout on "Distortion Analysis of Sampled Signals". The DFT will contain the fundamental, the harmonics and the other components. Signal to distortion ratio is the ratio of the fundamental to the harmonics (Take the 2nd and 3rd harmonics; Add their rms values). The ratio of signal to noise is the ratio of the fundamental to the sum of all other components in the DFT. Ignore the DC term as this may include bias related components. Report the DC term separately.
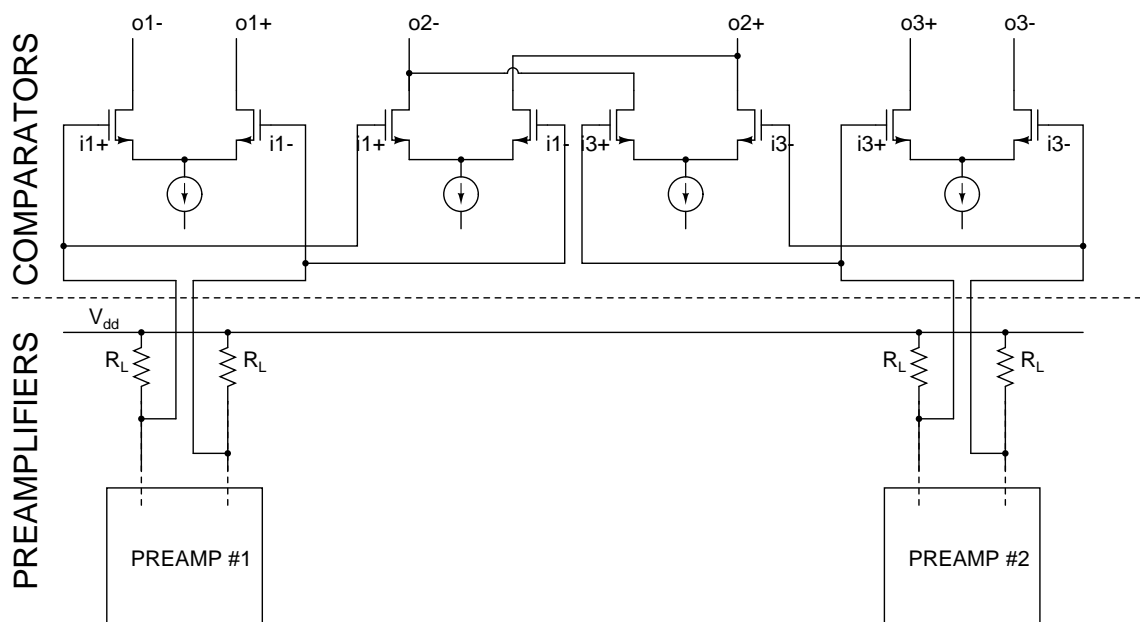
Figure 7: Interpolation using multiple input differential pairs in the comparators

4.4 Hierarchy

Use of a sensible hierarchy can significantly ease the simulation process. e.g. in the block diagram in Fig. 1, the resistor string, the preamplifier array, the comparator array, and the thermometer to decimal decoder can each be a subcircuit. In the preamplifier array, each preamplifier cell would be a subcircuit. The whole A/D converter can be a subcircuit which you would drop into your simulation "bench". Of course you would have separate simulation benches for testing separate parts of the circuit.

4.5 Parameterization

Parameterization of subcircuits helps where you have a large number of components of related values. e.g. in the A/D converter, the resistance values in the resistor string can be parameterized (using `pPar(``parameter'')`) facility in Cadence.

5 Timeline

The specs are not hard to meet in the given technology. The main purpose of the project is to get familiar with all the steps involved in the design of an A/D converter.

There are 5 weeks to the deadline. You should be able to finish this project easily in that time. You should plan to keep to the foll. timeline.

- Week 1: Resistor string, Ideal thermometer to decimal converter; design and simulation

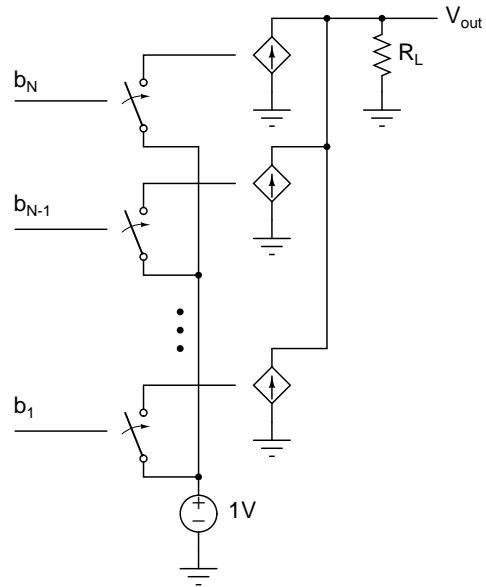- Weeks 2: Preamp and comparator; design and simulation

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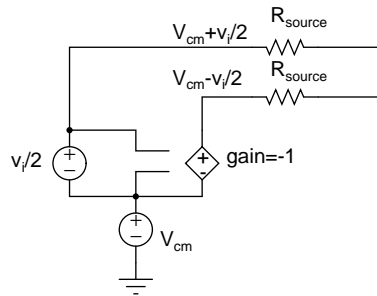Figure 8: Ideal thermometer to decimal converter

Figure 9: Differential voltage source

- Week 3: Putting the whole circuit together; basic verification; generation of input sources required for all simulations.

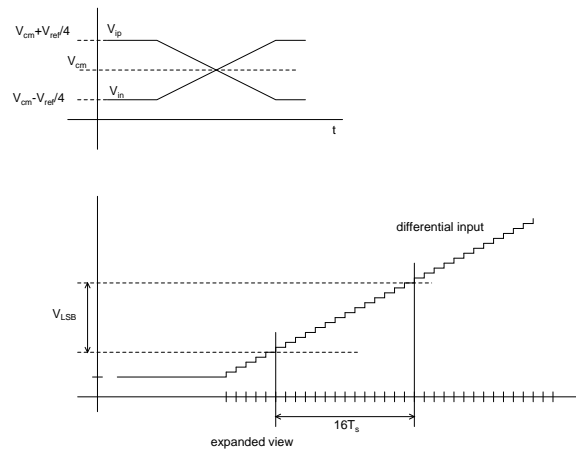- Week 4,5: Extensive simulations and report writing.

Figure 10: Input to determine the DC characteristics of the A/D converter